Guidelines for Verilog-A Compact Model Coding

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DOLPHIN Integration

Outline

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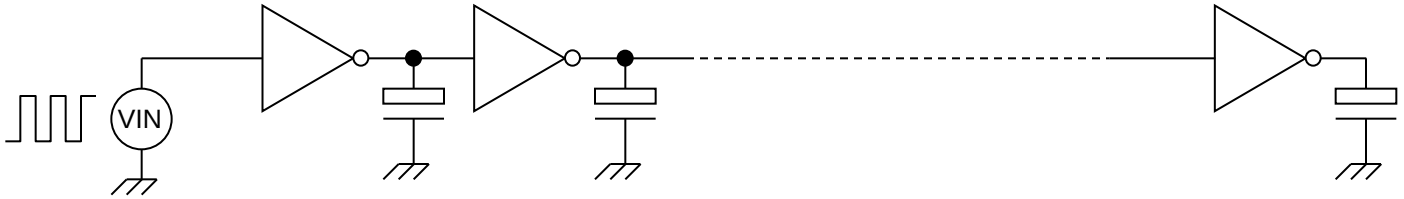
Context & Goals

- What needs to be done so that Verilog-A can become the standard for CM coding?
  - Benchmarking performed to understand current status and provide guidelines
    - Results presented at MOS-AK in Frankfurt (Oder)
  - Guidelines put together for CM coding
- What is at stake?
  - Fully taking into account SPICE-like integration of Verilog Compact Models in the ecosystem
  - Providing a viable and open alternative to “controlled” initiatives (such as TMI or CMI)

Benchmark of Verilog-A vs. SPICE Conditions



Test bench:

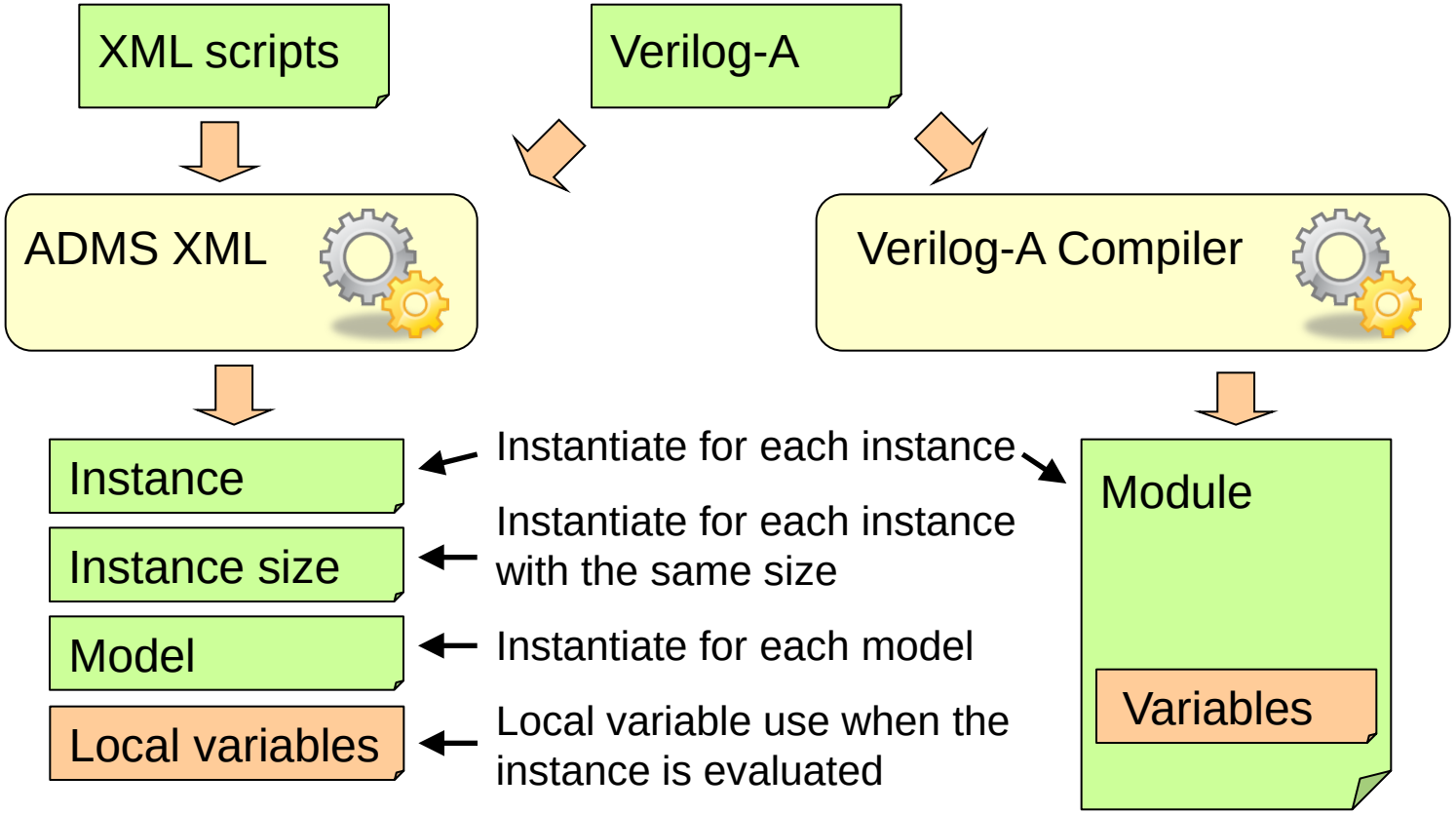
- Configurable CMOS delay (400, 4k or 40k MOS)
- Use default values for the parameters of the MOS models
- Use two models, on PMOS and one NMOS
- Computed iterations 2550±5
- Use TRAP method for integration

Benchmark of Verilog-A vs. SPICE Memory

Memory usage (Mb)		SMASH		Simulator B		Ratio Verilog-A / SPICE
		SPICE	Verilog-A	SPICE	Verilog-A	
PSP Model	Circuit #1 400 MOS	38 Mb	75 Mb	15 Mo	19 Mb	1.2
	Circuit #2 4k MOS	55 Mb	407 Mb	65 Mo	96 Mb	1.7
	Circuit #3 40k MOS	204 Mb	Too big	566 Mo	854 Mb	4.1
EKV3 Model	Circuit #1 400 MOS	39 Mb	68 Mb	NA	15 Mb	0.4
	Circuit #2 4k MOS	51 Mb	305 Mb	NA	62 Mb	1.2
	Circuit #3 40k MOS	166 Mb	Too big	NA	436 Mb	2.7

Verilog-A Limitations
Memory Consumption

- Model / Instance size / Instance



Benchmark of Verilog-A vs. SPICE Transient Speed

Simulation time (seconds)		SMASH		Simulator B		Ratio Verilog-A / SPICE
		SPICE	Verilog-A	SPICE	Verilog-A	
PSP Model	Circuit #1 400 MOS	1.2 s	32.4 s	3.1 s	28.5 s	23.1
	Circuit #2 4k MOS	17.7 s	675.4 s	40.3 s	405.1 s	22.9
	Circuit #3 40k MOS	216.5 s	Too big	421.1 s	8565.8 s	39.6
EKV3 Model	Circuit #1 400 MOS	2.1 s	47.7 s	NA	30.1 s	14.2
	Circuit #2 4k MOS	30.5 s	872.9 s	NA	339.2 s	11.1
	Circuit #3 40k MOS	375.2 s	Too big	NA	6676.7 s	17.8

Verilog-A Limitations
Simulation Speed

- Implementation dependent
  - Flow/Potential branches
  - Derivation/Integration
  - Bypass/Linearization
  - Iteration specific code vs. specific code (initialization, noise)
  - Hidden states
  - Extra nodes
    - added for correlated noise due to ADMS XML limitation
- Language (or coding) standard dependent
  - Iteration specific code vs. specific code (output variables)
  - Conditional nodes (collapsible nodes)

Benchmark of Verilog-A vs. SPICE Transient Speed

Simulator B					
Simulation time (seconds)	SPICE	PSP #1	PSP #2	PSP #3	Ratio Verilog-A / SPICE
Circuit #1 400 MOS	3.1 s	35.5 s	28.5 s	23.73 s	7.7
Circuit #2 4k MOS	40.3 s	3182.6 s	405.1 s	247.08 s	6.1
Circuit #3 40k MOS	421.1 s	> 230400 s	8565.8 s	5 793.38 s	13.8

PSP #1: model with 2 noise nodes and with 5 collapsible nodes

PSP #2: model with 2 noise nodes and without collapsible node

PSP #3: model without noise node and without collapsible node

Recommendations #1
Subset of Verilog-A

- Language: limit to the use of Verilog-A; digital Verilog-HDL is not relevant here.
- Data types: limit to the use of integer and real data types.
- Use only scalar, do not use vectors or arrays.
- Disciplines and natures: limit to the use of electrical discipline with voltage and current natures.
- Contribution statements: limit to the use of current (flow) versus voltages (potential).
- Port branches: do not access currents through module ports.
- Analog operators: limit to the use of ddt, ddx and idt, limit the order to one. Do not combine these operators between themselves.
- Do not use analysis functions.
- Do not use AC stimulus.
- Do not use system tasks and functions except the hierarchical parameter $mfactor.
- Do not use analog event control statements.
- The compact model is not hierarchical; do not use module instantiation or any hierarchical structures.

Recommendations #2
Focus on Spice integration

- **Completeness**: The model should be complete which means that it should contain everything needed by the final user for analog design.
  - For instance: include equations for NPN and PNP for a bipolar, or NMOS and PMOS for a MOS.
- **Port order**: SPICE primitives use ordered port connections; keep this order in the model, and use common port names (i.e. drain, gate, source, bulk for MOS primitives for instance).

EKV3	✓	Ok
PSP	✓	Ok
JUNCAP2	✓	Ok
HICUM	✗	Equations for PNP are not included

Recommendations #3
Focus on Spice integration

- **Common instance parameters**: SPICE primitives have predefined or common parameters.
  - For instance: W, L, AD, AS, PD, PS and NF for MOS or AREA for bipolar.
- **Instance/Model parameters**: contrarily to Verilog-A, SPICE makes a clear distinction between instance and model parameters.

EKV3	✓	NF was changed during EKV3 development to match the common meaning
PSP	✓	Ok
JUNCAP2	✓	Ok
HICUM	✗	Parameter AREA is not included

Recommendations #4
Focus on Spice integration

- **Parameter description**: for each instance and model parameter, give a short description using the info attribute, and specify its unit, if any, using the unit attribute.
- **Output variables**: they can be printed or plotted by SPICE simulators. Common variables like gm, gmds, gds or transistor state for MOS transistors should be defined.

EKV3	✗	Too few parameter descriptions (less than 10%) Output variables gm, gmds, gds and transistor state are not defined
PSP	✗	Transistor state is not defined
JUNCAP2	✓	Ok
HICUM	✗	Output variables gm, gpi, gmu, g0, beta and ft are not defined

Recommendations #5
Focus on Spice integration

- **Functional sections**: compact models have a large number of equations, which are not all needed at every phase of every type of analysis. To help model builders generate more efficient SPICE simulator code, we recommend to split the code at least into the following four sections using named blocks:
  - Model initialization
  - Instance initialization
  - Instance evaluation
  - Noise

EKV3	✗	We added the noise section
PSP	✓	Ok
JUNCAP2	✓	Ok
HICUM	✓	Ok

Recommendations #6
Focus on Spice integration

- **Noise types**: in SPICE, noise is generally divided into three categories: thermal, flicker, shot noise. When possible, we recommend to use one of these categories for specifying the noise source label in Verilog-A.
- **Port current probe**: avoid use of I(<port_name>) probes to define a current contribution. In some implementations, it will add an extra node which penalizes simulation speed.

EKV3	✗	Too many noise labels are used
PSP	✗	Too many noise labels are used
JUNCAP2	✓	Ok
HICUM	✗	Flicker noise is not marked with a label

Recommendations #7
Focus on Spice integration

- **ddt of ddt**: avoid use of derivative or integral of order greater than one.
- **Pure and impure**: to enable SPICE optimizations such as bypass or linearization, the instance evaluation section should be pure.
- **Collapsible nodes**: collapsible nodes have the benefit that they reduce the size of the system matrix. They should be defined during the instantiation phases, so they should be a function of model or instance parameters only. Avoid collapsing two ports, or one port and the ground.

EKV3	✓	Ok
PSP	✓	Ok
JUNCAP2	✓	Ok
HICUM	✗	Thermal port is collapsed with ground

Conclusion

- For the moment, SPICE simulators remain faster than their Verilog-A counterparts.
  - Compact models in Verilog-A should target SPICE simulators and respect the inherent constraints to facilitate their integration into different SPICE simulators.
- EDA vendors will fill this gap between SPICE and Verilog-A simulators. Therefore, the time is coming to:
  - Make Verilog-A more attractive than SPICE for semiconductor foundries as well as for final users
  - Compete with the “Standard Model API” to address the problems of deep submicron processes such as dynamic degradation, power consumption, system-level complexity…

Thanks!

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