SPICE and Models - Perfect Together

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SPICE and Models - Dead?

SPICE is the analog designer's version of Old Faithful — with the emphasis on “old.” Originally designed for simple designs with a handful of transistors, SPICE can't keep up with the demands of today's many-thousand-transistor designs. Companies are going to have to overcome their fears and shift to a top-down design approach if they want to remain competitive. Just working harder isn’t enough anymore.

Ken Kundert, “Why SPICE Won't Cut It For Analog Anymore,” *Computer Design,* April 1999.

IC Technology Changes in the Last 40 Years

- Design rules in mils (1 mil = 25.4 micron)
- Masks from rubylith
- Chips with a few transistors
- Wafer sizes of one inch
- Packages with a dozen pins

- Design rules in nanometers
- Masks from e-beam
- Chips with a few billion transistors
- Wafer sizes of twelve inches
- Packages with hundreds of pins

Moore's Law

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer."

Gordon Moore, *Electronics Magazine*, 1965

Moore's Law

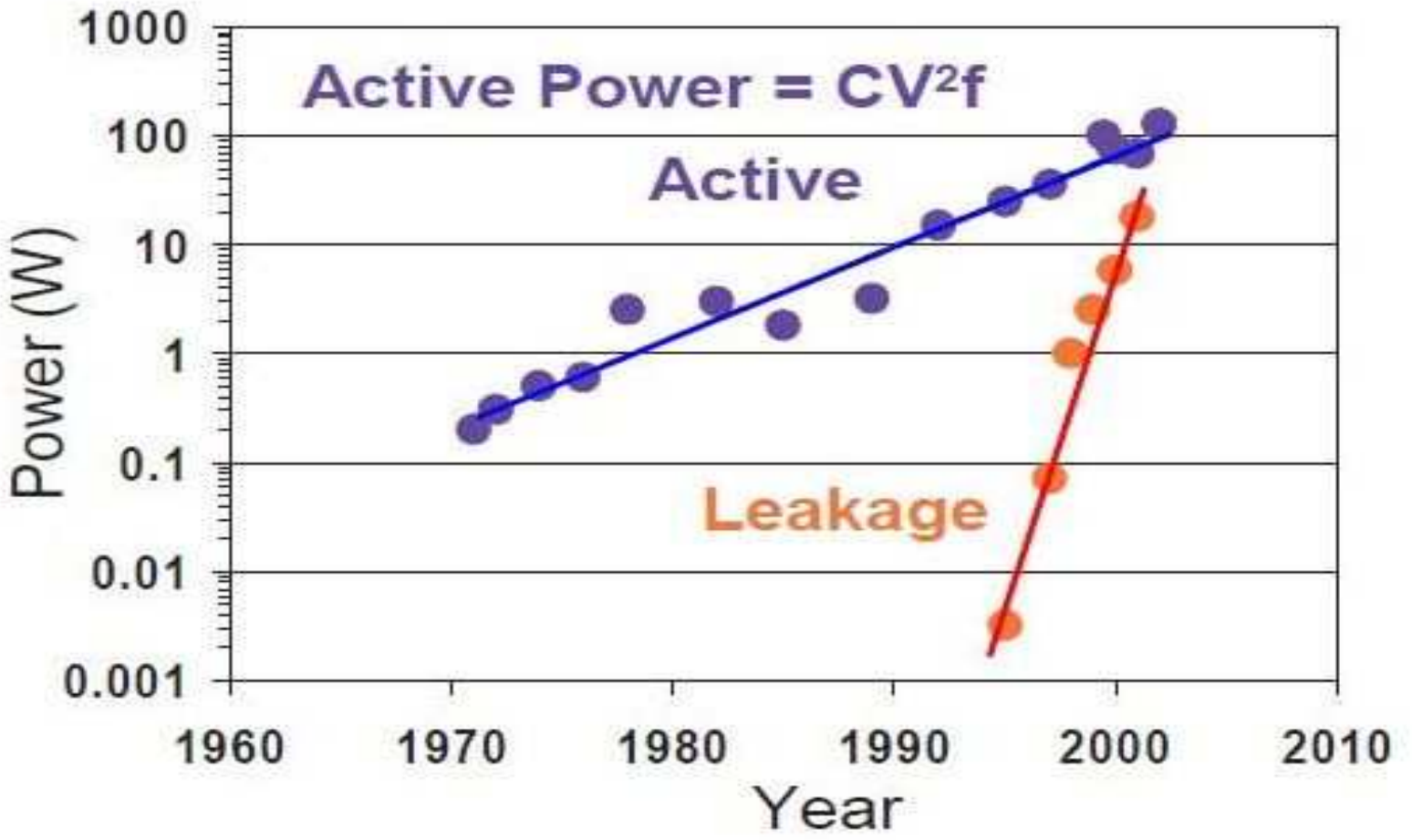
- Design rules decrease by a factor of $\sqrt{2}$ every two years (1,000X in 40 years)
- Because of shrinking design rules, the transistor density increases by a factor of 2 every two years (1,000,000X in 40 years)
- Therefore, the per function cost of electronics decreases by a factor of 2 every two years (assuming that the cost per cm^2 doesn't change)

Corollaries to Moore's Law

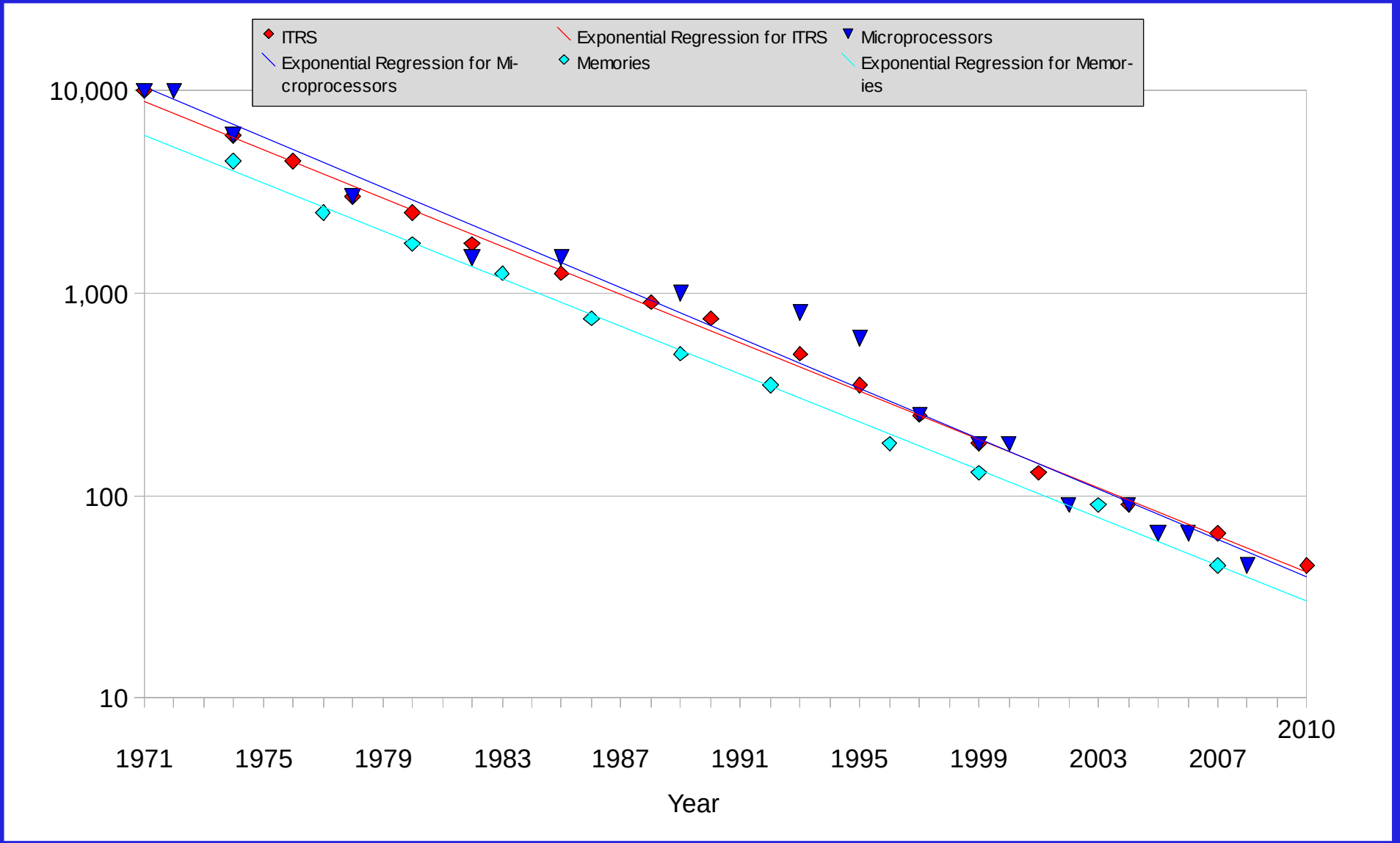
- The switching speed of a transistor decreases by a factor of $\sqrt{2}$ every two years. The maximum frequency of operation increases by the same factor.
- Because device capacitance and parasitic capacitance decreases by a factor of $\sqrt{2}$ every two years, and the clock rate (can) increase by a factor of $\sqrt{2}$ every two years, the per function power ($CV^2 f$) was supposed to stay constant. Unfortunately, this neglected leakage current!

The Leakage Problem

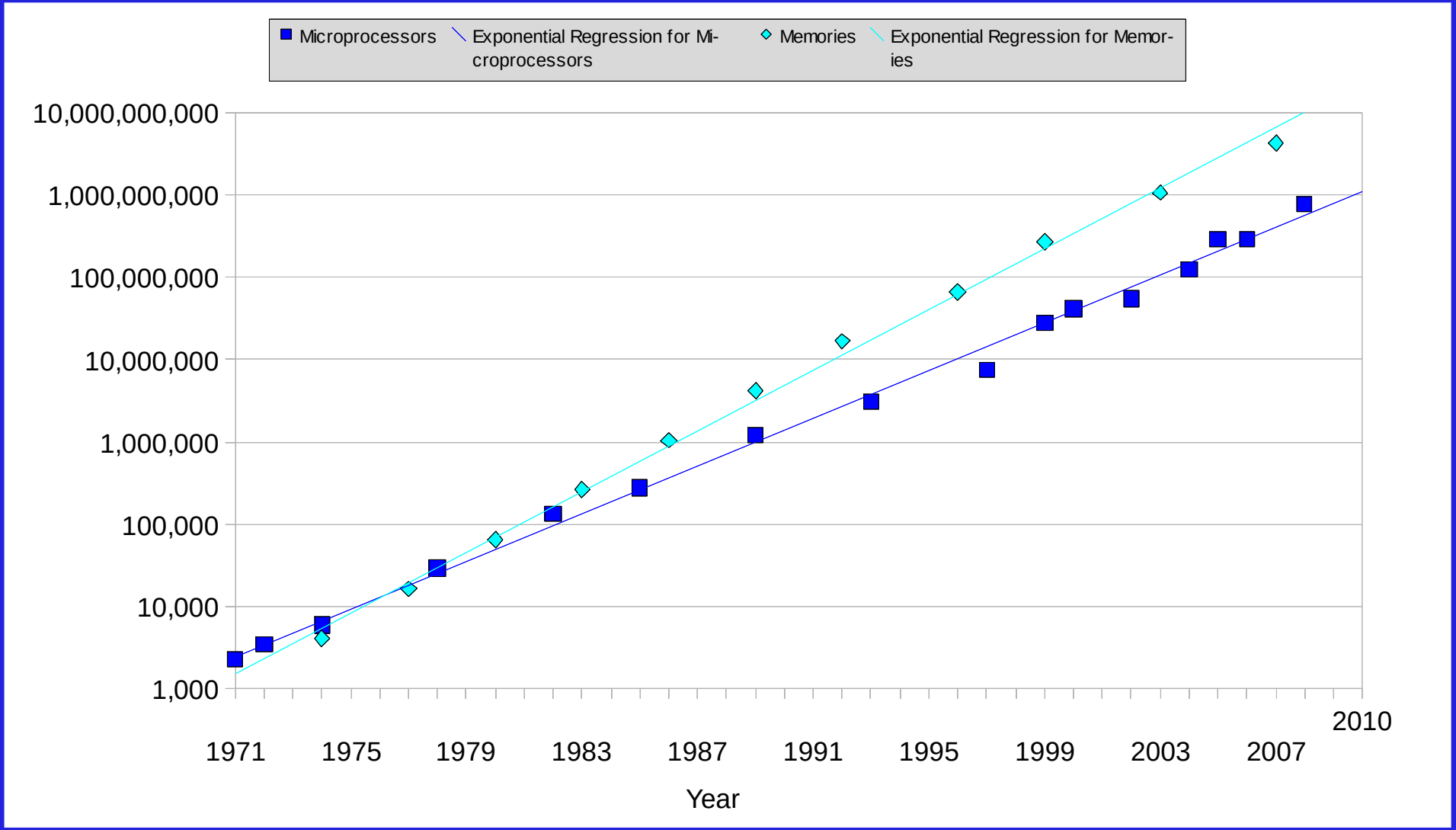
Paul Packer, CICC 2008 Short Course



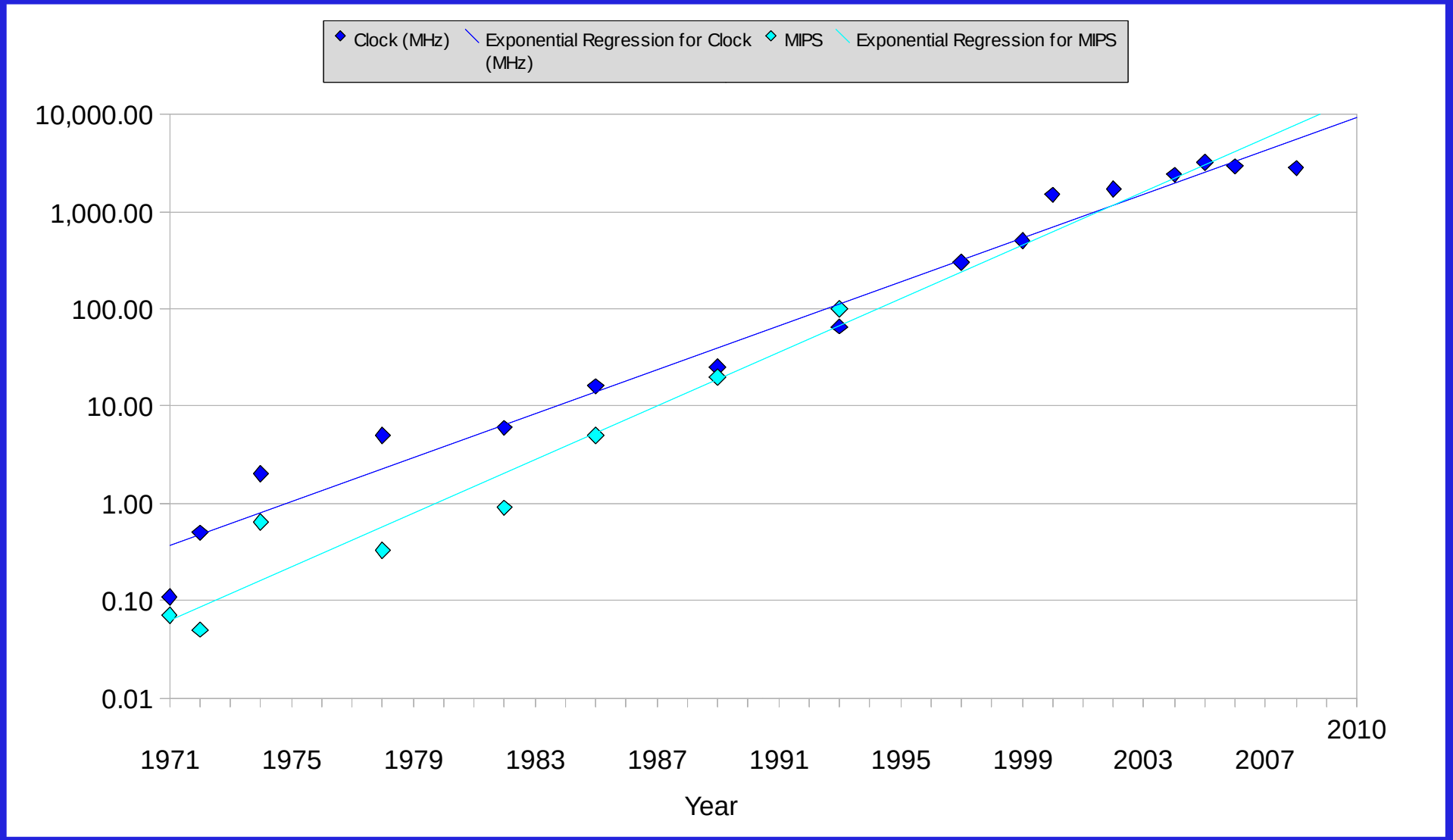
Moore's Law - Technology (nm)



Moore's Law - Transistors



Microprocessor Clock Speed (MHz)



SPICE and Models Time Line
Before SPICE

- 1947 - Point Contact Transistor Invented
- 1954 - Ebers-Moll BJT Model Published
- 1959 - Planar Integrated Circuit Process Invented
- 1960 - MOS Transistor Invented
- 1963 - Complementary MOS Invented
- 1966 - Pao-Sah MOS Transistor Model Published
- 1966 - ECAP Simulation Program Published
- 1971 - Gummel-Poon BJT Model Published

SPICE (Simulation Program with Integrated Circuit Emphasis)

- DC operating point analysis, small-signal AC analysis and transient analysis in one package
- Built-in models for diodes and bipolar transistors
- Modified Newton-Raphson iteration with heuristics that worked well with bipolar circuits
- Implicit integration techniques reduced problems with the widely spread time constants of an IC
- Utilized sparse matrix techniques, so it could run circuits with hundreds of nodes

A Perspective on Computing in the '70s

- The computer at UC Berkeley in the '70s was a CDC 6400
- The input to the computer was punched cards
- The output of the computer was a line printer
- The MIPS rate was comparable to an Intel 286 (1 MIPS)
- The maximum available memory was 100,000 octal 60 bit words daytime and 140,000 octal at night (comparable to 256 KByte)

SPICE and Models Time Line
The SPICE Era

- 1973 - SPICE1
- 1975 - SPICE2
- 1981 - HSPICE
- 1984 - PSPICE
- 1984 - Eldo
- 1985 - BSIM MOSFET
- 1986 - SPECTRE
- 1989 - SPICE3

The SPICE Era

- SPICE applications were
  - Analog circuits (small)
  - Critical paths in digital circuits
  - Memories
- SPICE algorithms were tuned to go faster but not work smarter
- Model development driven by technology evolution and digital circuits
- Emergence of “funny” circuits (switched-C)

SPICE Corollary of Moore's Law

SPICE CPU = Timepoints

* (Newton Iterations / Timepoint)

* (CPU / Newton Iteration / Transistor)

* (Transistors)

SPICE Corollary of Moore's Law

- Timepoints increase by at least $\sqrt{2}$ every two years
- Newton Iterations / Timepoint is constant
- CPU / Newton Iteration / Transistor is simply the CPU required to evaluate a device model. This has been relatively constant.
- Transistors increase by at least $\sqrt{2}$ every two years
- This is at least an N^2 Process!!!

SPICE Corollary of Moore's Law

- Fortunately, computer CPUs get faster by $\sqrt{2}$ every two years

Still…

- SPICE CPU consumption doubles every four years!!!

SPICE and Models
Challenges of the '90s

- By the end of the 1980's, at around the 1µm technology node, it was clear that smarter techniques were necessary
- There were numerous problems brought on by shrinking design rules
- As transistors became faster, it became possible to integrate RF circuits and the wireless explosion was on. This necessitated an entirely new line of algorithms and simulators

SPICE and Models Time Line
More Model Development

- 1995 - VBIC BJT Model
- 1995 - EKV MOSFET
- 1995 - HiSim MOSFET Model
- 1998 - SP MOSFET Model
- 1999 - HiCUM BJT Model
- 2001 - Phillips MOSFET Model 11
- 2005 - PSP MOSFET Model

SPICE and Models Time Line
RF Simulation

- 1988 - Microwave Design System (MDS)
- 1991 - Libra
- 1994 - ADS
- 1996 - SPECTRE RF
- 1998 - Eldo RF
- 2004 - HSPICE RF

SPICE and Models
Consequences of Smaller Dimensions

- Device variability and mismatch becomes increasingly important; using usual ± 3σ files misses important effects of mismatch
- Devices are placed closer to each other, increasing unintended coupling between devices
- Reduced design rules increase proximity effects, from wells and stress
- Reduced design rules increase the importance of parasitics, and result in incredible complexity of “accurate” extracted netlists

SPICE and Models
Consequences of Higher Frequencies

- Reduced device dimensions results in devices that can operate at much higher frequencies, which requires models that are accurate at higher frequencies
- RF operation requires a special class of simulator and algorithms that can simulate RF performance
- RF performance (distortion, phase noise) is much more sensitive to second-order device effects and derivatives of charge and current

SPICE and Models
Consequences of More Complexity

- Increased device density enables the integration of complex systems that include digital, RF, and analog circuitry on the same chip
- More complex chips require more ancillary circuitry for performing self testing, self calibration, and many different modes of operation
- Complex circuits require advanced simulation algorithms (especially in RF) and specialty analyses in MATLAB or Python Scripts

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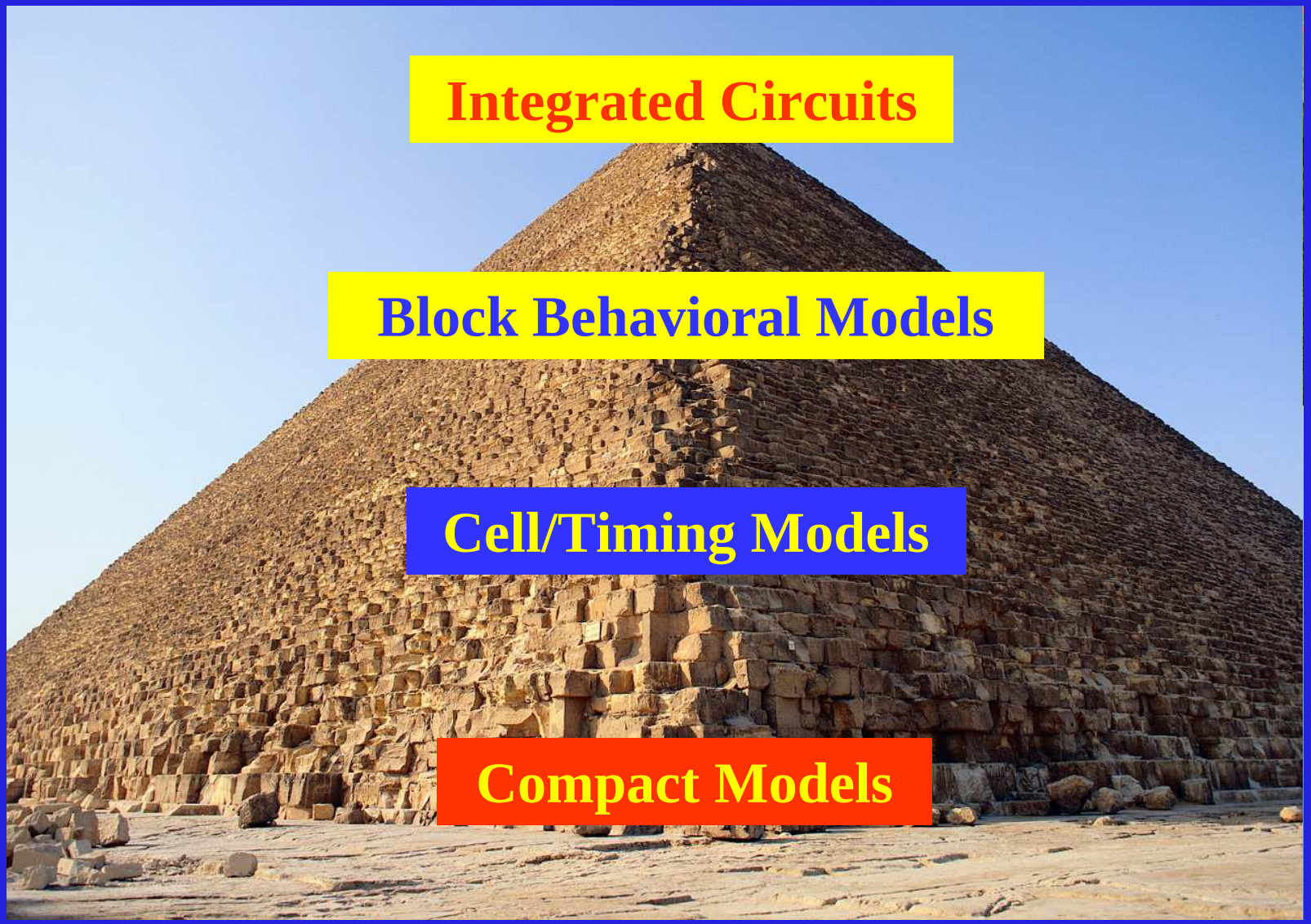
Are SPICE and Models Dead?
No!!! Not if …

- We can simulate analog blocks described in an Analog Hardware Description Language (AHDL)
- We can simulate different blocks in different domains (RF, analog, digital) using different algorithms
- We can simulate different blocks of a system in parallel
- We can exploit the inherent latency of most systems


Integrated Circuits
Block Behavioral Models
Cell/Timing Models
Compact Models