

# Modeling of the Subthreshold Characteristics of Triple-gate Transistors: Impact of the Channel Dimensions and Back-gate Bias

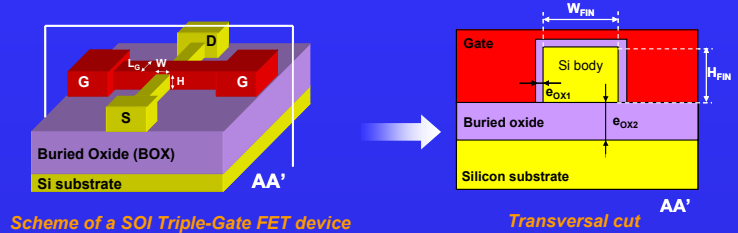


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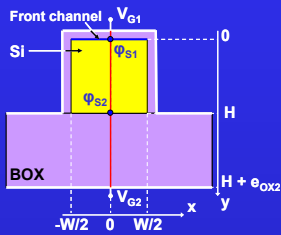


## 1. Context & motivations

- Triple-gate devices [1][2]:
  - Candidates for further scaling of logic devices
  - Excellent subthreshold characteristics ( $I_{OFF}$ , SS, DIBL) control
- Assumptions:
  - Long channels
  - Undoped channels
  - Under the subthreshold regime (negligible carrier concentration)
  - Quantum confinement neglected ( $W$  &  $H > 10$  nm)



## 2. Solution of the Poisson's equation



• Truncation of the complete solution at the first order; unfitted model ( $\lambda_2 = 2\sqrt{2}$ ) and fitted model ( $\lambda_2$  depending on the geometrical dimensions):

• potential in the vertical direction at the center of the device:

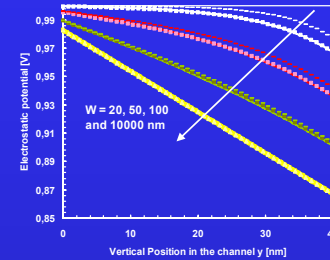
$$\varphi(y) = \varphi_{s1} + \frac{\text{sh}(y/\lambda_2)}{\text{sh}(H/\lambda_2)} (\varphi_{s2} - \varphi_{s1})$$

• Applying Gauss' theorem at the front and back interfaces yields:

$$V_{G1} = V_{FB1} + \varphi_{s1} + \frac{\epsilon_{Si}}{C_{OX1}} \frac{1}{\lambda_2 \text{th}(H/\lambda_2)} (\varphi_{s1} - \varphi_{s2})$$

$$V_{G2} = V_{FB2} + \varphi_{s2} + \frac{\epsilon_{Si}}{C_{OX2}} \frac{1}{\lambda_2 \text{th}(H/\lambda_2)} (\varphi_{s2} - \varphi_{s1})$$

- $\varphi_{s1}$  considered constant along the top channel
- Front channel inversion corresponding to the threshold voltage of the whole device



Comparison between Finite Elements solution (squares; obtained with [3]) and Fitted (plain lines)/Unfitted (dashed lines) models

W [nm]	lambda_2 [nm]	lambda_2 [nm]	lambda_2 [nm]	lambda_2 [nm]	lambda_2 [nm]	lambda_2 [nm]	lambda_2 [nm]	lambda_2 [nm]	lambda_2 [nm]
10	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
20	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
50	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
100	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
250	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
500	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
1000	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
2500	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
5000	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
10000	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00

Fit parameters a table ( $\lambda_2 = W/a$ )

## 3. Threshold voltage model

- Considering the potentials when the back-gate is driven into inversion/depletion/accumulation, threshold voltage model derived [4,5]:

Back - gate into accumulation ( $V_{G2} < V_{G2,ACC} = V_{FB2} - \frac{\epsilon_{Si}}{C_{OX2}} \frac{\varphi_{ST}}{\lambda_2 \text{th}(H/\lambda_2)}$ ):

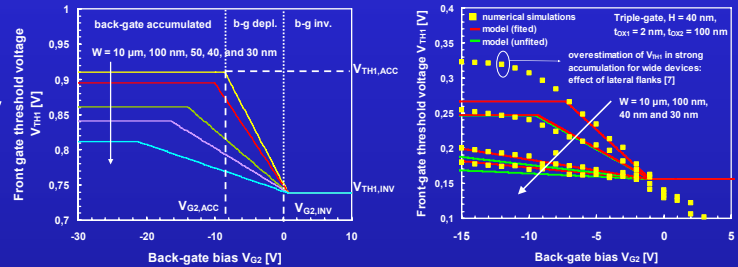
$$V_{TH,ACC} = V_{FB1} + \frac{\epsilon_{Si}}{C_{OX1}} \frac{\varphi_{ST}}{\lambda_2 \text{sh}(H/\lambda_2)}$$

Back - gate into depletion ( $V_{G2,ACC} < V_{G2} < V_{G2,INV}$ ):

$$V_{TH,DEP} = V_{FB1} - \frac{\epsilon_{Si}}{C_{OX1}} \frac{1}{\lambda_2 \text{th}(H/\lambda_2)} (V_{G2} - V_{FB2}) + (1 + \frac{\epsilon_{Si}}{C_{OX1}} \frac{1}{\lambda_2 \text{th}(H/\lambda_2)} (\frac{1}{1 + \frac{\epsilon_{Si}}{C_{OX2}} \frac{1}{\lambda_2 \text{sh}(H/\lambda_2)}})) \varphi_{ST}$$

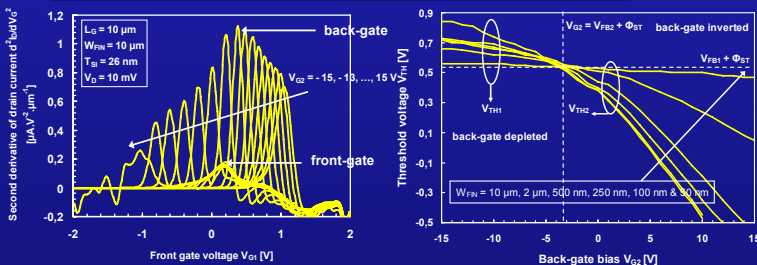
Back - gate into inversion ( $V_{G2} > V_{G2,INV} = V_{FB2} + \varphi_{ST}$ ):

$$V_{TH,INV} = V_{FB1} + \varphi_{ST}$$



Model of front gate threshold voltage  $V_{TH1}$  vs. back-gate bias  $V_{G2}$  for various fin width  $W$  (squares; obtained with [6]) and Fitted (red lines)/Unfitted (green lines) models

Excellent accordance for fitted model, correct for purely geometrical model



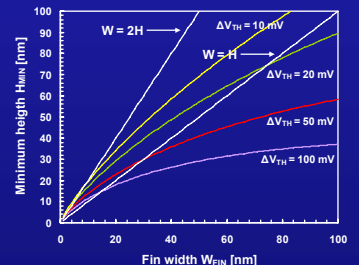
Simulated second derivative of the drain current vs. Back-gate bias  $V_{G2}$ . Two peaks in back-gate inversion appear

Experimental front gate threshold voltage  $V_{TH1}$  vs. back-gate bias  $V_{G2}$  for various fin width  $W$  (from [7])

Experimental existence of an invariant point between back-gate depletion and inversion regimes, marking the prior inversion of the front or the back-channel

- Considering the maximum amplitude (difference between the two plateaus):

$$H_{MIN}(W, \Delta V_{TH}) = \lambda_2 a \sinh\left(\frac{\epsilon_{Si} \varphi_{ST}}{C_{OX1} \Delta V_{TH} \lambda_2}\right)$$



Minimum Fin height  $H$  vs. Fin width  $W$  for various  $\Delta V_{TH}$

For  $W < 2H$ , back-gate influence very significantly reduced

## 4. Conclusions

- Fully compact and versatile model for multi-gate transistors
- Accuracy adjustable with geometrical fit parameters
- Model validated by numerical simulations and experimental measurements
- Invariant point predicted by the model experimentally observed
- Definition of a geometrical criterion – if respected, the effect of the back-gate can be neglected

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