Advances in SOI Compact Modeling

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ROVIRA I VIRGILI UNIVERSITY

COMON

Outline

Presentation of the COMON project

1. Introduction
2. Charge based compact models
3. Conformal mapping
4. Fourier's series
5. Conclusions

Outline

Presentation of the COMON project

- Who are we?
- Goals

1. Introduction
2. Charge based compact models
3. Conformal mapping
4. Others techniques
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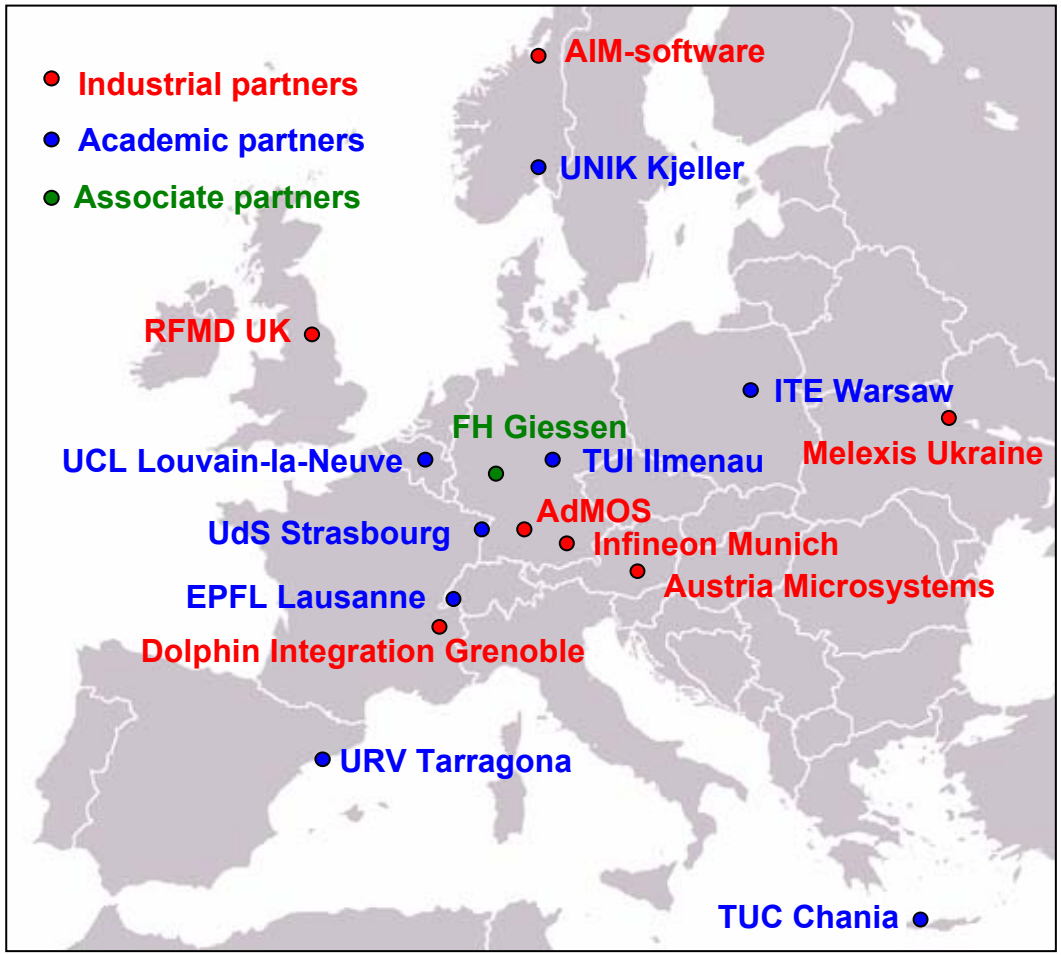
EU COMON Project – Who are we?

COMON: COmpact MOdeling Network



✓ "Marie-Curie" Industry-Academia Partneship and Pathways project (IAPP FP7, ref. pro. 218255)

✓ Duration: 4 years, started from Dec. 2008.

✓ Coordinator: Prof. B. Iñiguez (URV Tarragona) benjamin.iniguez@urv.cat

➢ More information available on our website: http://www.compactmodelling.eu

EU COMON Project – Goals

- To address the full development chain of Compact Modeling, to develop complete compact models of Multi-Gate MOSFETs (Foundry: Infineon), HV MOSFETs (Foundry: Austriamicrosystems) and III-V FETs (RFMD (UK)).

- Development of complete compact models of these types of advanced semiconductor devices.
- Development of suitable parameter extraction techniques for the new compact models.
- Implementation of the compact models and parameter extraction algorithms in automatic circuit design tools.
- Demonstration of the implemented compact models by means of their utilization in the design of test circuits.
- Validation and benchmarking: compact model evaluation for analog, digital and RF circuit design: convergence, CPU time, statistic circuit simulation.

+ facilitate the mobility of young researchers, secondments of knowledge, organisation of training courses, ...

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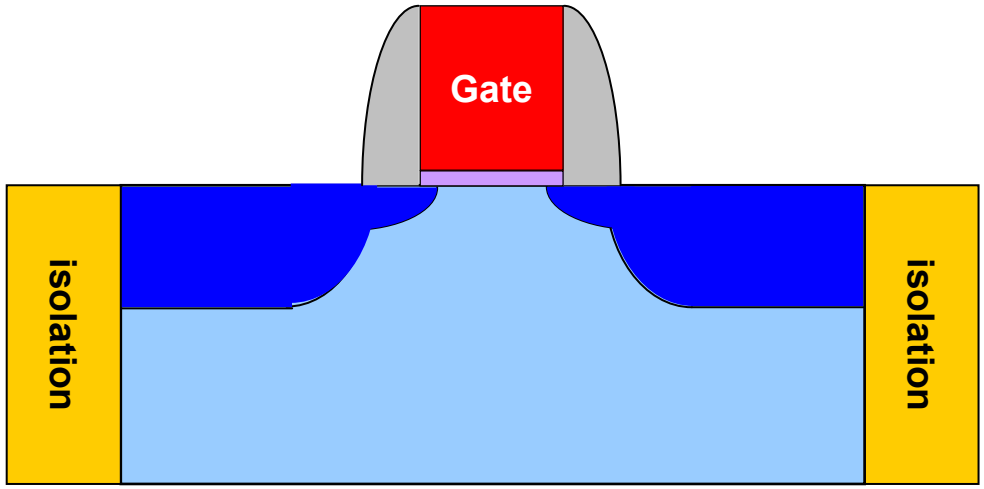
1. Introduction
   - SOI technology
   - Why several gates?
   - Multi-gate SOI structures benchmark
2. Charge based compact models
3. Conformal mapping
4. Others techniques
5. Conclusions

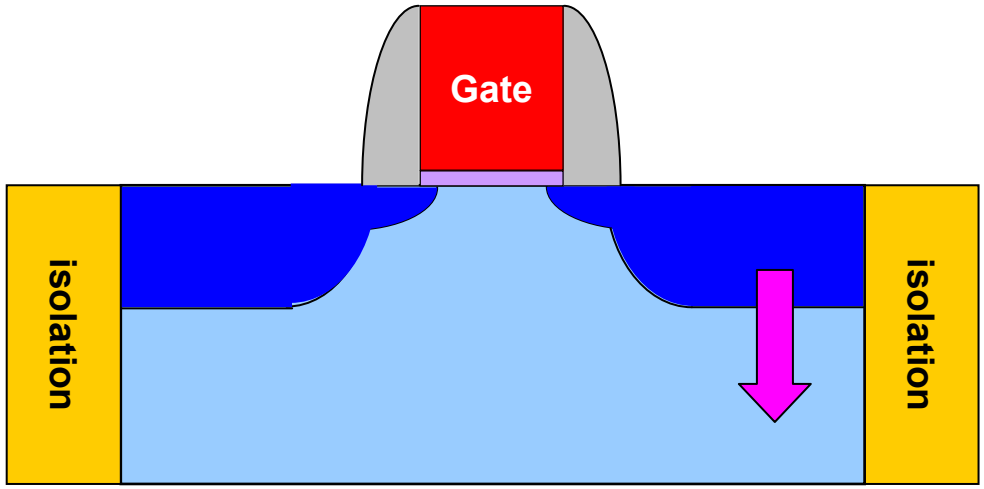
1.1 SOI technology

- Necessity to reduce the gate length while maintaining a good electrostatic control and controling the leakages



1.1 SOI technology

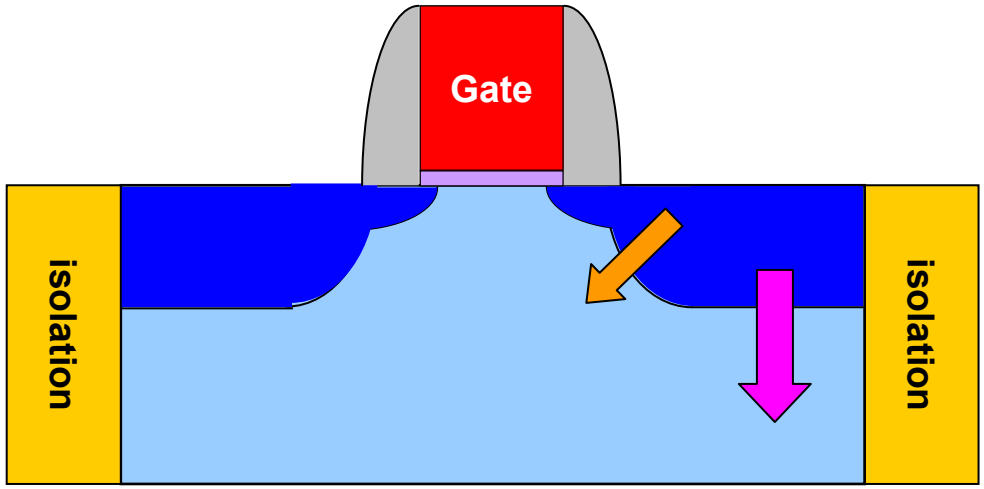
- Necessity to control the gate length while maintaining a good electrostatic control and controling the leakages



Junction leakages

1.1 SOI technology

- Necessity to control the gate length while maintaining a good electrostatic control and controling the leakages

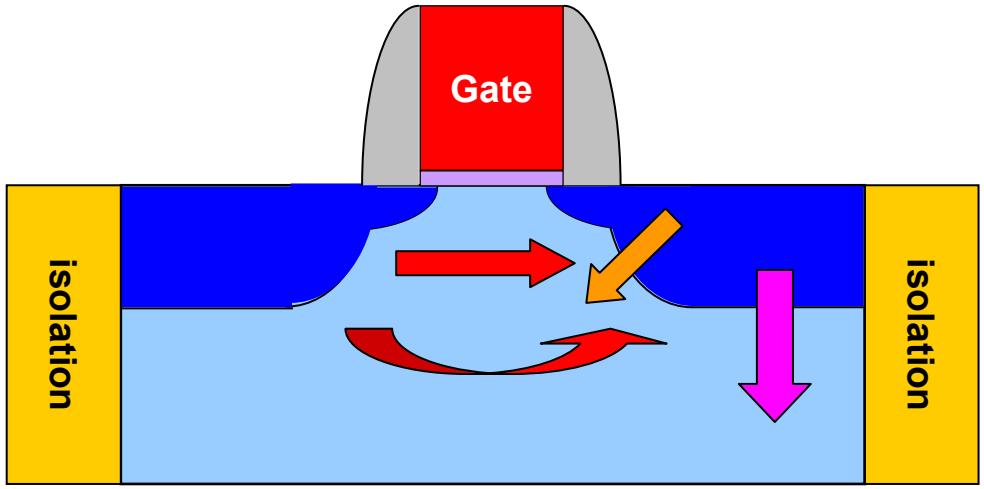


Junction leakages

High field effects in the drain

1.1 SOI technology

- Necessity to control the gate length while maintaining a good electrostatic control and controling the leakages



Junction leakages

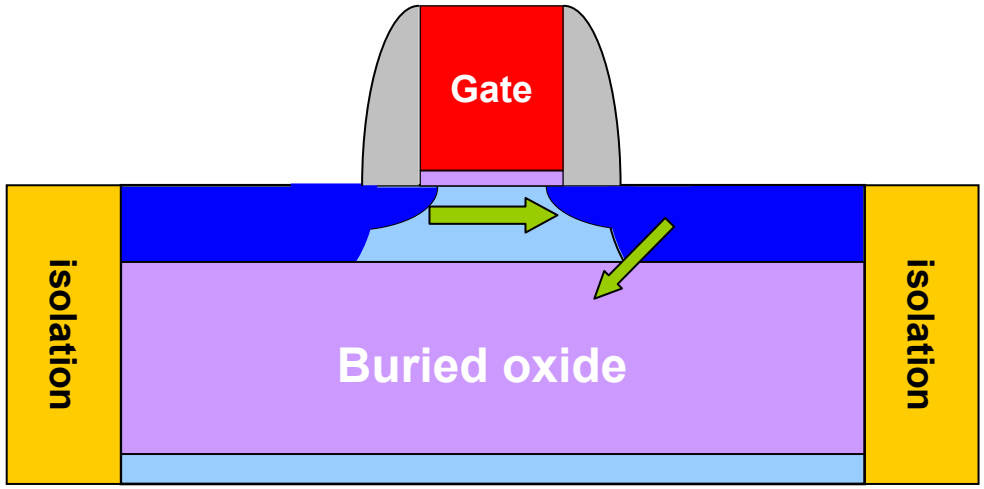
High field effects in the drain

Subthreshold leakages

1.1 SOI technology

➢ Necessity to control the gate length while maintaining a good electrostatic control and controling the leakages

- Isolate the electrically active layer from the bulk
- SOI (Silicon On Insulator) concept



Junction leakages

High field effects

In the drain

Subthreshold leakages

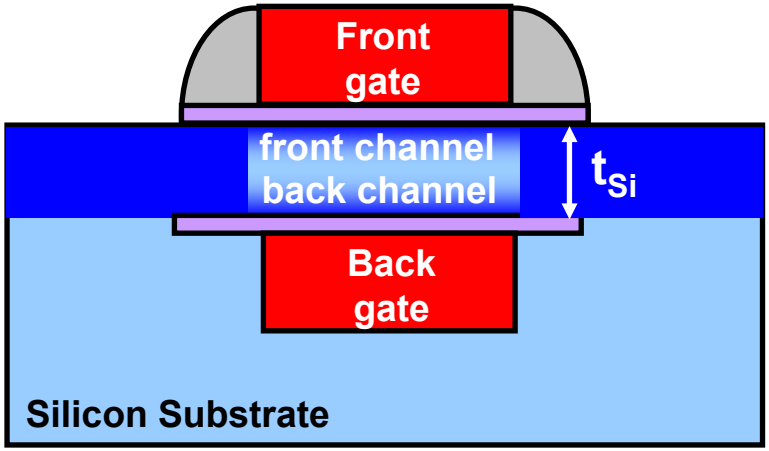
with SOI:

✓ **Reduced parasitic effects – reduction of source/channel and drain/channel capacitances**

✓ **Better electrostatic control**

SOI allows to continue further the downscaling

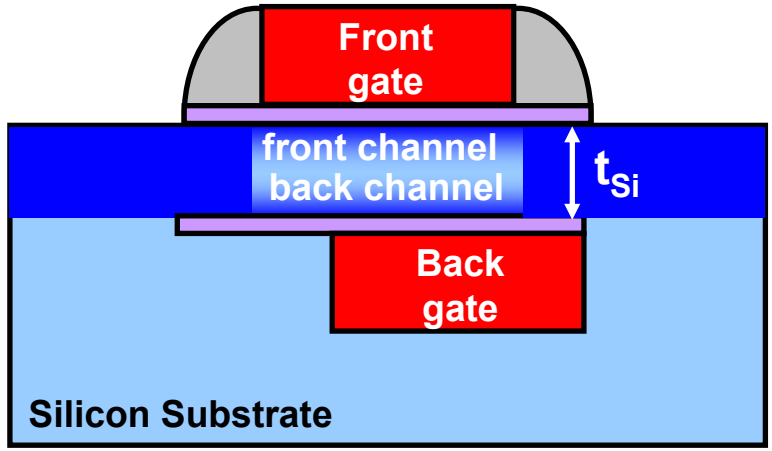
1.2 Why several gates?



'Planar double-gate' architecture

- Double-gate transistor
- Two conduction channels
  - → good I_{ON}
- Excellent electrostatic coupling:
  - → ✓ Short Channel Effects (SCEs) reduction
  - ✓ leakage currents reduction

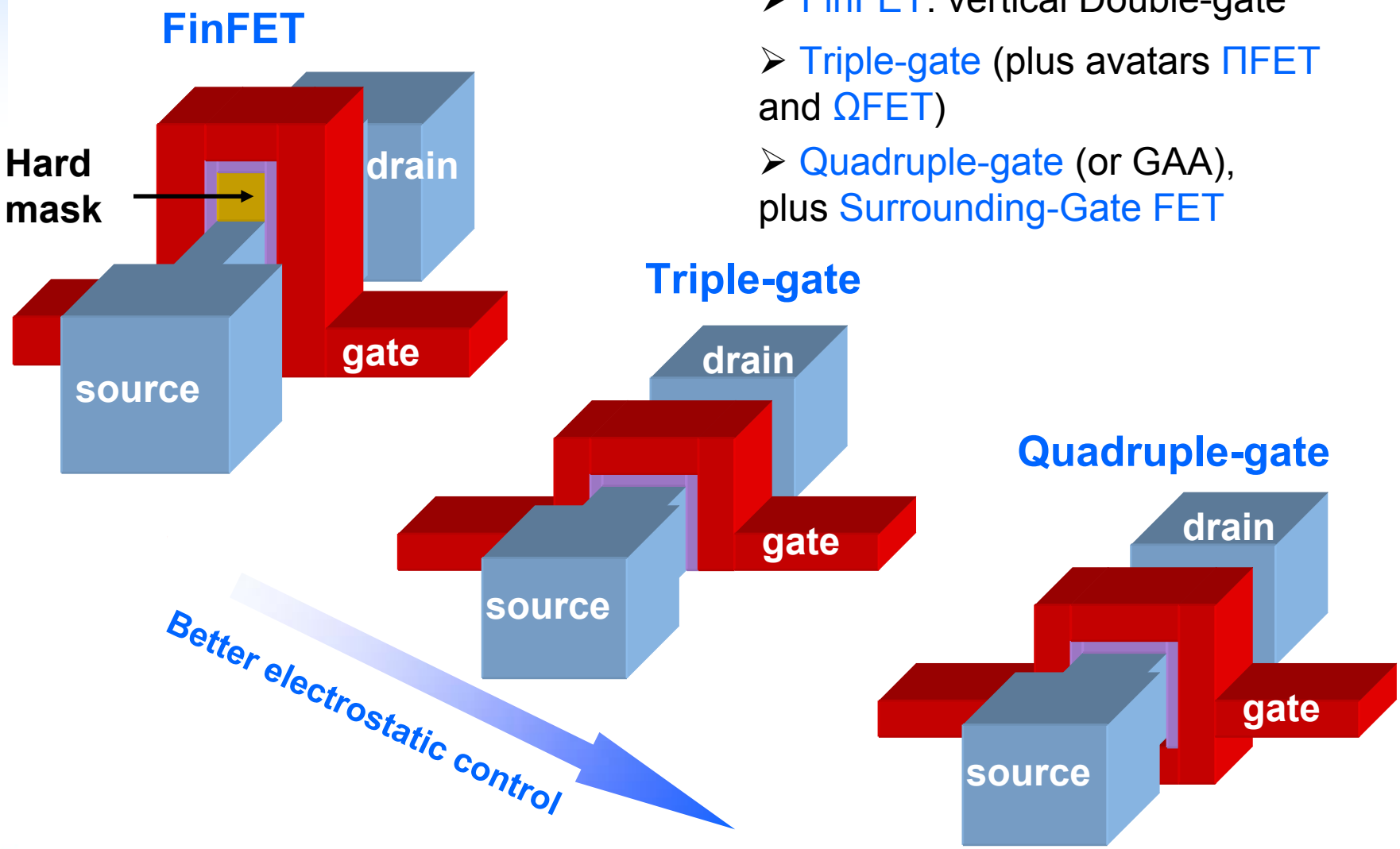
- But self-alignment of the gates required to maintain Double-gate advantages
  - → idea of vertical gates: FinFET type transistors



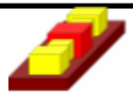
Gate misalignment

1.2 FinFET-like transistors

- FinFET: vertical Double-gate
- Triple-gate (plus avatars ΠFET and ΩFET)
- Quadruple-gate (or GAA), plus Surrounding-Gate FET



1.3 (non exhaustive) SOI Benchmark

		State of the art	Main advantages	Main drawbacks	Potential for sub-30 nm nodes
Bulk Single-gate		Production	. Well known process	. Short Channel Effects Control	NO / MAYBE
Strained Single-gate		Development	. Increased mobility	. Relaxation of strained layers for small dimensions	YES
Partially Depleted SOI		Development	. Pragmatic technology	. Floating body effects	MAYBE
Fully Depleted SOI		Development	. No Floating body effects	. Thin and well-controlled thicknesses mandatory . Fringing fields in the BOX	YES
Double-gate SOI		Research	. Two channels conduction . Good electrostatic control	. Gate self-alignment . Thin channel thickness mandatory.	YES
FinFET SOI		Research	. Self aligned technology . Relatively CMOS compatible	. Lithographic pitch . Source/Drain Doping . Access resistances	YES
Triple-gate SOI		Research	. Three conduction channels . Self aligned technology	. Lithographic pitch . Source/Drain Doping . Access resistances	YES
Gate All Around SOI		Research	. Good electrostatic control	. Not a very pragmatic technology . Source/Drain Doping . Access resistances	YES
Multichannels		Research	. Integration density . Good electrostatic control	. Difficult process . Source/Drain Doping . Access resistances	YES

1.3 (non exhaustive) SOI Benchmark

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Bulk Single-gate		Production	. Well known process	. Short Channel Effects Control	NO / MAYBE
Strained Single-gate		Development	. Increased mobility	. Relaxation of strained layers for small dimensions	YES
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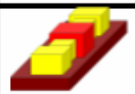
Triple-gate SOI		Research	. Three conduction channels . Self aligned technology	. Lithographic pitch . Source/Drain Doping . Access resistances	YES
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   - Double-gate transistors
   - FinFETs
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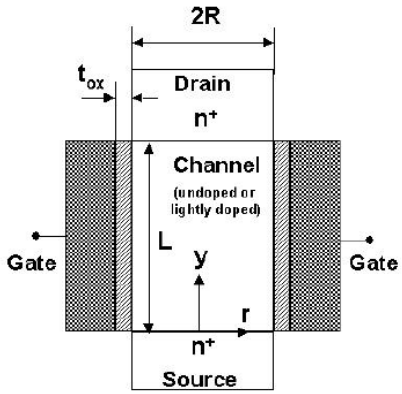
2.1 Surrounding-gate FETs



➢ 1D Poisson's equation (no SCEs):

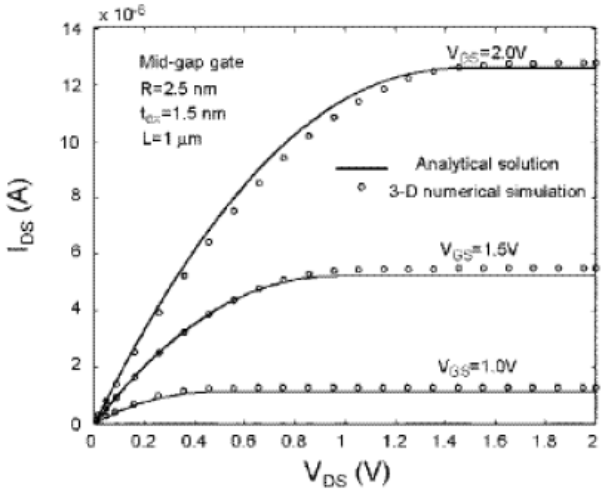
$$\frac{d^2\psi}{dr^2}+\frac{1}{r}\frac{d\psi}{dr}=\frac{kT}{q}\delta\cdot e^{\frac{q(\psi-V)}{kT}}$$

➢ Solving the 1D Poisson's equation [Jimenez'04], charge control model obtained:

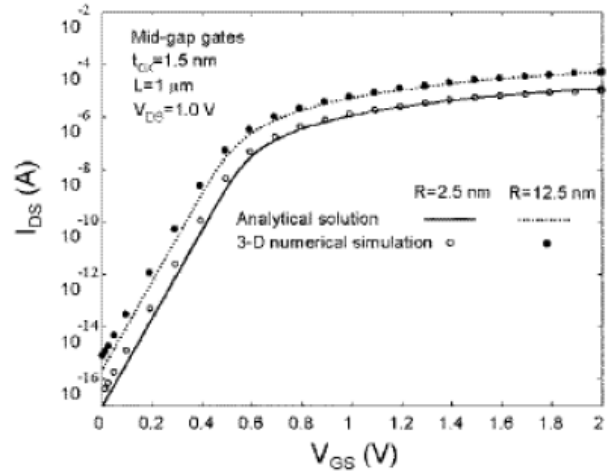
$$(V_{GS}-V_0-V)=\frac{Q}{C_{ox}}+\frac{kT}{q}\log\left(\frac{Q}{Q_0}\right)+\frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

➢ Drain current calculation:

$$I_{DS}=\mu\frac{2\pi R}{L}\int_0^{V_{DS}}Q(V)dV$$



Comparison model/numerical simulations: drain current I_D vs. drain voltage V_D

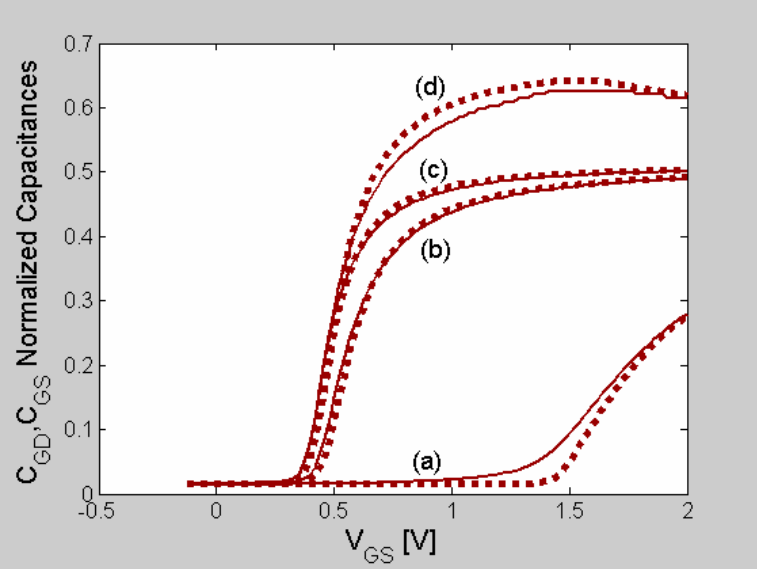


Comparison model/numerical simulations: drain current I_D vs. gate voltage V_G

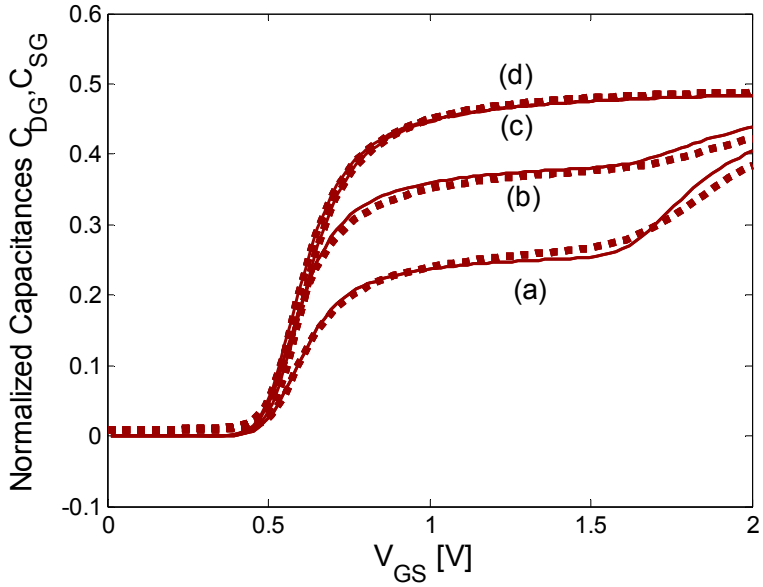
[Jimenez'04] D. Jimenez et al., IEEE EDL, vol. 25, no. 8, pp. 571-573, 2004.

2.1 SGFETs- Capacitance modeling

➢ Analytical expressions [Moldovan'09] of the total electrode charges obtained by integrating the mobile charge density over the channel length. Ward-Dutton partitioning is assumed. Capacitances are obtained by differentiation of total charges.



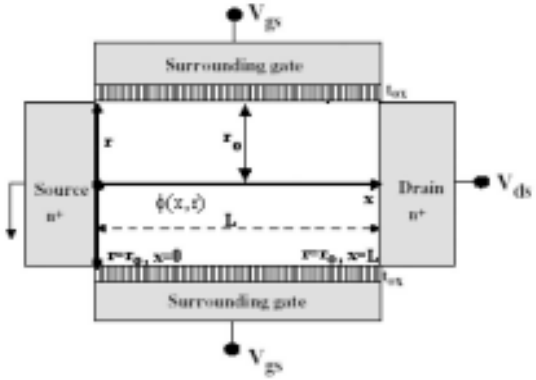
Normalized C_{GD} (a, b) and C_{GS} capacitance (c, d) with respect to the gate voltage, for SG MOSFET V_{DS}=0.05V (b,c) and V_{DS}=1V (a,d). Solid line: DESSIS-ISE simulations; Symbol: analytical model. L=1 μm, t_{Si}=20 nm, t_{ox}=2 nm



Normalized C_{DG} (a, c) and C_{SG} (b, d) with respect to the gate voltage, for SG MOSFET with V_{GB}=0, V_{DS}=1V (a, b) and V_{DS}=0.05V (c, d); t_{si}=31nm. L=1 μm. Solid line: analytical model; Symbols: DESSIS-ISE simulation

[Moldovan'09] O. Moldovan et al., IEEE TED, vol. 54, no. 1, pp. 162-165, 2007.

2.1 SGFETs, short channels effects



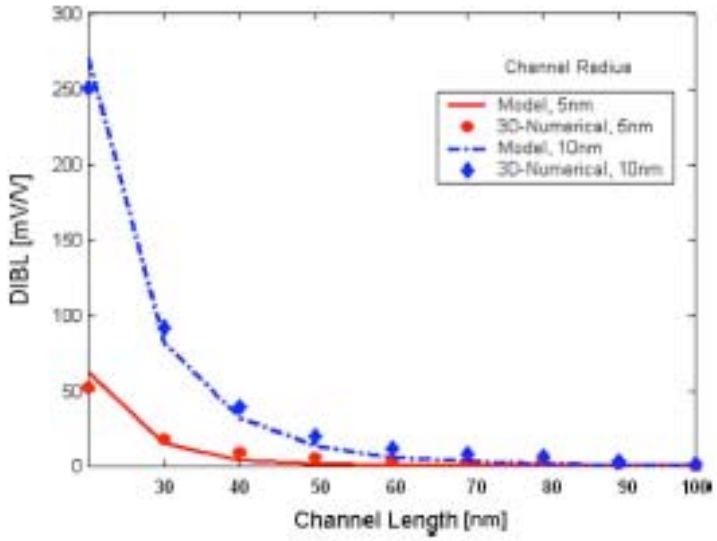
- Inclusion of SCEs [AbdElHamid'07]:

$$\varphi(x,y) = \varphi_1(y) + \varphi_2(x,y)$$

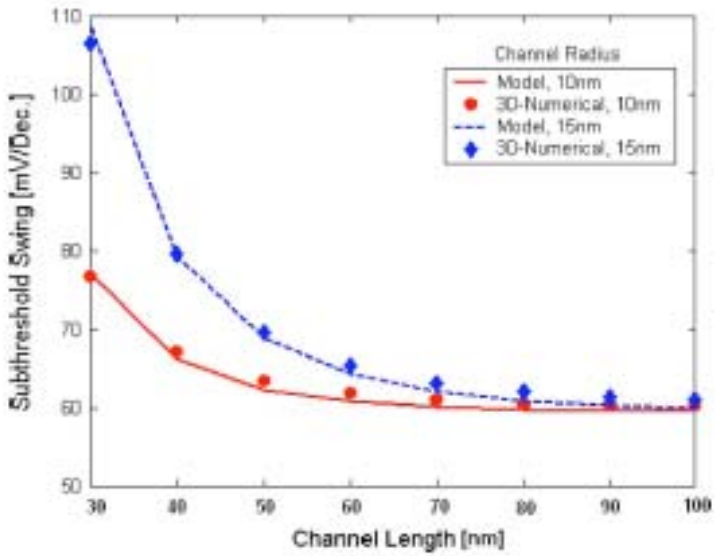
$\varphi_1(y)$ Solution of the 1D Poisson's equation

$\varphi_2(x,y)$ Solution of the remaining 2D equation

- Minimum of potential giving threshold voltage V_{TH} and subthreshold slope SS



DIBL vs. channel length L_G (radius = 5 and 10 nm). Comparison between model (lines) and numerical simulations (circles, diamonds)



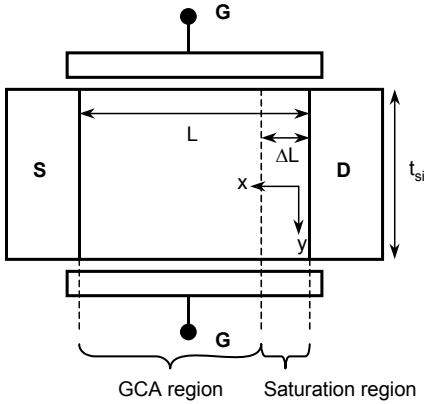
Subthreshold slope SS vs. channel length L_G (radius = 5 and 10 nm). Comparison between model (lines) and numerical simulations (circles, diamonds)

[AbdElHamid'07] H. Abd El Hamid et al., IEEE TED, vol. 54, no. 3, pp. 572-577, 2007.

2.3 Symmetrical Double-gate FETs

COMON

- Transistor in saturation [Lime'08]:



- Electrostatic potential derived from 2D Poisson's equation:

$$\varphi(x,y) = \varphi_1(y) + \varphi_2(x,y)$$

$\varphi_1(y)$ Solution of the 1D Poisson's equation

$\varphi_2(x,y)$ Solution of the remaining 2D equation

$$\phi(x,y) = a + b(x)y + c(x)y^n$$

$$\rightarrow \quad \frac{\partial^2\varphi}{\partial x^2} - \frac{\varphi}{\lambda^2} = 0 \qquad \text{with} \qquad \lambda = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{2\varepsilon_{ox}} + \frac{t_{si}^{\,2}}{8}\left(1 - \frac{2}{n(n+1)}\right)} = \frac{t_{si}}{2}\sqrt{\frac{1}{2} + \frac{1}{2r} - \frac{1}{n(n+1)}}$$

$$\rightarrow \quad \varphi(x) = \varphi_{sat}\cosh\left(\frac{\Delta L + x}{\lambda}\right) + \frac{k\, v_{sat}}{\mu}\lambda\sinh\left(\frac{\Delta L + x}{\lambda}\right) \qquad \text{with}$$

$$\varphi(x = -\Delta L) = \varphi(\phi_S = V_{deff} + \phi_b) = \varphi_{sat}$$

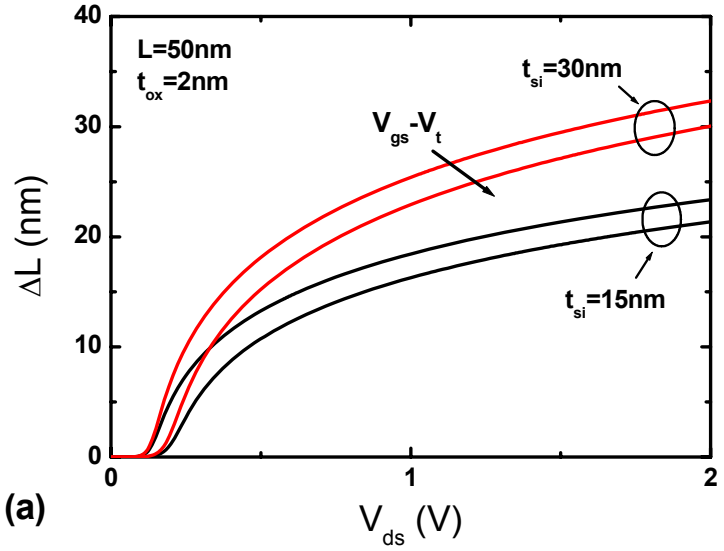
$$\left.\frac{d\varphi}{dx}\right|_{x=-\Delta L} = \frac{k\, v_{sat}}{\mu}$$

NMOS: k=2
PMOS: k=1

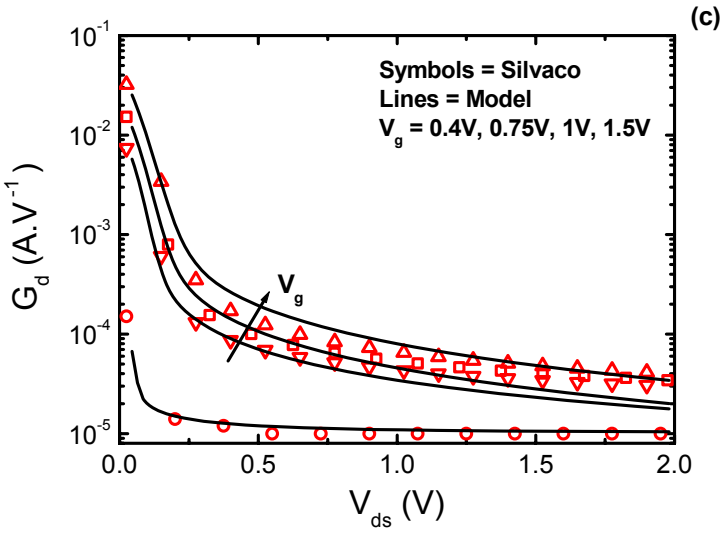
→ Determination of saturated length ΔL

[Lime'08] F. Lime et al., IEEE TED, vol. 55, no. 6, pp. 1441-1448, 2008.

2.3 Symmetrical Double-gate FETs



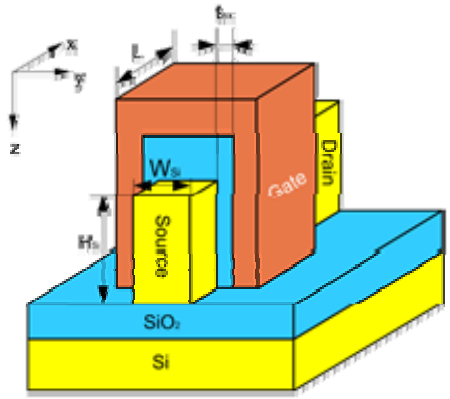
Saturation region length ΔL vs. drain current V_{DS} . ($V_{GS} - V_{TH}$ = 0.25 and 0.5V; L = 50nm)



Output conductance G_D vs. drain current V_{DS} . V_{GS} = 0.4, 0.75, 1, and 1.5 V; t_{ox} = 2nm, t_{Si} = 15 nm and L = 50 nm.

Modeling of the saturation for Symmetrical Double-gate FETs

2.4 FinFETs compact modelling



FinFET scheme

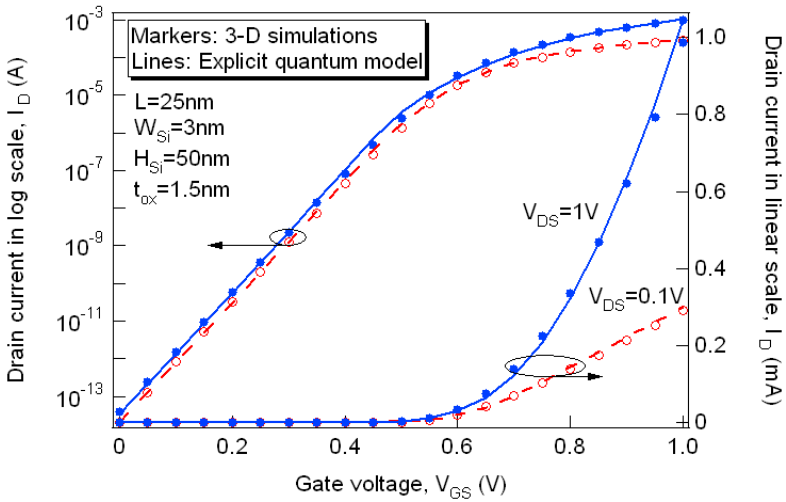
- Relationship between the charge density and the potentials [Sallese'05][Tang'09] :

$$v_g^* - v_{ch} - v_{to} = 4 \cdot q_g + \ln(q_g) + \ln[1 + \alpha \cdot q_g] \quad \text{with} \quad \alpha = \frac{C_{ox}}{C_{Si}}$$

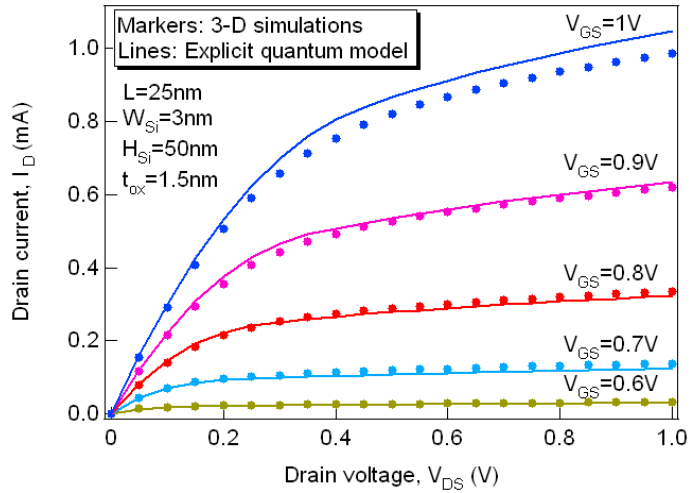
*This equation is solved by an explicit algorithm [Prégaldiny'06].

- Drain current expression:

$$i = -q_m^2 + 2 \cdot q_m + \frac{2}{\alpha} \cdot \ln\left(1 - \alpha \cdot \frac{q_m}{2}\right)\Bigg|_{q_{mS}}^{q_{mD}} \quad \text{with} \quad q_m = f\left(v_g^* - v_{to} - v_{ch}\right)$$



Comparison model/numerical simulations: drain current I_D vs. gate voltage V_G



Comparison model/numerical simulations: drain current I_D vs. drain voltage V_D

[Sallese'05] J. M. Sallese et al., *Solid State Electronics*, vol. 49, no. 3, pp. 485-489, 2005.
[Tang'09] M. Tang, F. Prégaldiny, C. Lallement and J.-M. Sallese, *IEEE TED,* vol. 56, no. 7, pp. 1543-1547, Jul. 2009.
[Prégaldiny'06] F. Prégaldiny et al., Int. J. Numer. Model: Elec. Network Dev. Fields, vol. 19, no. 3, pp. 239–256, May 2006.

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3. Conformal mapping
   - Application to Fully Depleted single-gate FETs: effect of the Drain through the BOX
   - Symmetrical Double-gate FETs
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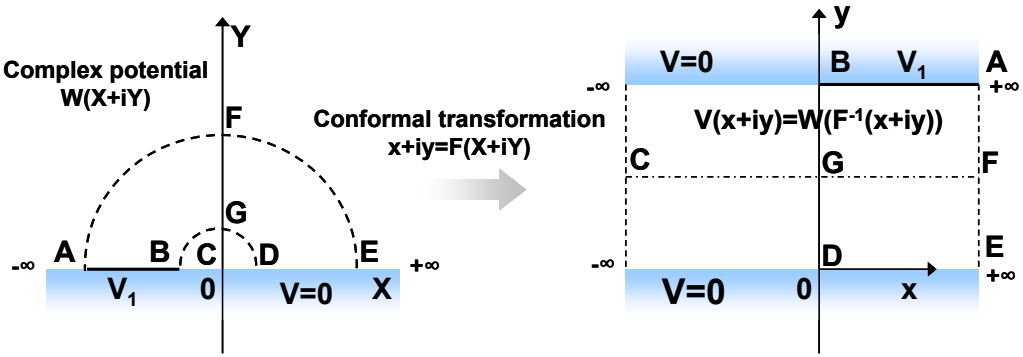
3.1 What is conformal mapping?

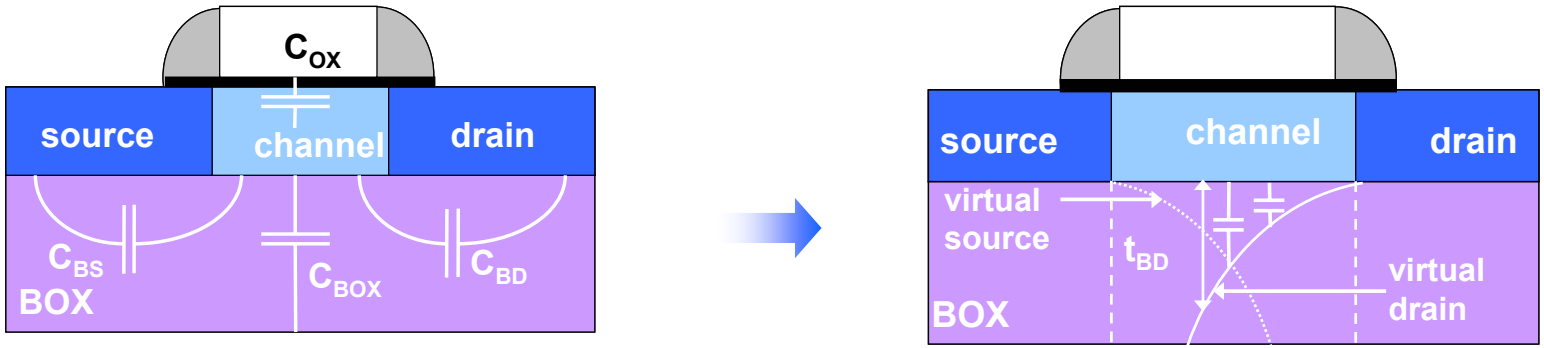
- Conformal transformation: transformation of an analytical function in a complex space:



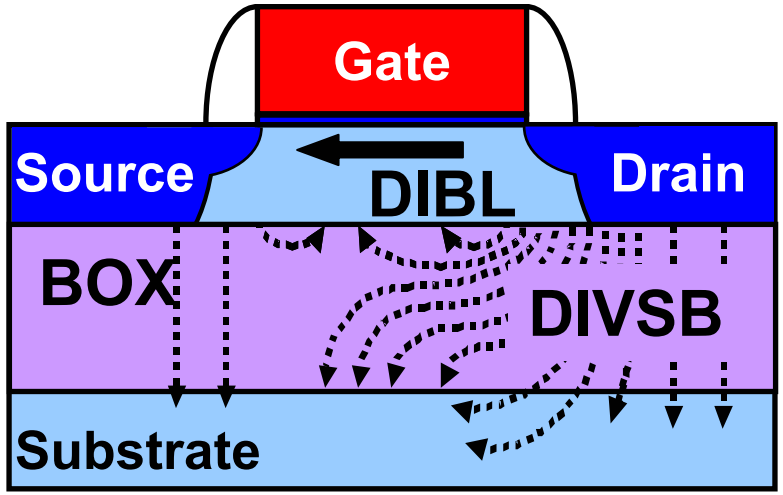
- Conservation of the Laplace's equation in the two spaces

→ Simplification of the geometry possible

- Application to FDSOI structures:



3.1 FDSOI: effect of the Drain through the BOX



✓ Penetration of the electric field from the drain into the BOX and the substrate

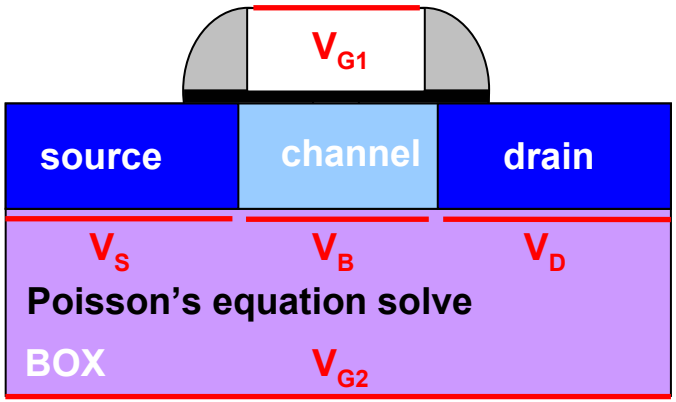
- electrostatic potential at the body-BOX interface modified
- because of coupling between back and front channels (Lim & Fossum model), front channel properties degraded

'*Drain Induced Virtual Substrate Biasing*' (DIVSB) effect [Ernst'99]

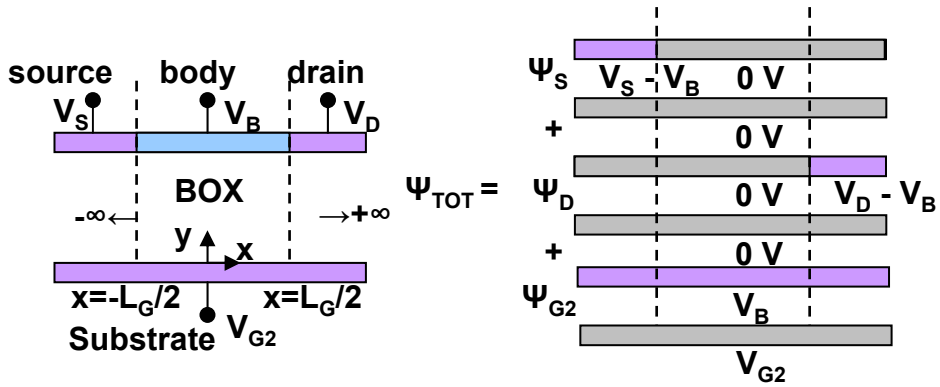
[Ernst'99] T. Ernst, S. Cristoloveanu, IEEE Int. SOI conf. 1999, pp. 38-39.

3.1 Conformal mapping in the BOX for FDSOI

- Bidimensionnal case: fully depleted transistor



Electrostatic problem to solve



Superposition theorem

- Superposition theorem:

$$\psi_{TOT}(x,y,V_S,V_D,V_B,V_{G2}) = \psi_{G2}(y,V_B,V_{G2}) + \psi_S(x,y,V_S,V_B) + \psi_D(x,y,V_D,V_B)$$

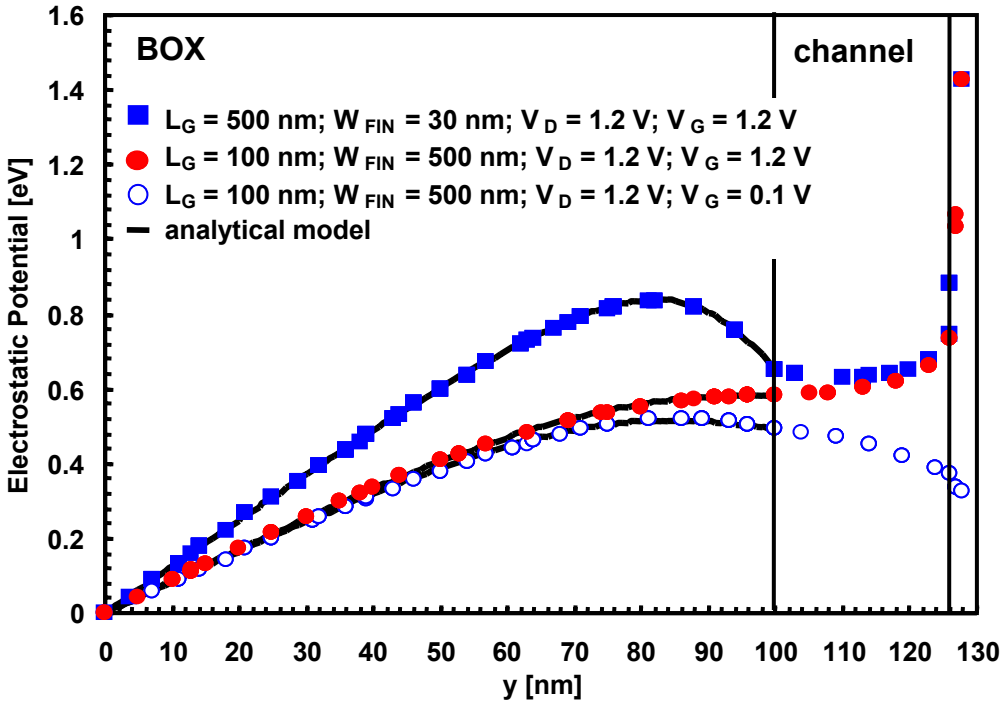
- With the analytical transformation:

$$\psi_D(x,y) = \mathrm{Re}\left\{\frac{V_D - V_B}{i\pi}\ln\left[1+\exp\left[\frac{\pi}{t_{BOX}}((x+iy)-\frac{L}{2})\right]\right]\right\} = \frac{V_D - V_B}{\pi}\arctan\left[\frac{\sin(\frac{\pi}{t_{BOX}}y)\exp(\frac{\pi}{t_{BOX}}(x-\frac{L}{2}))}{1+\cos(\frac{\pi}{t_{BOX}}y)\exp(\frac{\pi}{t_{BOX}}(x-\frac{L}{2}))}\right]$$

→ Electrostatic potential modelling in the BOX

3.1 Conformal mapping in the BOX for FDSOI

➢ Comparing with numerical simulations (using ISE/Synopsis) [Ernst'07]:



Comparison model / numerical simulations (ISE DESSIS)

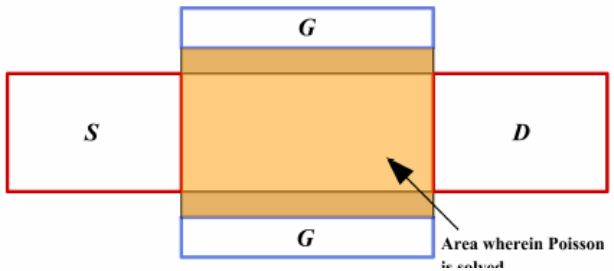
Exact modelling of the electrostatic potential

[Ernst'07] T. Ernst, R. Ritzenthaler, O. Faynot, and S. Cristoloveanu, *IEEE TED*, vol. 54, no. 6, pp. 1366-1375, Jul. 2009

3.2 Application to Symmetrical Double-gate FETs

COMON

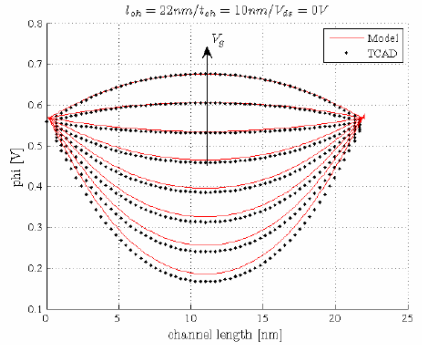
➢ In the subthreshold regime (resolution of 2D Laplace's equation) for Double-gate FETs [Børli'08] and Schottky Barriers DGFETs [Schwarz'09]:



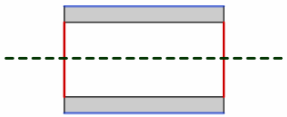
$$\varphi(u,v) = \frac{1}{\pi}\int_{-\infty}^{+\infty} \frac{v}{(u-\bar{u})^2+v^2}\varphi(\bar{u})d\bar{u}$$

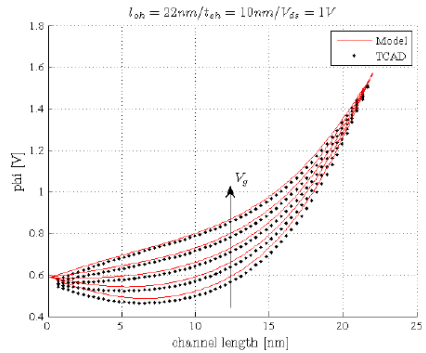
Scheme and core formula ('Poisson's integral')

- ✓ 2D closed form
- ✓ No fitting parameters
- ✓ Intrinsically compact expression
- ✓ Excellent agreement with numerical simulations

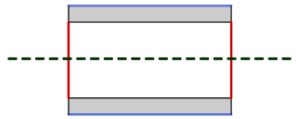


(a)





(b)



Potential in the channel obtained for a step of gate bias V_G with model (solid lines) and numerical simulations (points. Drain voltage V_D = 0 V (a) and 1 V (b). L_G = 22 nm, t_{Si} = 10 nm.

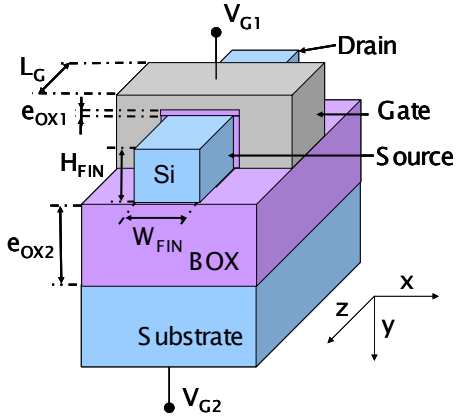
[Børli'08] H. Børli et al., IEEE TED, vol. 55, no. 10, oct. 2008.
[Schwarz'09] M. Schwarz et al., to appear in ISDRS'09 proceedings, Dec.. 2009

Outline

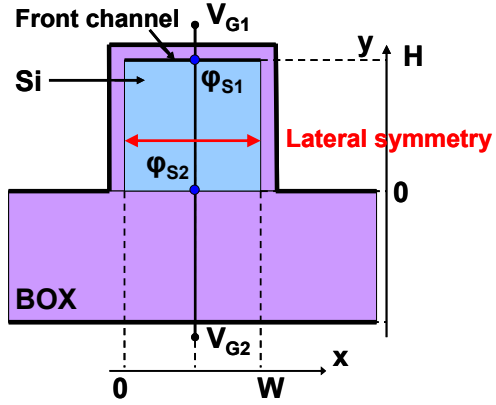
Presentation of the COMON project

1. Introduction
2. Charge based compact models
3. Conformal mapping
4. Fourier's series development
   - Triple-gate FETs 2D interface coupling
   - Π-gate FETs 2D interface coupling
5. Conclusions

4.1 Triple-gate FETs 2D interface coupling

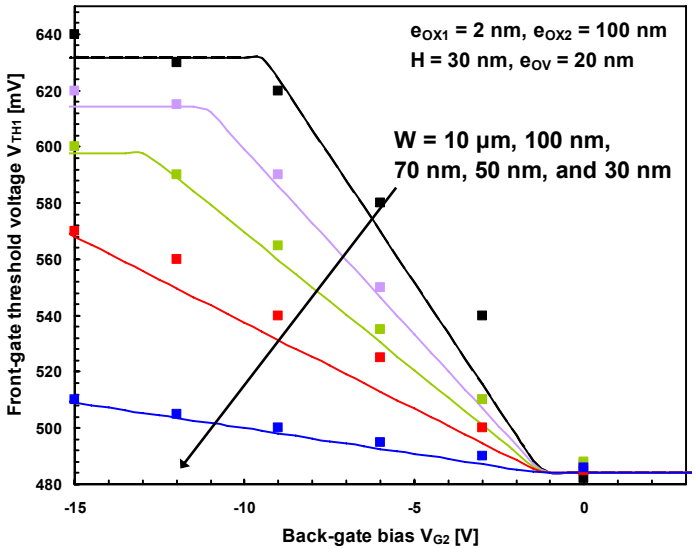


Triple-gate FET



Triple-gate FET, transversal cross-section

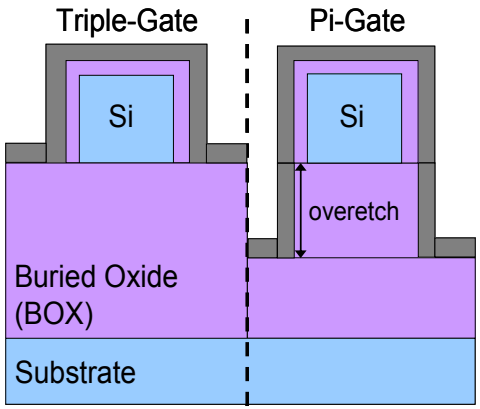
➢ Resolution of 2D Laplace's equation using series's development and Gauss's theorem at the interfaces:



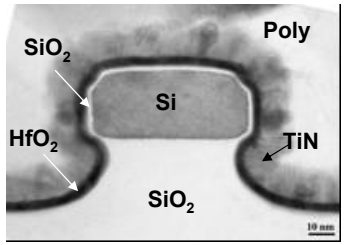
analytical (but not compact) modelling of the threshold voltage

Comparison front-gate threshold voltage V_{TH1} vs. back-gate bias V_{G2} with model (lines) and numerical simulations (squares)

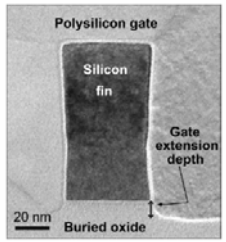
4.2 Π-gate FETs 2D interface coupling



Tranversal cross-section for Triple- and Pi-gate FETs

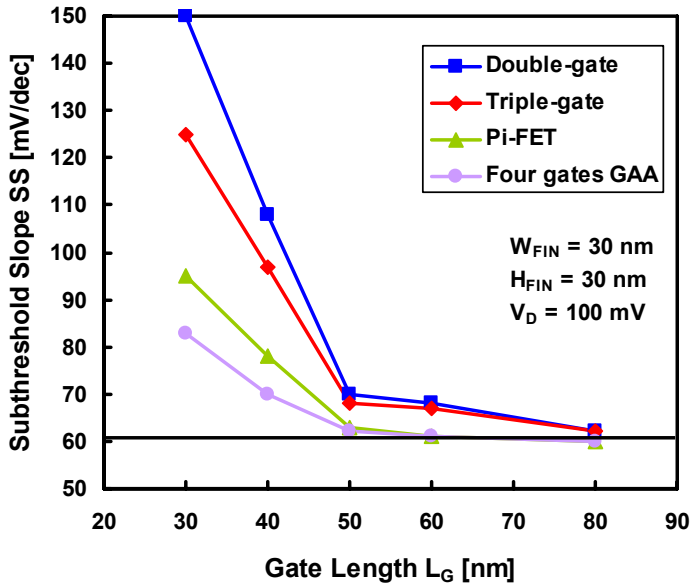


LETI [Jahan'05]



TI / Infineon [Frei'04]

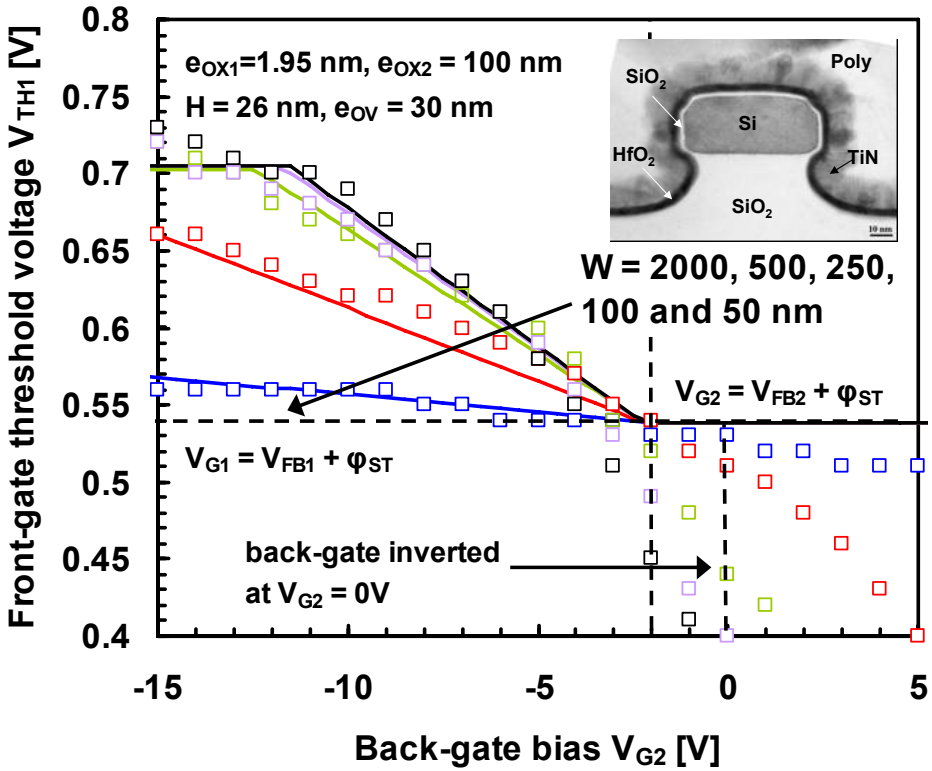
The process-induced gate overetch in the BOX is improving the device scalability



Subthreshold slope SS vs. gate length L_G for TG and Pi-FETs (from [Park'01])

[Jahan'05] C. Jahan et al., VLSI tech. dig., 2005.
[Frei'04] J. Frei et al., IEEE Electron Device Letters, vol. 25, no. 12, pp. 813-816, 2004.
[Park'01] J.-T. Park, J.-P. Colinge, C.H. Diaz, "Pi-Gate SOI MOSFET", IEEE Electron Device Letters, vol. 22, no. 8, pp. 405-406, 2001.

4.2 Π-gate FETs 2D interface coupling



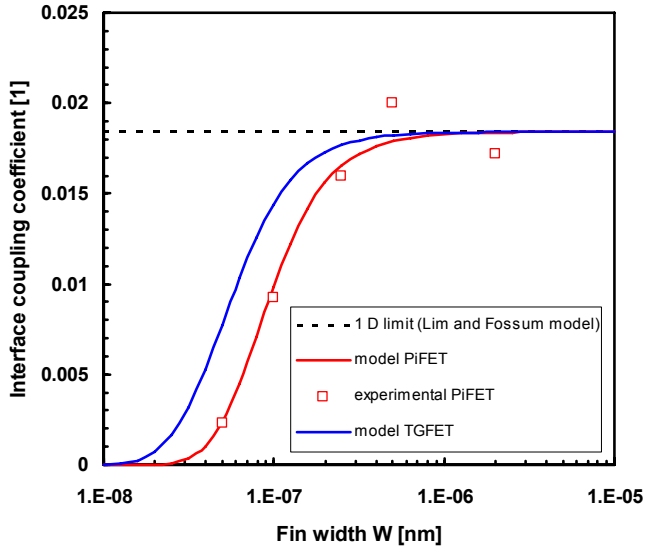
Comparison front-gate threshold voltage V_{TH1} vs. back-gate bias V_{G2} with model (lines) and experimental measurements (squares) [Ritzenthaler'09]

Perfect agreement analytical model/experimental measurements

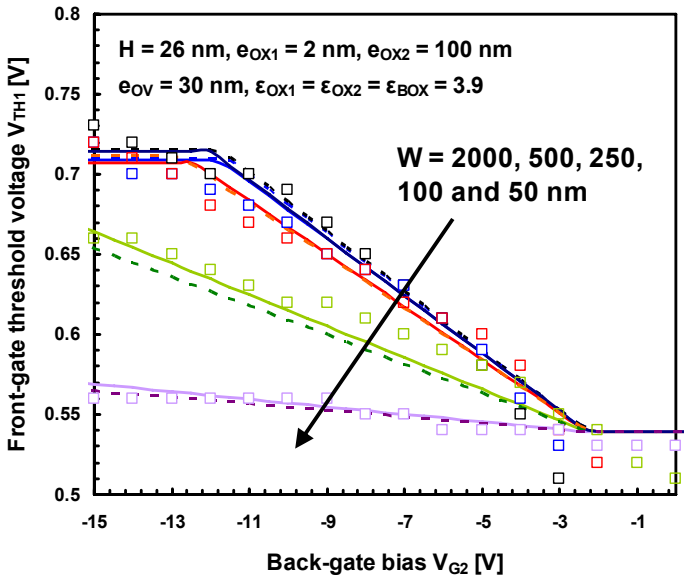
[Ritzenthaler'09] R. Ritzenthaler, O. Faynot, S. Cristoloveanu, and B. Iniguez, ISDRS conference proceedings, 2009.

4.2 Π-gate FETs 2D interface coupling

- Coupling coeff.: slope of $V_{TH1}(V_{G2})$ when the back-gate is depleted.
- Good agreement between experimental measurements and model.
- Triple-gate FETs are slightly more sensitive to back-gate influence than Pi-gate FETs.



Comparison coupling coefficient vs. gate width W using model (lines) and experimental measurements (squares)



Comparison front-gate threshold voltage V_{TH1} vs. back-gate bias V_{G2} with model (lines), compact model (dashed lines) and experimental measurements (squares)

compact model of the threshold voltage taking into account the effect of the overetch

Outline

Presentation of the COMON project

1. Introduction
2. Charge based compact models
3. Conformal mapping
4. Others techniques
5. Conclusions

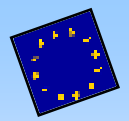
5. Conclusions

- Recent developments in compact/analytical modeling from COMON partners presented:

  - ✓ Compact charge based models in Multiple-Gate MOSFETs (DG MOSFETs, GAA MOSFETs, FinFETs):
    - A core model, developed from a unified charge control model obtained from the 1D Poisson's equation (using some approximations in the case of DG MOSFETs).
    - 2D or 3D scalable models of the short-channel effects (threshold voltage roll-off, DIBL, subthreshold swing degradation and channel length modulation), developed by solving the 2D or 3D Poisson's equation using appropriate techniques.

  - ✓ Conformal mapping technique presented, with applications to the case of fringing fields in FDSOI, and Schottky Barriers DGFETs.

  - ✓ Series´s development used to develop compact threshold voltage models for 2D interface coupling in Triple-gate and Pi-FETs architectures



Thank you for your attention!

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✓ URV Tarragona (Spain): Prof. B. Iñiguez, Dr. F. Lime, Dr. O. Moldovan, Dr. H. Abd El Hamid, Dr. B. Nae, G. Darbandy, M. Cheralathan.

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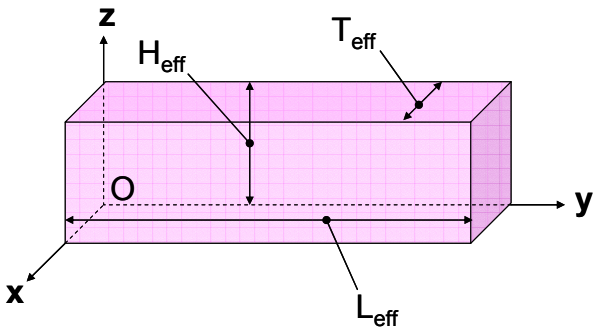
✓ Minatec Grenoble (France): Prof. Sorin Cristoloveanu

✓ Tyndall Cork (Ireland): Prof. J.-P. Colinge

Back-up slides

Triple-gate FETs short channel effects



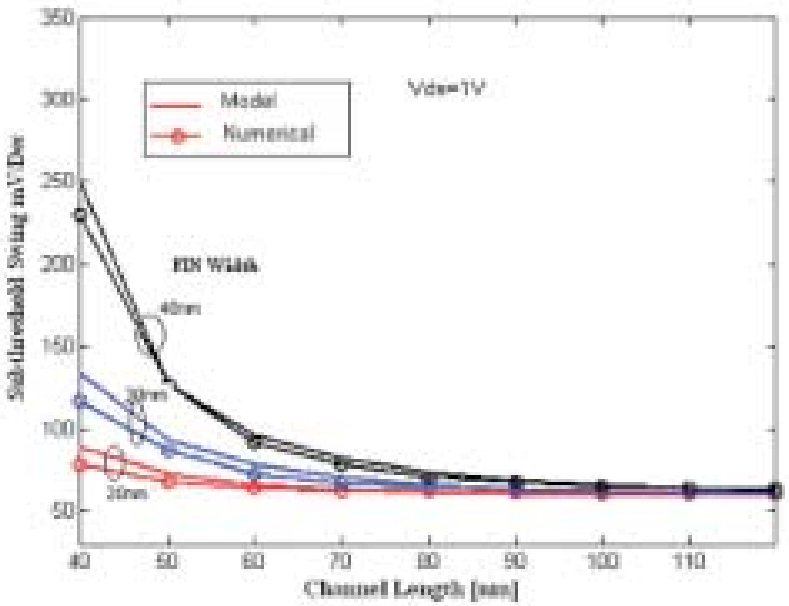
- Inclusion of SCEs [AbdElHamid'07-2]:

$$\varphi(x,y) = \varphi_1(y) + \varphi_2(x,y)$$

$\varphi_1(y)$ Solution of the 1D Poisson's equation

$\varphi_2(x,y)$ Solution of the remaining 3D equation

- Conduction path approach and virtual cathode position calculation.



Subthreshold slope SS vs. channel length L_G. Comparison between model (lines) and numerical simulations (markers)

[AbdElHamid'07-2] H. Abd El Hamid et al., IEEE TED, vol. 54, no. 9, pp. 2487-2493, 2007.