An Introduction to OLED/TFT Device Model and FPD Design Flow

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Outline

- LCD and OLED Flat Panel Display (FPD)
- TFT/OLED Devices and SPICE Modeling
- OLED FPD Design Flow
  - Circuit design entry
  - SPICE circuit simulation
  - Layout design
  - RC parasitic extraction
  - Design verification
  - IRdrop/EM analysis
- Future Work
LCD Pixel

- Liquid Crystal Display (LCD)
  - Liquid crystal molecule will rotate under external electric field
  - The electrical field for each liquid crystal is controlled by the TFT matrix for Active Matrix LCD (AMLCD)
  - Back light can be fully passed (white), fully blocked (black), or partially passed (grey)
  - Color light is created after the back light passed the color filter

![Diagram of LCD pixel]
OLED Pixel

- Organic Light-Emitting Diode (OLED)
  - A multi-layer structure between anode and cathode, including a few organic layers, such as Hole Transportation Layer (HTL), Electron Transportation Layer (ETL), and Emission Layer (EL).
  - When a voltage bias is applied to an OLED device, the holes from anode and the electrons from cathode will re-combine in EL and RGB lights will be emitted.
Flat Panel Display

- AMLCD

- AMOLED
OLED FPD Status

- Advantages
  - Light and thin: no backlight
  - Flexible display
  - Better view: true black, higher contrast ratio, higher response time, wider viewing angle, etc.
  - Wider temperature range
  - Low cost with simpler process

- Disadvantages
  - Higher price for large size display
  - Lifetime has been improved to meet the commercial requirements. However, blue light OLED has more severe aging effect.
  - In addition, it needs higher TFT driving capability: LTPS or IGZO
TFT Device

- Three major types of TFT
  - Amorphous Silicon TFT (a-Si)
  - Low Temperature Poly Silicon TFT (p-Si)
  - Oxide TFT (IGZO)

<table>
<thead>
<tr>
<th>TFT</th>
<th>a-Si</th>
<th>IGZO</th>
<th>p-Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobility (cm²/VS)</td>
<td>0.5 - 1</td>
<td>10 - 25</td>
<td>&gt;100</td>
</tr>
<tr>
<td>Uniformity</td>
<td>Good</td>
<td>Medium</td>
<td>Bad</td>
</tr>
</tbody>
</table>
TFT SPICE Modeling

- Data preparation for SPICE model generation
  - $I_{ds}$-$V_{gs}$@$V_{ds}$
  - $I_{ds}$-$V_{ds}$@$V_{gs}$
  - $C_{gs}$-$V_{gs}$
  - Target trend vs. W/L/T
## TFT Device Target

- **Device Target (or KOP, Key Output)**

<table>
<thead>
<tr>
<th>Target</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vth</td>
<td>$V_{gs}@I_{ds}=10\text{nA}*W/L$, $V_{ds}=0.1\text{V}$</td>
</tr>
<tr>
<td>SS</td>
<td>$I_{d1}=10\text{nA}*W/L$, $I_{d2}=1\text{nA}*W/L$, $V_{gs1}@I_{ds}=I_{d1}$, $V_{ds}=0.1\text{V}$, $V_{gs2}@I_{ds}=I_{d2}$, $V_{ds}=0.1\text{V}$, $SS=(V_{g1} - V_{g2}) / (\log I_{d1} – \log I_{d2})$</td>
</tr>
<tr>
<td>Ion</td>
<td>$I_{ds}@V_{gs}=30\text{V}$, $V_{ds}=40\text{V}$</td>
</tr>
<tr>
<td>Ion2</td>
<td>$I_{ds}@V_{gs}=30\text{V}$, $V_{ds}=0.1\text{V}$</td>
</tr>
<tr>
<td>Ioff</td>
<td>$I_{ds}@V_{gs}=-30\text{V}$, $V_{ds}=40\text{V}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>W</th>
<th>L</th>
<th>T</th>
<th>Vth</th>
<th>Ion</th>
<th>...</th>
</tr>
</thead>
<tbody>
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<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
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</table>
Point Model

Traditionally, GOA is separated from the TFT matrix.

- The mobility of A-Si TFT is too low for GOA. GOA is provided by an IC design company.
- As the number of TFT devices in a pixel cell is small, we can afford the luxury to develop point model: one SPICE model for one TFT device.
- The model extraction work is easy, accurate, and not a big task.

When LTPS TFT is introduced, the driving capability has been much improved. The integration of GOA with TFT matrix is becoming feasible.

- The benefits
  - Lower cost, smaller frame, more reliable

- The challenge
  - More model cards need to be developed with more geometries
  - A scalable model should be developed for multiple geometries
Global Model

- Two ways to develop a scalable model
  - Global model
  - Bin model

- Global model
  - Measure data for a group of devices with a combination of \( W \) and \( L \)
  - The best fitting for different devices could be conflicting to each other. Some trade-off has to be made.
  - The model equation is the foundation to develop a good global model
Bin Model

- Bin model
  - Divide the big W-L space into a few small bins, one model for one bin.
  - Measure device data for each grid point and extract its model parameters to fit one device.
  - For each bin, use the following “binning” equation, $P_{eff} = P_0 + \frac{L_P}{L_{eff}} + \frac{W_P}{W_{eff}} + \frac{P_P}{(L_{eff} \cdot W_{eff})}$, resolve the four unknowns ($P_0$, $L_P$, $W_P$, and $P_P$) with four equations from the four grid points.
  - For any device with any W/L geometry values, use the above “binning” equation to calculate $P_{eff}$ which is the model parameter for this device.
Process Variation

- Process variation
  - Device target variation caused by different machines, materials, process conditions, etc., in lot/glass/panel hierarchy
Corner Model

- Typical model (TT)
  - The mean value of measurement data is defined as the typical

- Corner Model (FF/SS)
  - The three sigma from the mean is defined as the upper and lower corners of the measurement data

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<th>Ion</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT</td>
<td>Mean</td>
<td>Mean</td>
</tr>
<tr>
<td>FF</td>
<td>Mean-3*Sigma</td>
<td>Mean+3*Sigma</td>
</tr>
<tr>
<td>SS</td>
<td>Mean+3*Sigma</td>
<td>Mean-3*Sigma</td>
</tr>
</tbody>
</table>

TFT.lib

```
.lib TT
.model TFT1 nmos +vt0=0.1  ute=1
....
..endl TT
.lib FF
.model TFT1 nmos +vt0=0.09  ute=1.1
....
..endl FF
.lib SS
.model TFT1 nmos +vt0=0.11  ute=0.9
....
..endl SS
```

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RPI TFT Model

- RPI TFT Models
  - Continuous expressions valid through all operating regimes
  - Gate-bias dependent field-effect mobility
  - Leakage current in deep subthreshold: grain boundary trap states and DIBL
  - Threshold voltage model that includes scaling with channel length and DIBL effect
  - Temperature dependence of model parameters
  - Kink effect caused by Vth decrease at high Vds
  - For both a-Si and poly-Si

- Where TFT model can be improved
  - Leakage current
  - Subthreshold region
  - Temperature model
  - Stress and hysteresis effects
Leakage Current

Three major mechanisms for TFT leakage current

① Front channel conduction: Conduction leakage current by accumulated negative carriers in front channel. Covered by RPI model.

② Back channel conduction: More negative gate voltage will decrease TFT band bending and the accumulated negative carriers at the front channel interface move to the back channel interface. They form the conduction leakage current in back channel

\[ I_{bc} \sim I_{BCF} \cdot \exp[f(V_{GS}, V_{DS})] \]

③ Front channel emission: Higher negative gate voltage will increase the emission of carriers from the trap states in the front channel interface by virtue of Poole-Frenkel effect, and will consequently increase the leakage current

\[ I_{fc} \sim I_{FCF} \cdot \exp(f(V_{DS})) \cdot \exp(f(V_{GS})) \]
Subthreshold Model

- Improve Vds dependency
  - Additional 2\textsuperscript{nd} order effect, the overall DIBL coefficient $\sim dibl0 + f(dibld, V_{DS})$
  - Additional bias-dependent subthreshold swing calculation $\sim e^{f(ss, V_{DS})}$
Temperature Dependency

- RPI TFT temperature model
  - Threshold voltage ($V_{th}$) $\sim$ linear function of DT
  - Saturation voltage ($V_{sat}$) $\sim$ linear function of DT
  - Activated leakage current ($I_{ol}$) $\sim \exp \left( \frac{1}{T} \right)$
  - Saturation velocity ($V_{max}$) $\sim$ linear function of DT

- Enhancement can be made
  - Nonlinear part can be added for the above components
  - Some new components can include temperature model, such as VFB, mobility, front channel leakage, back channel leakage, DIBL, etc.

T$=-15^\circ$C  T$=27^\circ$C  T$=60^\circ$C  T$=90^\circ$C
Stress Effect

- When TFT device operates under high gate voltage for a certain long period, some carriers in the device channel under the gate insulator layer will be trapped in the interface between the channel and the insulator layer. It will result in threshold voltage shift which causes device degradation.

\[ \Delta V_{th} \propto (V_{GS} - V_{th0} - V_{DS} \cdot \frac{V_{GS}}{V_{DS} + V_{GS}}) \cdot (1.0 - e^{-\frac{\text{time}}{\tau \beta}}) \]
Hysteresis Effect

- When the forward gate-voltage sweep applies on TFT device, as the $V_{GS}$ voltage continues to increase, the stress effect will take place as explained in the previous slide.

- Vice versa, when the device operates in the reverse gate-voltage sweep, $V_{GS}$ voltage gradually changes from ON-state to OFF-state, the carrier de-trapping process will give the threshold voltage chance to recover.

- As the speed of de-trapping is much slower than the speed of trapping, we will see the following Hysteresis effect.
Circuit Stress Simulation

- Vth shift after pulsed signal stress

2-periods | several periods | after long time

Input Signal

$V_{th}$ Shift

$V_{th}$ Shift
Circuit Stress Simulation

- Stress effect model used by compensation circuit design

Useless simulation if model has no hysteresis effect.

Very useful for compensation ckt design if model has hysteresis effect.

Current drop due to Vth increase.

Current mis-match.
OLED Structure

- **OLED layers**
  - EIL/HIL: electrons and hole injection layers
  - ETL/HTL: electrons and hole transport layers
  - HBL/EBL: hole and electron block layers
  - EL: emission layer

- **OLED operation mechanism**
  - Electrons and holes are injected from EIL/HIL
  - Electrons and holes accelerate in ETL/HTL
  - Minority hole and electron are blocked in HBL/EBL
  - Majority electrons/holes exciton formation and light generation in EL
OLED I-V Model

- \( J_{OLED, total} = J_{Break \ Down} + J_{Leakage} + J_{dio} + J_{2nd} \)
  
  - \( J_{dio} \propto f(\sum_{i=1}^{N-1} f(d_i, k_{oi}, J_{oi})) \cdot \left[ \exp\left(\frac{V_{OLED}}{n_{dio}v_t}\right) - 1.0 \right] \)
  
  - \( f(\sum_{i=1}^{N-1} f(d_i, k_{oi}, J_{oi})) \) is derived based on the following idea for N-layer OLED device
    - \( V_{OLED} = \sum_{i}^{N-1} \varepsilon_i \cdot d_i \)
    - \( J_{OLED} = J_1 = J_2 \cdots = J_i \cdots = J_{N-1} \)

- Summary: Simplified the complex OLED multi-layer physics to form an equivalent single-diode like equation.
OLED C-V Model

- A PWL (Piece-Wise Linear) model can be used to accurately model OLED C-V characteristics.
- More studies are needed to develop a more physics-based model for OLED with multiple organic layers.
OLED FPD Design Flow

Design Entry

Pixel/GOA SPICE Simulation

Pixel/GOA Layout Design

Pixel/GOA RC Extraction

Full Panel SPICE Simulation

Panel RC Extraction

Panel Layout Verification

Panel Layout Design

Full Panel Analysis IR Drop/Crosstalk/Leakage
Schematic Design Entry

- Most important feature
  - Approximate arbitrary shape of panel schematic, such as watch, automobile dash board, etc.
Layout Editor

- Most important features
  - Support arbitrary geometric shapes
  - Support advanced routing functions
    - Equal Resistive Routing (ERR)
    - Routing for a specified resistance value
    - Routing by Aperture in given area to assure enough light transmittance
  - Support narrow frame design

- Pixel placement near outline
- Ladder placement for GOA & DeMux
- Narrow frame fanout attaching to outline
Layout Verification

- Most important features
  - Avoid false DRC violations for arbitrary geometric shapes
  - Avoid wrong LVS netlist generation for arbitrary geometric shapes
- GOA rotation at round corner
False DRC Violation

- After rotation, the angles between “a” and “c”, and “a” and “e” may not equal to 90 degrees any more after the vertexes snapped to grid points. DRC may report “a - c” and “d – e” minimum space violation which is a false alarm.
Wrong LVS MOSFET Extraction

- After rotation, and after the vertexes snapped to grid points, MOSFET extraction could be wrong as the S-pin and D-pin may not touch the gate area.
RC Extraction

- Most important features
  - High accuracy, high performance, 3D RC extraction.
    - Pixel 3D RC extraction. High accuracy is required.
    - Metal mesh replaced metal solid piece for flexible touch panel. Thousands of grid points for 3D coupling capacitor extraction between the finger and the metal mesh.
OLED Full Panel Simulation

- OLED is a current driving device. FastSpice is not accurate for current simulation.

- Traditional SPICE is not able to handle the size of a full panel circuit. E.g., a 4K OLED TV has 3840*2160*8*3 (7T1C pixel) =200M TFT/OLED devices, plus 10x more parasitic RC elements.

- VDD/VSS IR drop and leakage current are the most critical concern for OLED FPD design. Full panel simulation is the only way to verify any issues in advance.
OLED Full Panel Simulation

- White: 96(1920/20) x 540(1080/2) (1/40)
- Red: 96(1920/20) x 1080 (1/20)
- Green: 192(1920/10) x 1080 (1/10)

A partial circuit may not be able to represent the full panel circuit. Full panel simulation considers IR drop, leakage, etc.
Full Panel IR Drop Analysis

- Must have for OLED FPD as high accuracy of OLED current is needed
- Simulates voltage distribution for power and ground nets in full panel
- Extract accurate but efficient resistive network
Future Work

SPICE Modeling

- OLED C-V model development
- OLED stress model development
- Statistical model generation with small sampling size

Circuit Simulation

- Hardware acceleration to speed up full panel simulation for 4K (200M TFT/OLED elements) and 8K (800M TFT/OLED elements) OLED
- Circuit stress simulation

Design Verification

- Handle arbitrary shapes more efficiently
Thank You!