



World-Wide Compact Model Standardization for an Expanding Industry

Si2 Compact Model Coalition

Peter M. Lee, Chairman

December 7, 2016

MOS-AK Workshop

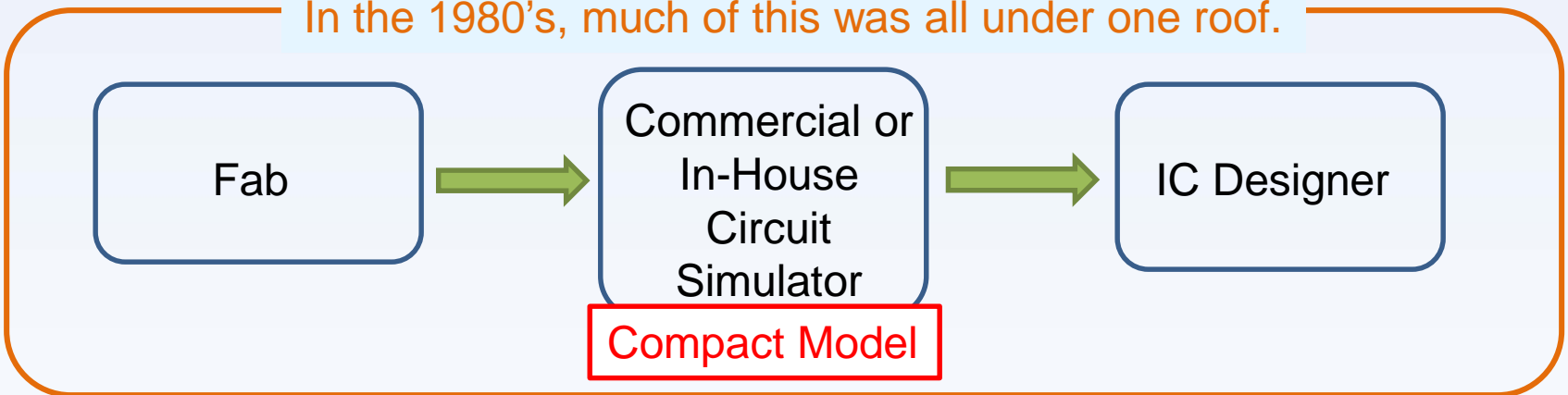
Outline

- The Birth of the CMC
- Operation, Members
- CMC Standards History and Works In Progress
- Membership Benefits
- Summary

The Birth of the CMC

- Compact models provide the vital connection to convey the detailed physical behavior of devices to circuit behavior.

In the 1980's, much of this was all under one roof.



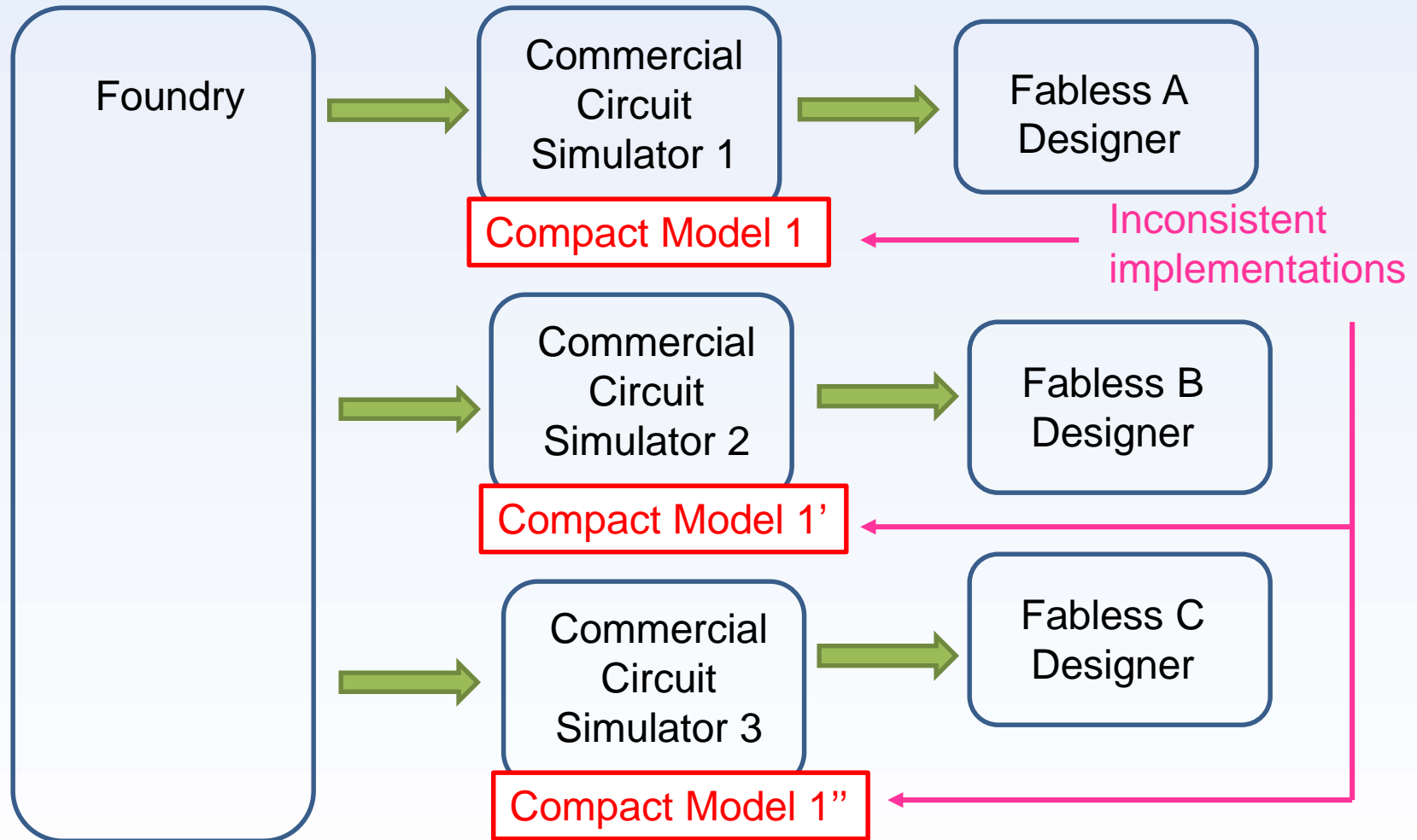
- This enables circuit designers to create the most optimum circuit taking into account the details of device physics.
- In the 1980's, the industry was dominated by IDMs with both the design and chip fabrication under one roof.
 - ❖ Many companies used in-house circuit simulators with some using in-house developed device models.

Changes in the 1990's



- The 1990's saw a transformation to where chip fabrication was being done at a foundry while design was being done by separate fabless companies.
 - ❖ This necessitated using EDA vendors and the device models implemented into the EDA vendor tools.
 - ❖ This caused issues concerning obtaining inconsistent results due to no standards across different vendor tools and the models implemented.
 - ❖ Foundries had to qualify their PDKs using different vendor tools to make sure that consistent results would be obtained.

Foundry/Fabless Model



- Multiple simulators with the “same” Model 1 but could result in different implementations (Model 1', Model 1'') which show inconsistencies in the results

The Need for Standardization

- To solve the inconsistencies which result from using different implementations of the same model into different vendor tools, a group of foundries, fabless design houses, IDMs, EDA vendors, and universities got together in 1995 to form the Compact Model Council (CMC)
- The main goals were to:
 - ❖ Create a standardization body to solve the model inconsistency issues
 - ❖ Create a system to fund model developers so that the models would always be up-to-date and serve the needs of the industry

CMC was born in Washington, D.C., on December 15, 1995

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Officers

Chair: Peter Lee (Micron)

Vice Chair: Josef Watts (GLOBALFOUNDRIES)

Secretary: Richard Williams (IBM)

Treasurer: Takeshi Naito (Toshiba)

Officers are elected to two-year terms by CMC member balloting.
Present officers are serving a 2016-2017 term.

Members in 2016

Analog Devices	ams	AWR/National Instruments	Broadcom	Cadence
Fujitsu Semiconductor	Global Foundries	IBM	Infineon	Intel
Keysight	Mentor Graphics	Micron	NXP	Oracle
Peregrine Semiconductor	ProPlus	Qualcomm	Raytheon	Renesas Electronics
Ricoh	Samsung	Sandia Labs	Silvaco	SK Hynix
Sony	ST Micro	Synopsys	TI	Toshiba
TSMC				

- Presently there are 31 member companies

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CMC Standards

Compact Models:

- Planar Bulk MOSFETs:

BSIM3 (1995)

BSIM4 (2000)

BSIM6 (2013)

PSP (2006)

HiSIM2 (2011)

HiSIM_HV (2007)

- LDMOS:

BSIMSOI (2002)

- SOI MOSFETs:

HiSIM-SOI (2012)

- BJTs:

MEXTRAM (2004)

HICUM (2004)

- Multi-Gate MOSFETs:

BSIM-CMG (2012)

BSIM-IMG (2015)

HiSIM-SOTB (2015)

- MOS Varactor:

MOSVAR (2006)

- Resistors:

R2_CMC (2005)

R3_CMC (2007)

- Junction Diodes:

DIODE_CMC (2009, 2016)

Other Standards:

- OMI Modeling API (2010)

- Standard SPICE Language (2012)

Verilog-A

Expected in 2016: GaN HEMT

Working Groups and Chairs



BSIM-Bulk	Kaiman Chan (TI)
BSIM-SOI	Saurabh Sirohi (GLOBALFOUNDRIES)
BSIM-CMG	Richard Williams (IBM)
BSIM-IMG	Josef Watts (GLOBALFOUNDRIES)
Diode Reverse Recovery	Klaus-Willi Pieper (Infineon)
GaN HEMT	Samuel Mertens (Cadence)
HICUM	Didier Celi (ST)
HiSIM2	Shigetaka Kumashiro (Renesas)
HiSIM-HV	Ehrenfried Seebacher (ams) & Takeshi Naito (Toshiba)
HiSIM-SOI	Marek Mierzwinski (Keysight)
HiSIM-SOTB	Marek Mierzwinski (Keysight)
MEXTRAM	Jin Tang (TI)
Model QA & Release	Shahriar Moinian (Avago)
MOSVAR	Geoffrey Coram (ADI)
PSP	Andries Scholten (NXP) & Gert-Jan Smit (NXP)
Standard Operating Point Variables	Samuel Mertens (Cadence)
OMI	Colin Shaw (Silvaco)

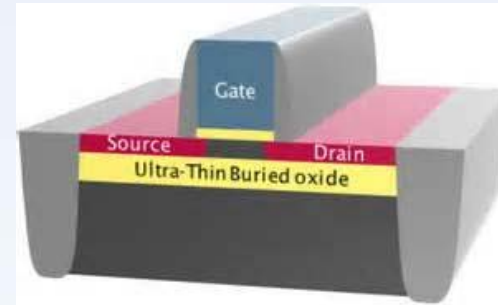
Currently 17 working groups

Recent New Standards

- Models for Fully-Depleted Silicon-on-Insulator (FDSOI) MOSFET Technologies

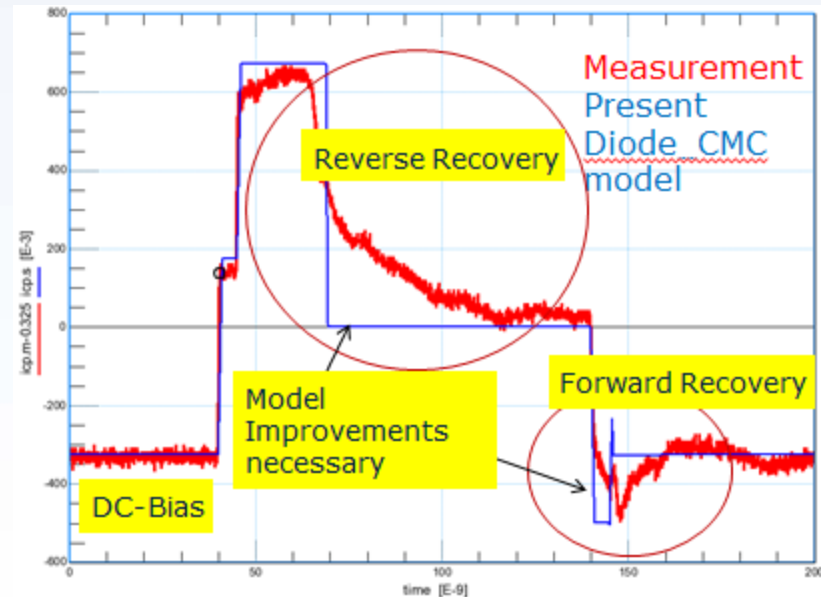
28nm → 10nm CMOS

- BSIM-IMG for the BSIM platform
- HiSIM-SOTB for the HiSIM platform



- Accurate forward and reverse recovery modeling in DIODE_CMC

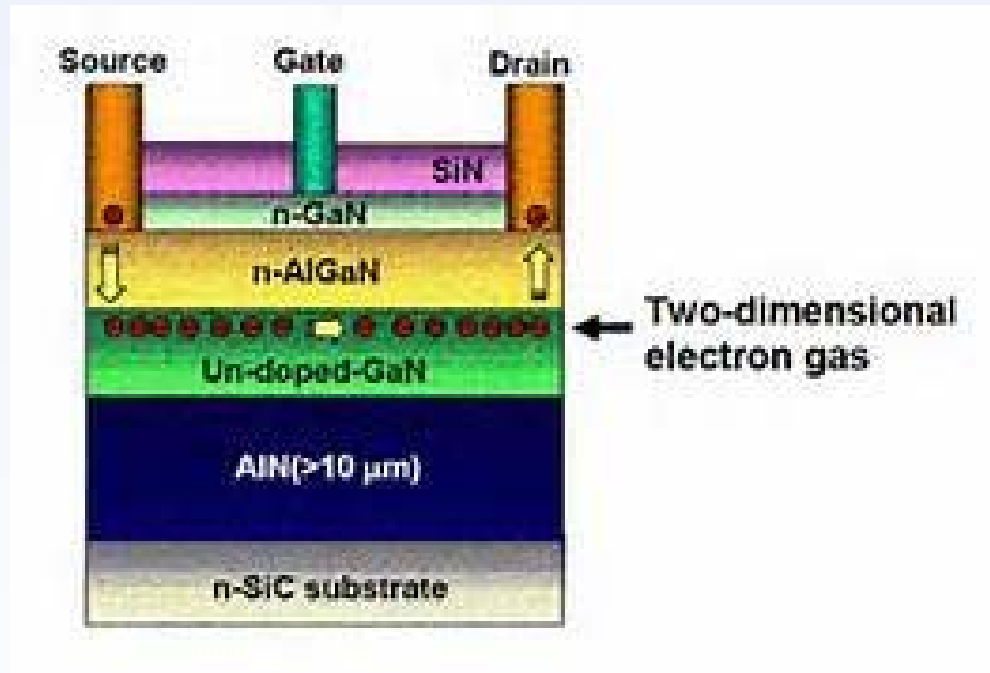
- Project 100% completed



2015-2016 Key Works In Progress

- GaN HEMT Model Standard

Power & RF



Current Status: Balloting for a GaN standard model has started this month to choose one or two standard models from two candidates. Decision will be made before the end of December.

External Collaboration

- **NEEDS Project:** Have started information exchange and studying how we can effectively collaborate to enhance model quality and development of the standard models.
- **Accellera SystemVerilog-AMS:** Information exchange to make sure we align on Verilog practices for standard model code. Currently we use the Verilog-AMS LRM Version 2.4.

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Member Benefits

- **Members have a say** in what models become a standard
- **Members** have the opportunity to request enhancements specific to their needs
- **Members attend** quarterly CMC meetings with leading industry and academic model developers, where they learn about technology, often before they are published in the literature
- **Members have access** to model beta code
- **Members have access** to functional assets such as the model implementation QA suite and API code
- All of the information from the meetings is available to **members only** on the CMC website

Asset Availability



Silicon Integration Initiative

General Standard Type	Model / API Documentation or Specification	Released Code and Other Ancillary Files
University-Developed Compact Model, e.g., BSIM6	On University Site with Link from Si2 CMC Site	On University Site with Link from Si2 CMC Site
CMC modified or Developed Compact Model, e.g., MOSVAR	On Si2 CMC Public Site	On Si2 CMC Public Site
Quality Assurance Program	Si2 CMC Private Site	Si2 CMC Private Site
Test Suite for Verilog-A Compliance	Si2 CMC Private Site	Si2 CMC Private Site
Application Programming Interfaces	Si2 CMC Public Site	Si2 CMC Private Site
Standard Netlist and File Format	Si2 CMC Public Site	Si2 CMC Public Site

Research Institution Partners



- **University of California at Berkeley – Professor Chenming Hu**
 - ❖ BSIM3, BSIM4, BSIM6, BSIM-SOI, BSIM-IMG and BSIM-CMG
- **Hiroshima University – Professor Mitiko Miura-Mattausch**
 - ❖ HiSIM2, HiSIM_HV, HiSIM-SOI and HiSIM-SOTB
- **University of California at San Diego – Professor Michael Schroter**
 - ❖ HICUM
- **Auburn University – Professor Guofu Niu**
 - ❖ MEXTRAM
- **CEA-Leti – Dr. Jean-Charles Barbé**
 - ❖ PSP

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- The CMC enhances the IC development process
 - ❖ Standardizing high-quality device models and simulator interfaces
 - ❖ Providing a forum and mechanism to keep these standards current to expanding industry needs
- The CMC is a member-driven organization open to any company in the semiconductor business

http://projects.si2.org/cmc_index.php