Gate Resistance Measurement and Modeling for 3D FETs

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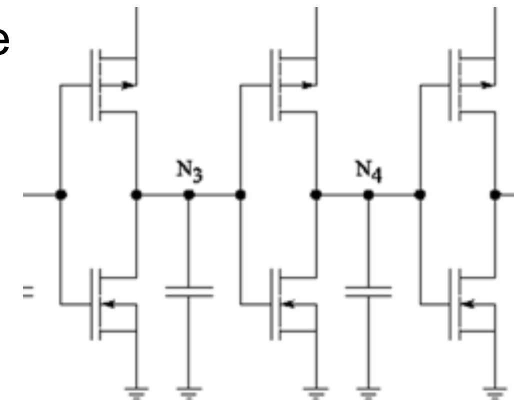
Outline

- Who cares about gate resistance
- Gate Resistance and Capacitance in 3D FETs
- Small Signal Analysis
- Rgate from S-parameters
- Rgate for Modeling
- Conclusions

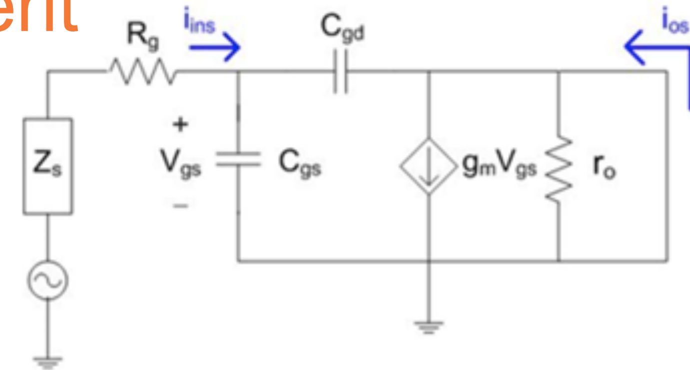
Rgate and logic delay

- Rgate adds delays to the slewing of the gate
  - $\tau_{Rg} = R_g C_{gg}$
  - Important if τ is a significant fraction of rise/fall time
- In Cmos logic 1 FET drive at least 2 gates
  - Plus some wiring
  - For fanout > 1 add more pairs of gates
  - Fanout of 3 is a typical metric



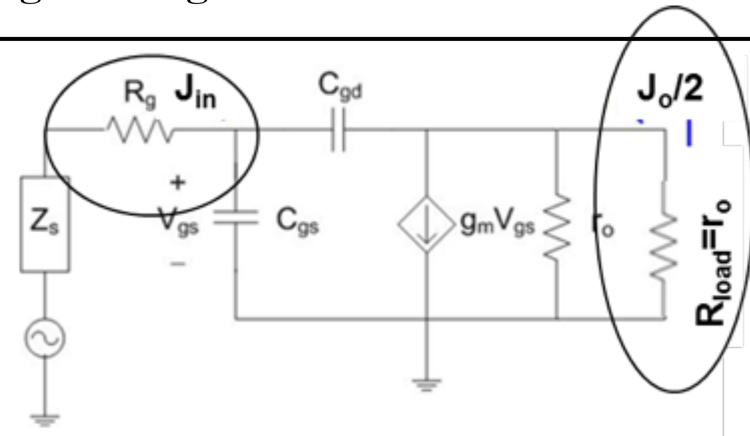
- In a fanout 3 inverter ring oscillator 1 transistor drive 6 gates
  - $\tau_L \approx 6 C_{gg} V_{dd} / g_m (V_{dd} - V_t)$
  - Rgate can be important if it is high enough

RF performance figures of merit



- $f{\downarrow}T$: The frequency at which a FET has unity **current** gain
  - Rgate does not effect current gain

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\left[1 + g_m(R_S + R_D)\right]\right)}$$



- $f{\downarrow}MAX$: The frequency at which a FET has unity **power** gain
  - Rgate Increases the input power for a given output.
  - ∴ Decreases Fmax

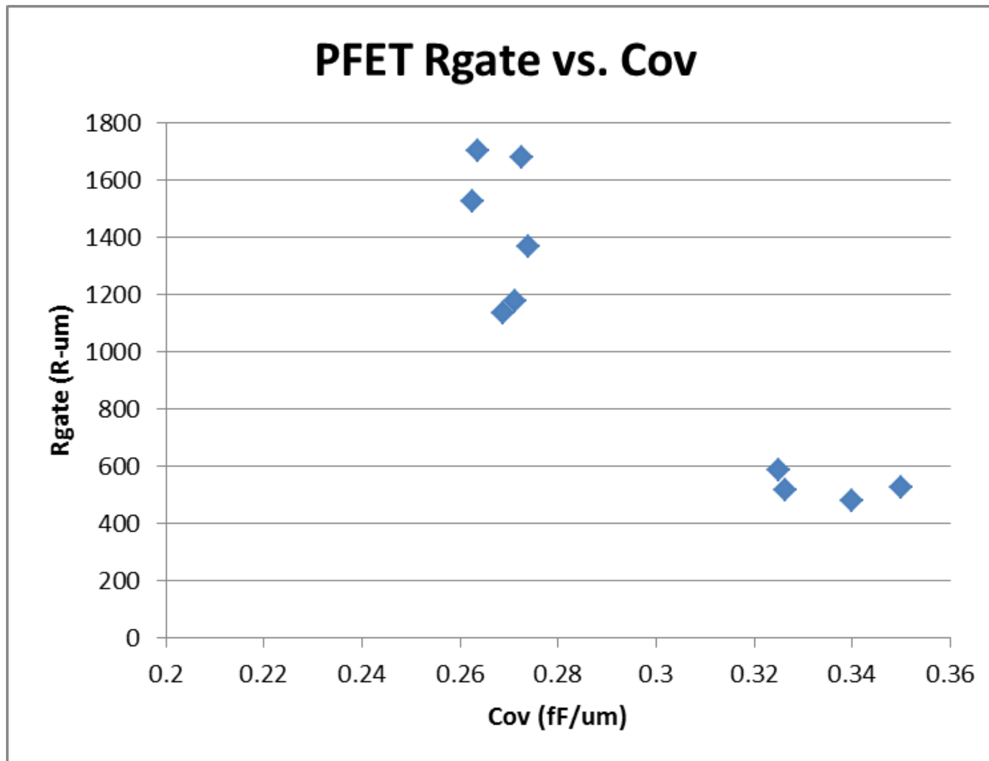
$$f_{MAX} = \frac{1}{2}\frac{f_T}{\sqrt{\frac{g_m}{(C_{gs} + C_{gd})}C_{gd}(R_g + R_s) + \frac{R_g + R_s}{r_o}}}$$

Logic vs RF sensitivity to Rgate

- RF is more demanding of low Rgate because the slew rates are higher
- Logic: $\tau_L \approx 6 C_{gg} V_{dd} / g_m (V_{dd} - V_t)$

- RF
  - $\tau_{ft} \approx C_{gg} / g_m$
  - RF is at 5-10 times as sensitive as Logic to Rgate
  - RF devices are typically wider, increasing Rgate

Gate Resistance and Capacitance in 3D FET
A surprise result



- A process change significantly increased PFET Cov—expected
- PFET Rgate dropped
  - Rg=Re[1/Y11]
- Physically Rgate should not change
- NFET Rgate did not change (same physical structure, no change to NFET Cov)

Rgate & Cgg in 3D FETs
Schematic Structure of a finFET

Region of intrinsic capacitance

gate

source

drain

W

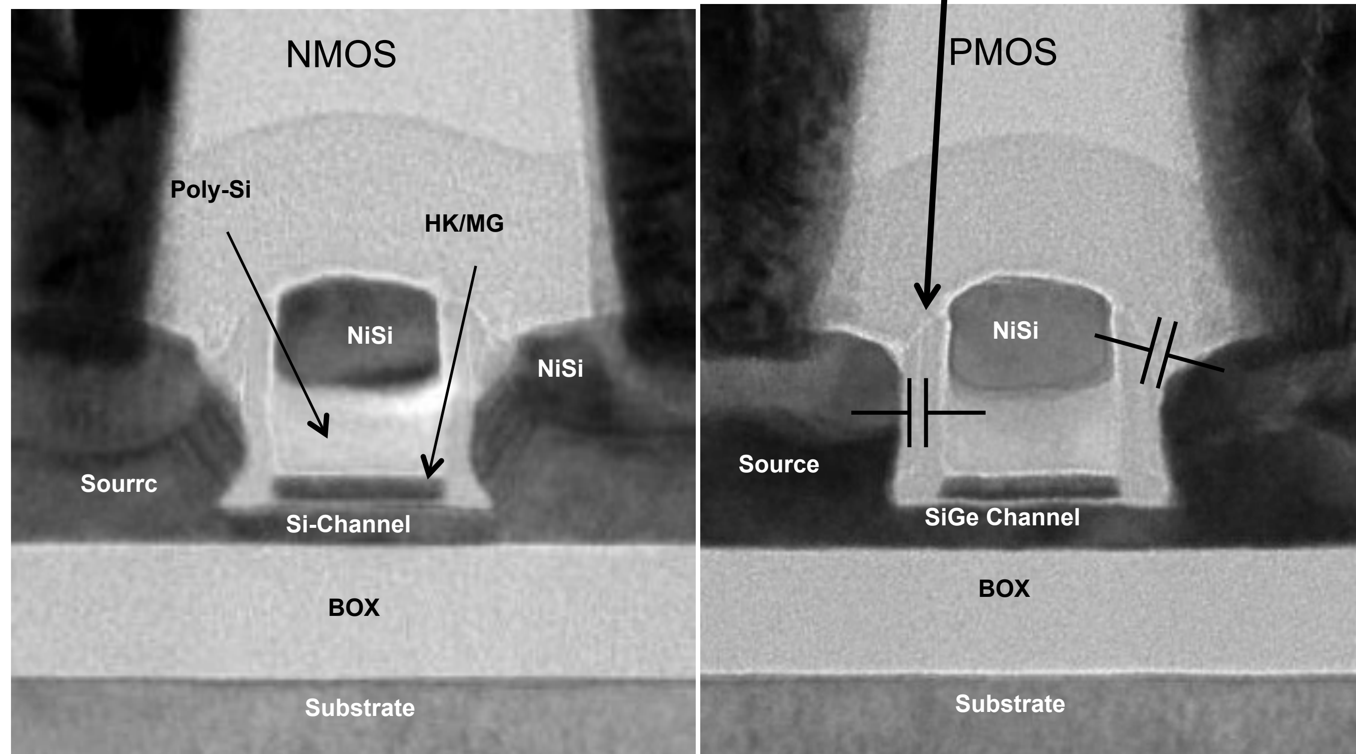
Gate Current

Extrinsic Cgs

Resistance at the work function metal interface and Intrinsic Cgs

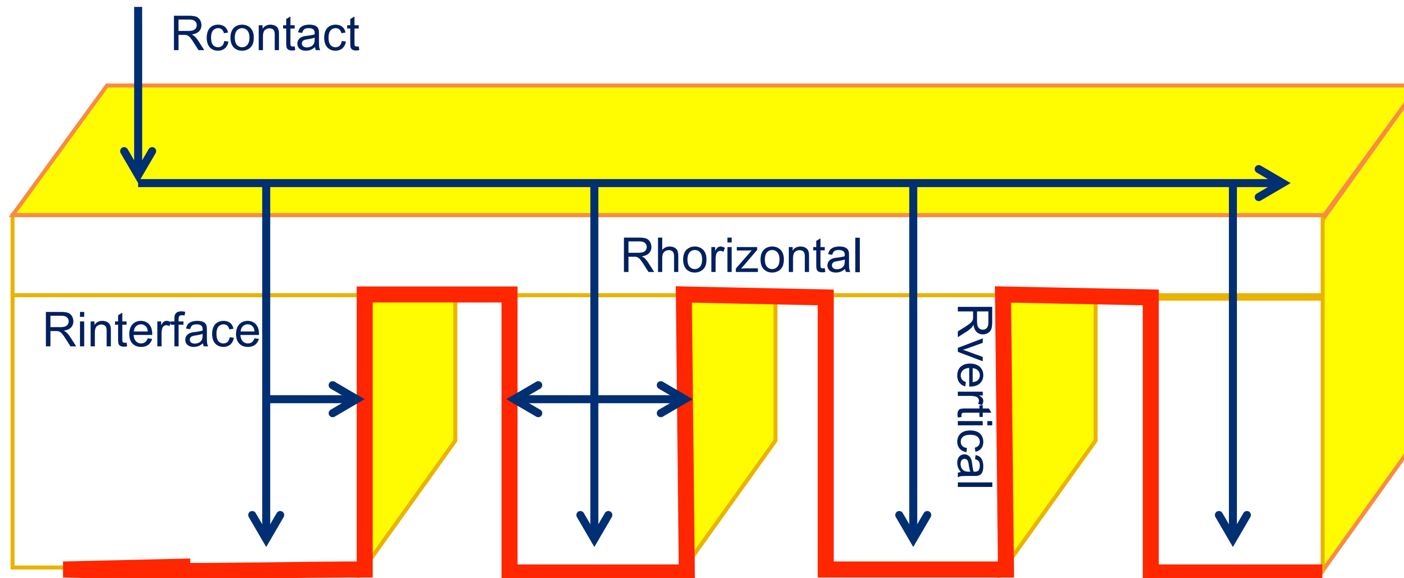
FDSOI with Raised Source Drains

- Large capacitance above the work function metal



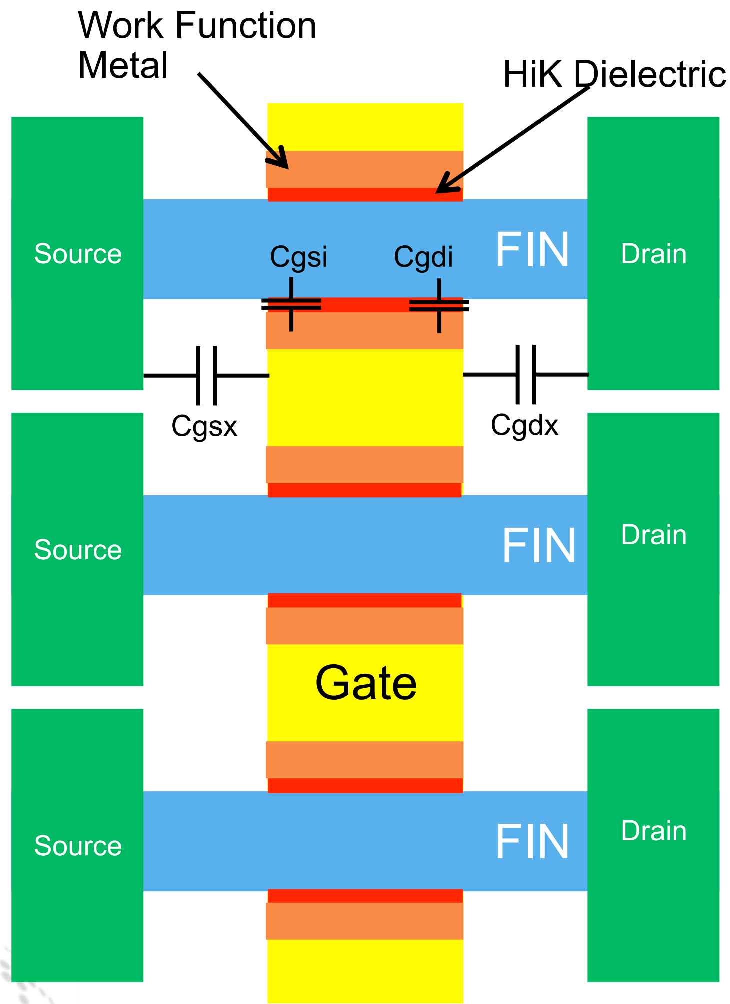
Normalized Gate Resistance Scaling

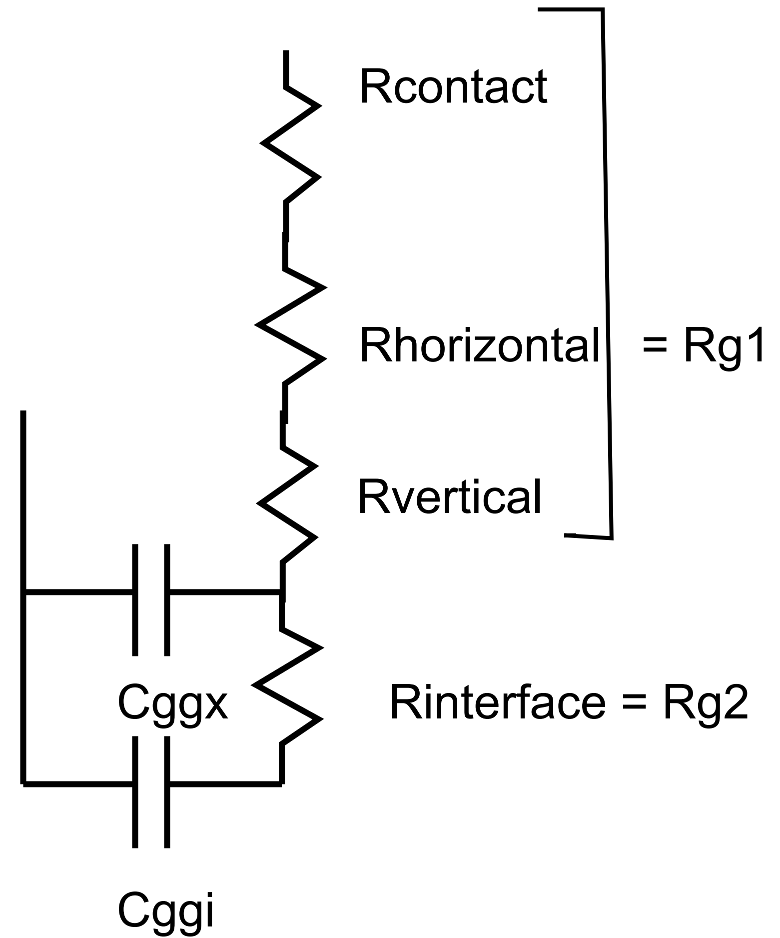
Rgate is normalized as Rg*Nfin*Wfin so that Rg*Cgg is W independent



- Normalized Rcontact scales as W
- Normalized Rhorizontal scales as W^2
- Normalized Rvertical and Rinterface do not scale with W

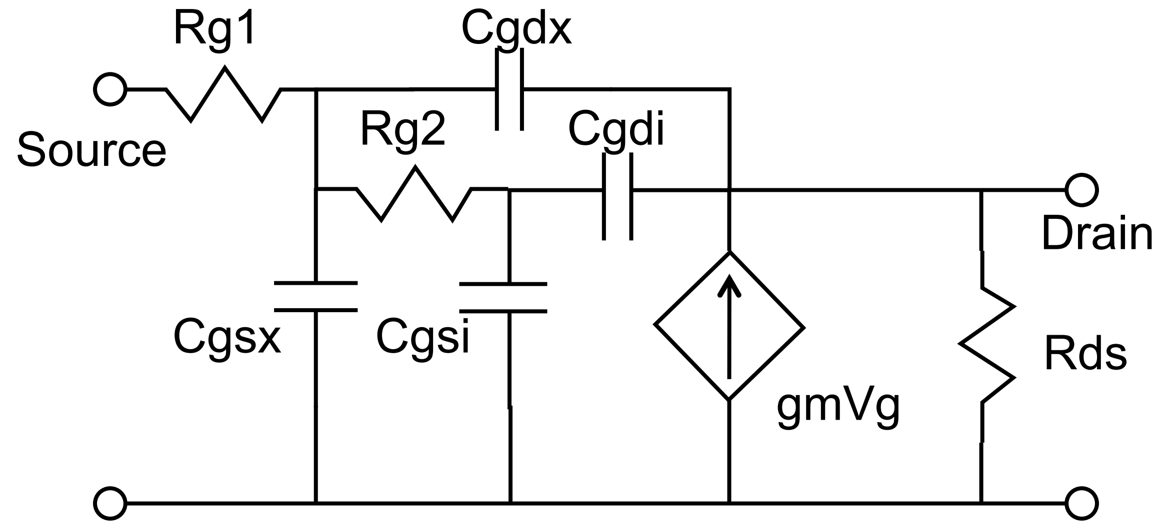
Top view, Crossection through fin



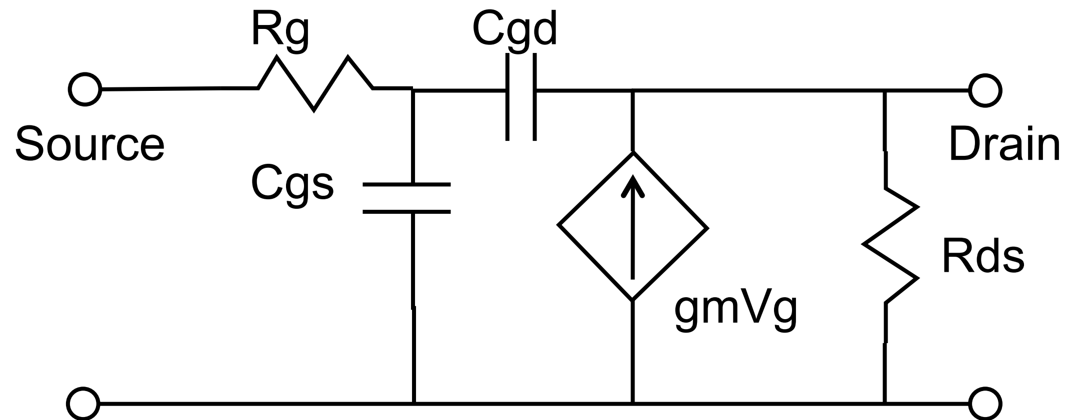


3-D FET small signal model

Approximate the distributed RC by a Pi-network



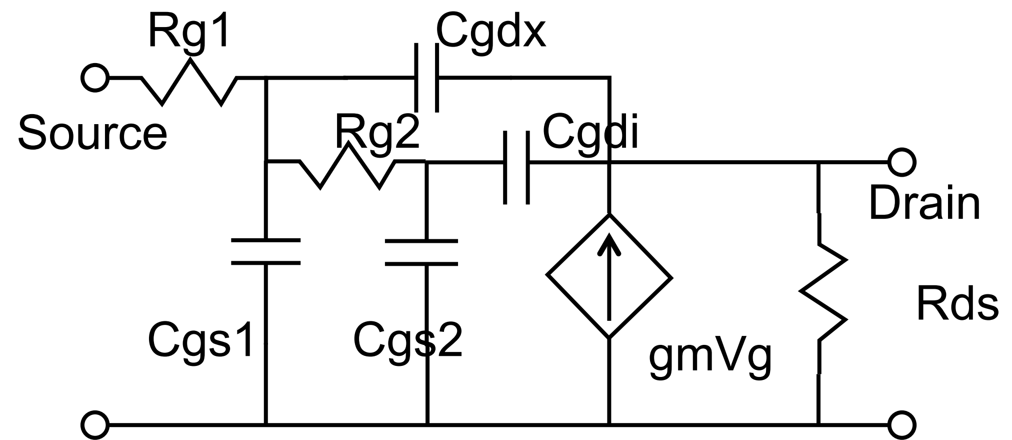
Looking for the equivalent Rg for the standard topology



Common definitions of Rg for measurement

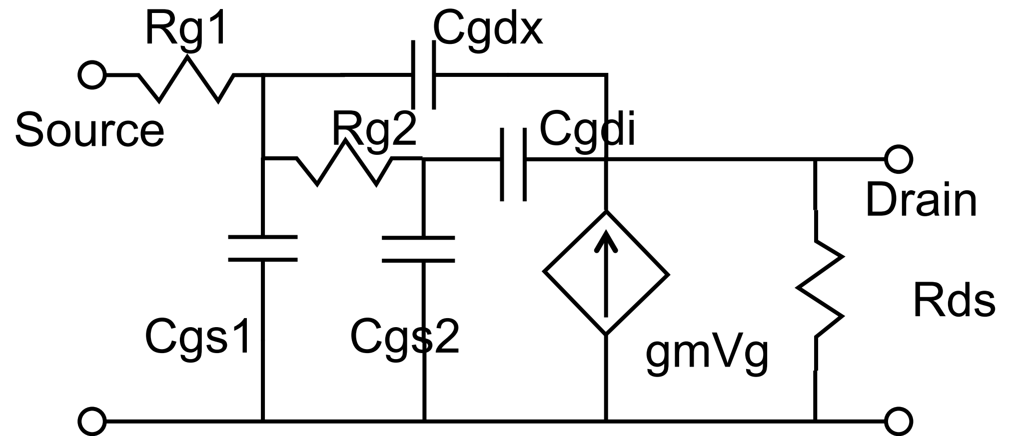
- Rg = Re[1/Y11] : Real part of the impedance "looking into the gate"
- Rg = Re[Y12]/(Im[Y11]*Im[Y12] : "looking into the drain"
- $Y11 = I_1 / V_1$ with $V_2 = 0$
- $Y12 = I_1 / V_2$ with $V_1 = 0$
- Use the fact that $R_g \ll 1/\omega C_{gg}$
- Because Rg is so small the effective gate capacitance is unchanged by the resistor network:
- $C_{gg} = (C_{ggi} + C_{ggx})$; $C_{gd} = (C_{gdi} + C_{gdx})$; $C_{gs} = (C_{gsi} + C_{gsx})$

3-D Gate Resistance



- $Y11 = \omega^2 C_{ggi} (C_{ggx} R_{g1} + C_{ggi} R_{g2}) + j\omega C_{gg}$
- $Y12 = \omega^2 (C_{gd} C_{gg} R_{g1} + C_{gd2} C_{gg2} R_{g2}) + j\omega C_{gd}$
- $R_g = Re[1/Y11] = R_{g1} + R_{g2} (C_{ggi} / (C_{ggx} + C_{ggi}))^2$
- $R_g' = Re[Y12]/Im[Y12] Im[Y11] = R_{g1} + R_{g2} C_{gdi} C_{ggi} / ((C_{gdi} + C_{gdx})(C_{ggi} + C_{ggx}))$
- Re[Y12]/Im[Y12] > Re[Y11]/Im[Y11] therefore Rg' gives a better measurement
- Rg (looking into gate) is always > Rg' looking into drain
- Typical data for our PFET shows Rg/Rg' ~ 1.5-2.0

Modeling the 3-D gate resistance



- Adding the extra node gives physically correct model for Rgate looking into both gate and the drain.
- Rgate is most important for its impact on input power
- Output power is determined by Rds and output circuit impedance
- For operation in common source circuits can drop the extra node with little impact on accuracy
- Gate resistor should be the resistor given by Re[1/Y11]
- In practice we tune resistor to match power gain (f_{MAX})

Conclusions:

- 3-D gate makes measured Rgate a function of the distribution of capacitances between extrinsic and intrinsic regions
- Rgate looking into gate and looking into drain are different
- Can simulation with a single effective Rgate
- Rgate looking into drain gives a more repeatable measurement
- Rgate looking into the gate give correct power simulation