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PHILIPS

Compact Modelling of LDMOS Devices

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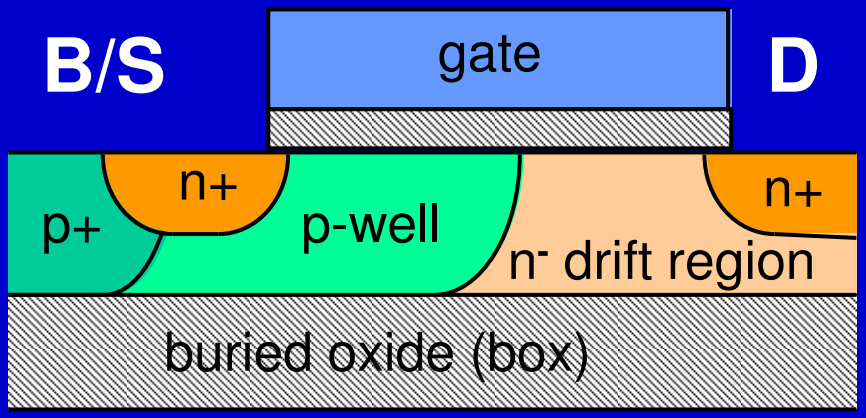
introduction: LDMOS devices

Low-voltage



introduction: LDMOS devices

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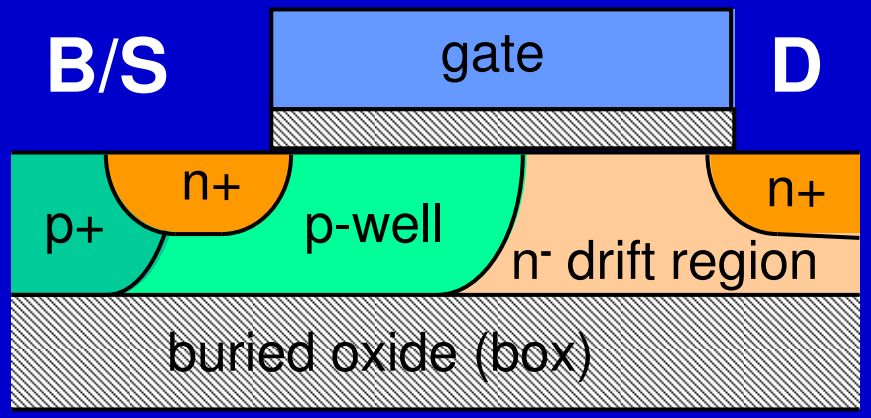
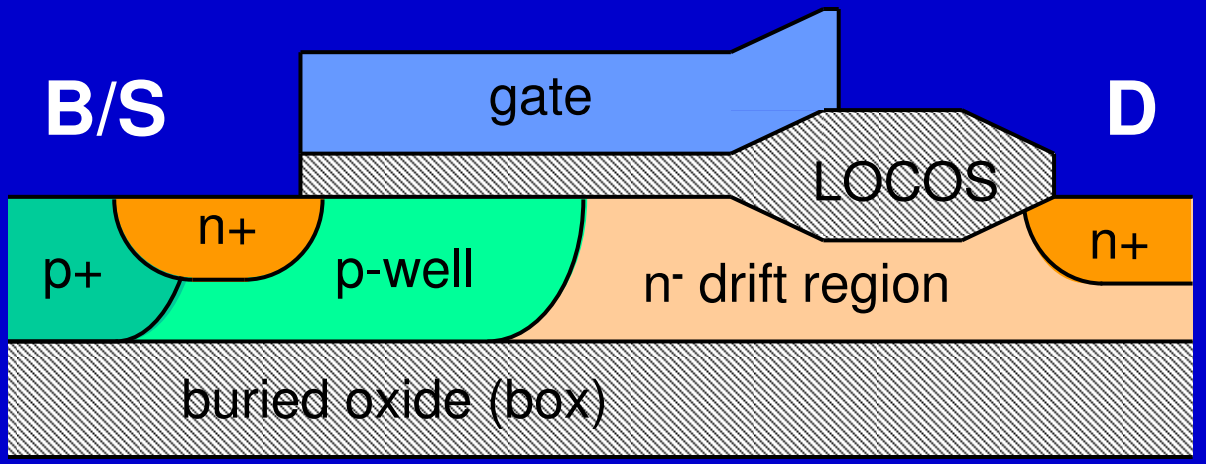


High-voltage



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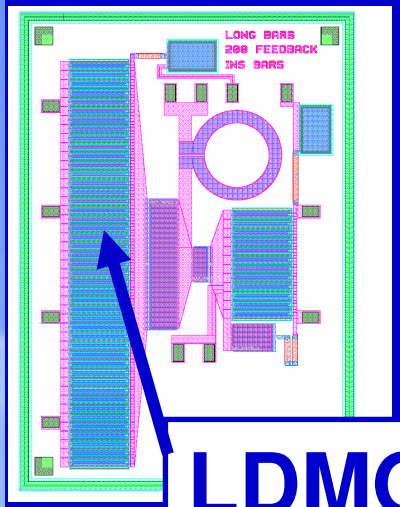
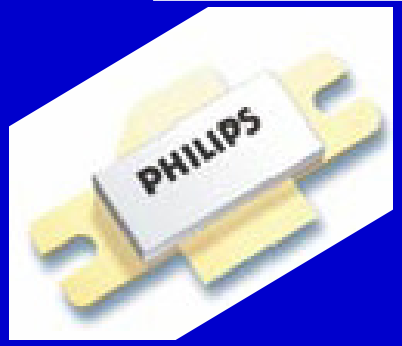
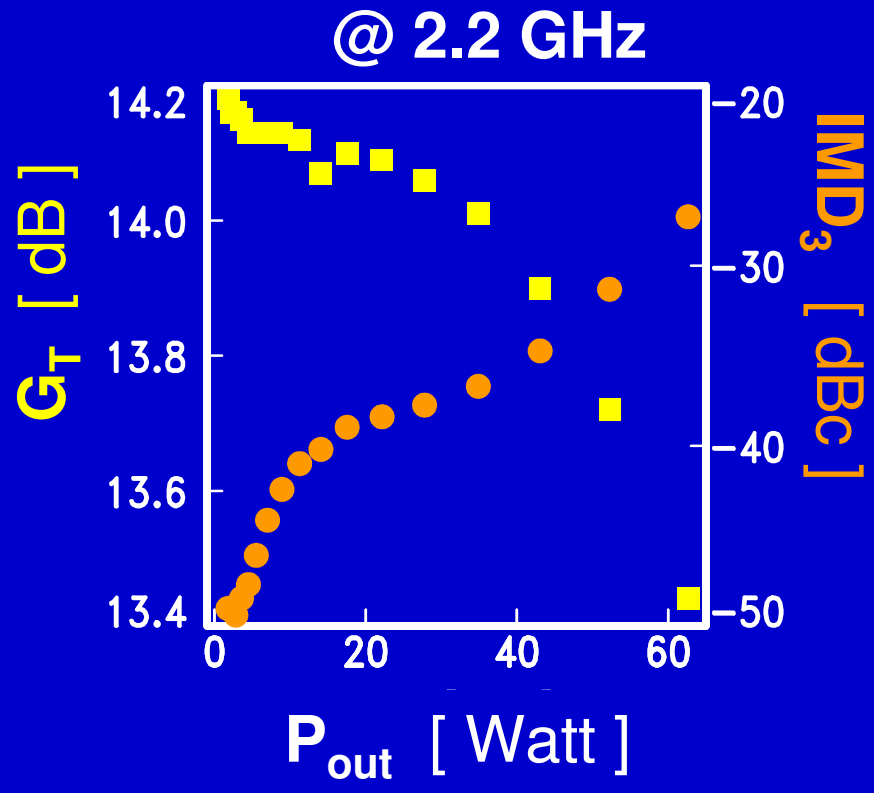


LDMOS

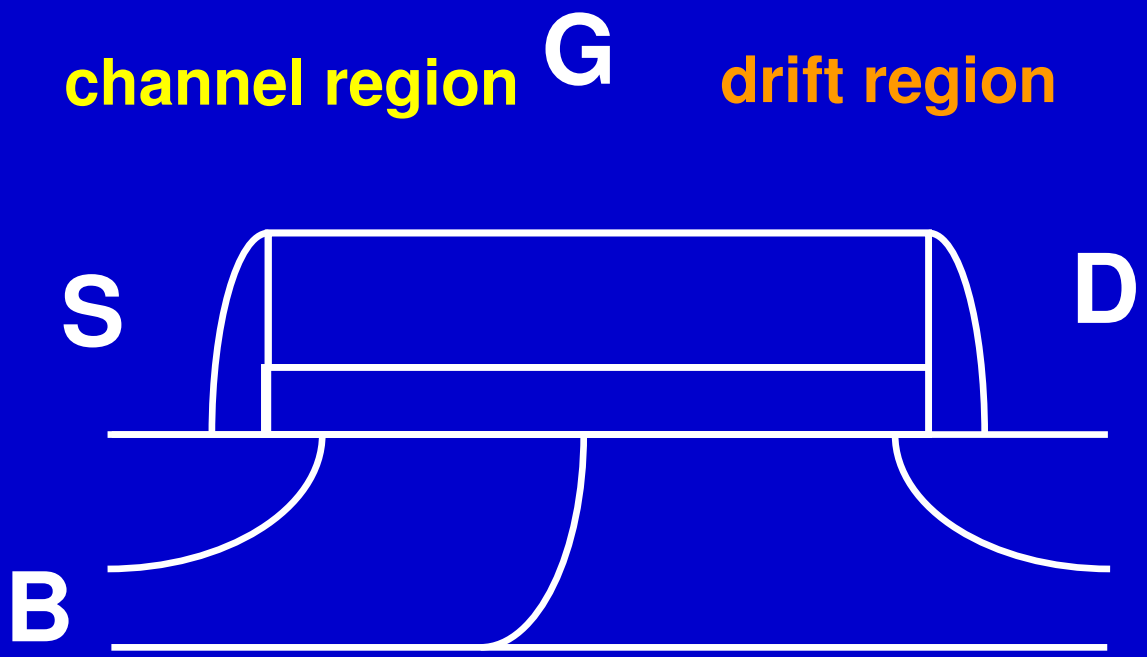


RF-power amplifiers

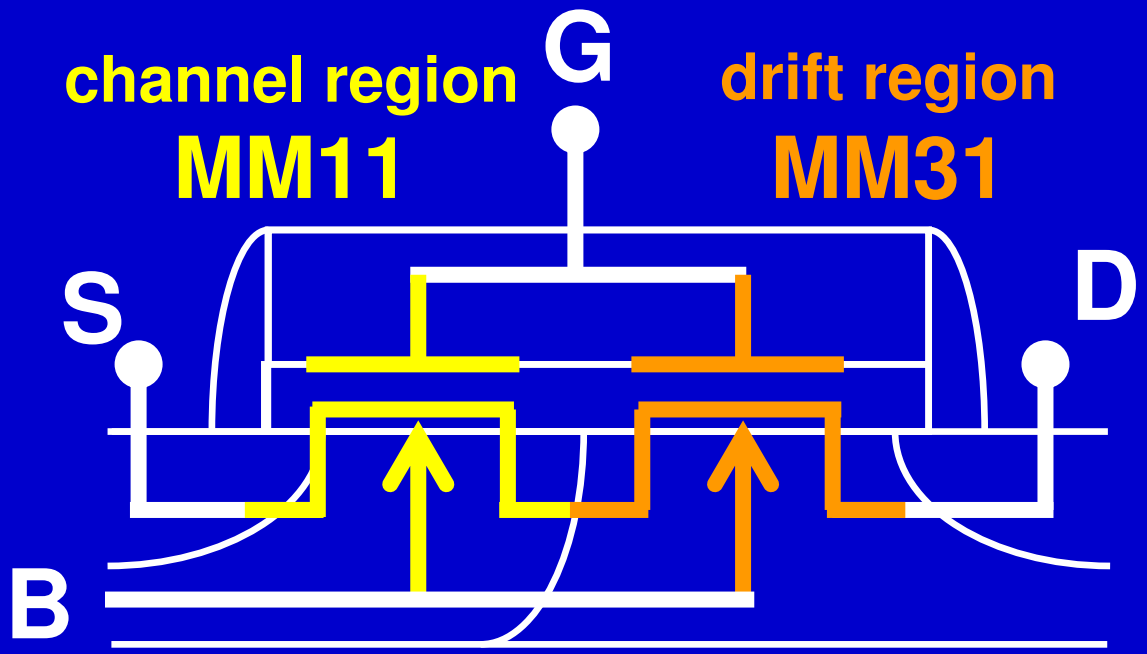


LDMOS applications ⇒ accurate modelling important

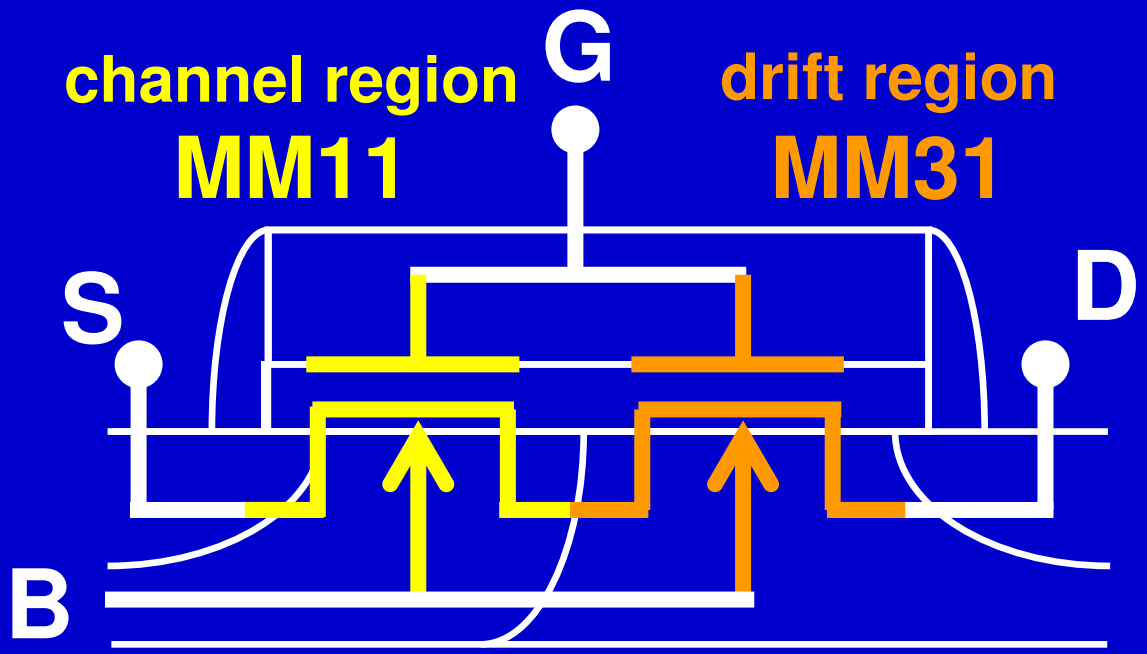
modelling approach: sub-circuit models



modelling approach: sub-circuit models



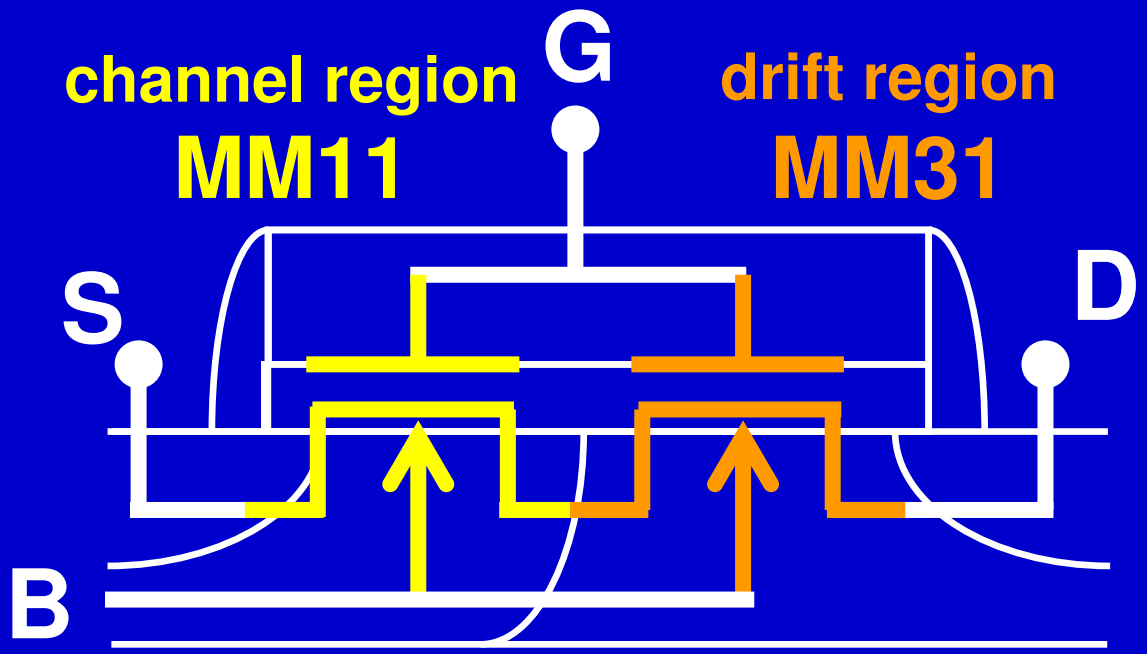
modelling approach: sub-circuit models



pro's

- flexible
- charge partitioning
  channel / drift region

modelling approach: sub-circuit models



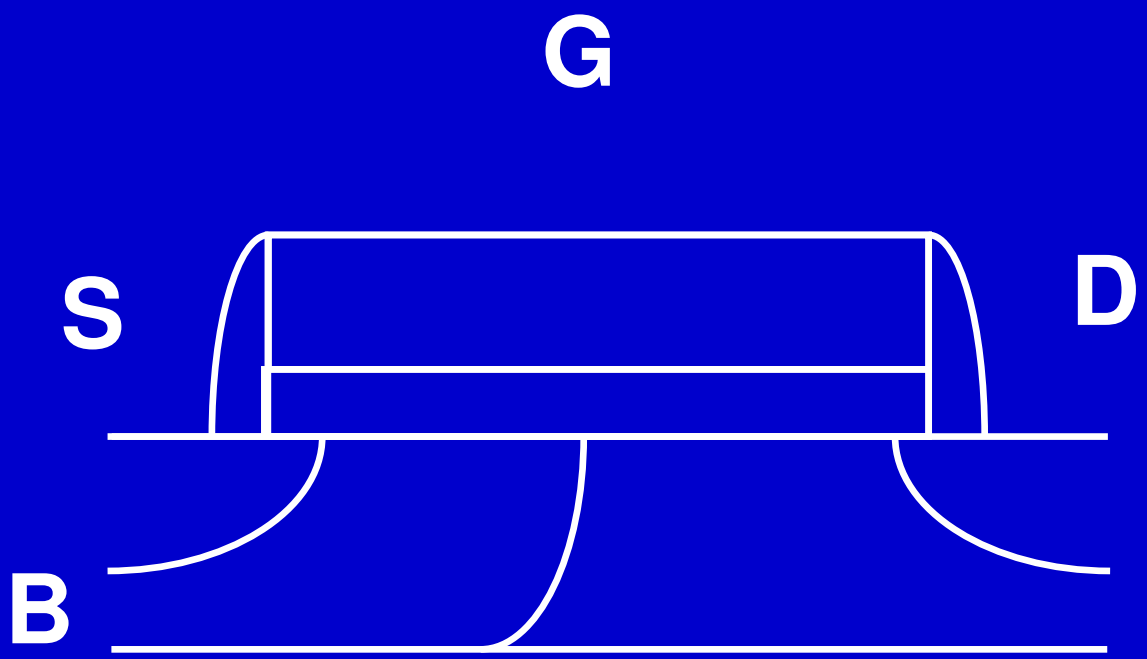
pro's

- flexible
- charge partitioning channel / drift region

con's

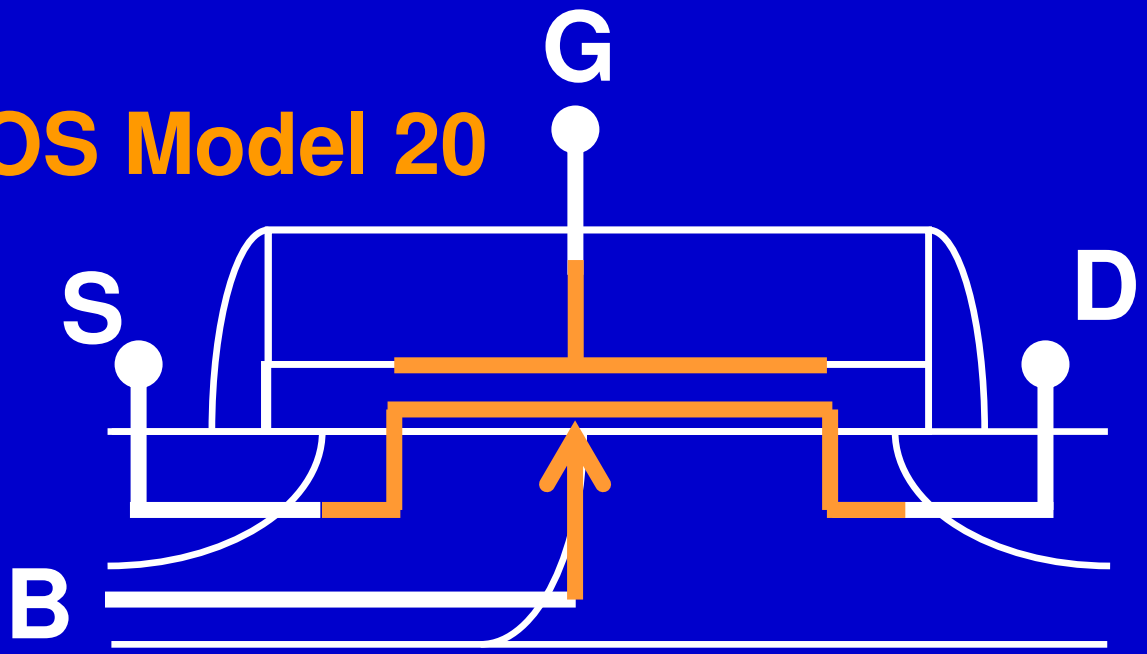
- uncontrolled node
- computation time / convergence

modelling approach: single models

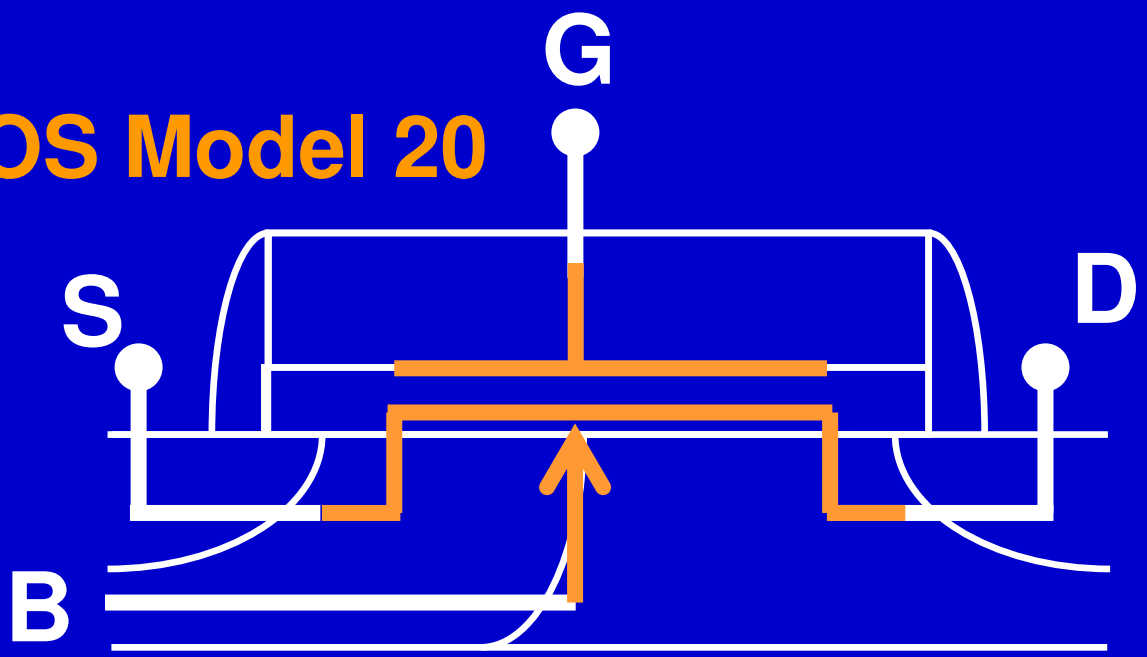


modelling approach: single models

MOS Model 20



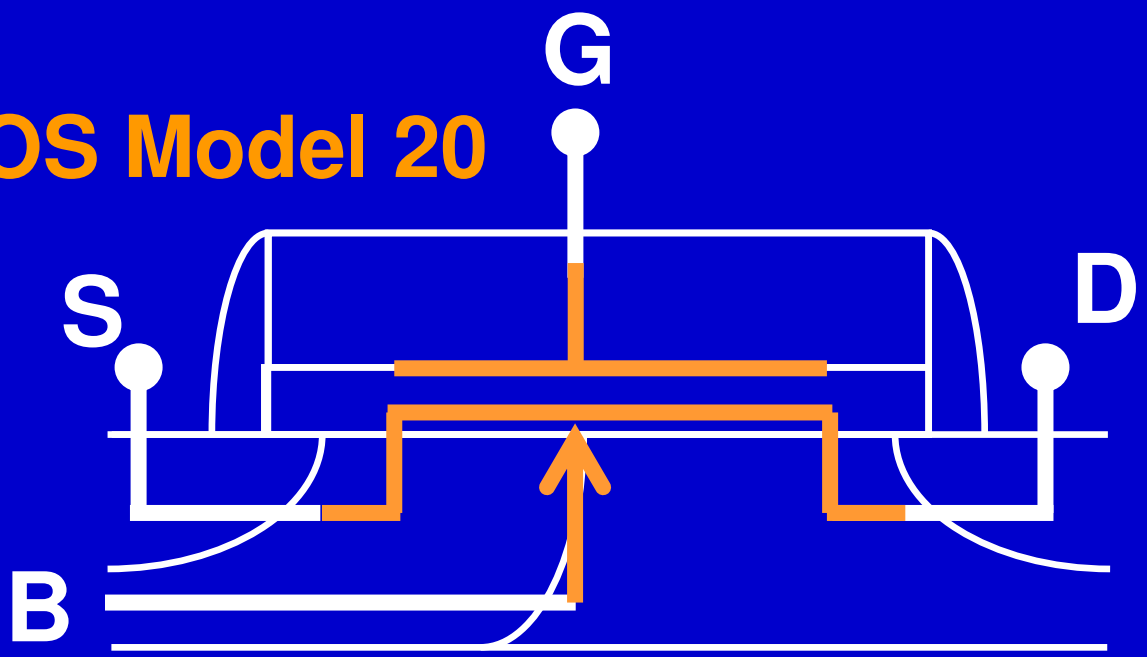
modelling approach: single models



pro's

- no uncontrolled node
- convergence

modelling approach: single models



pro's

- no uncontrolled node
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- charge partitioning
  channel / drift region

outline

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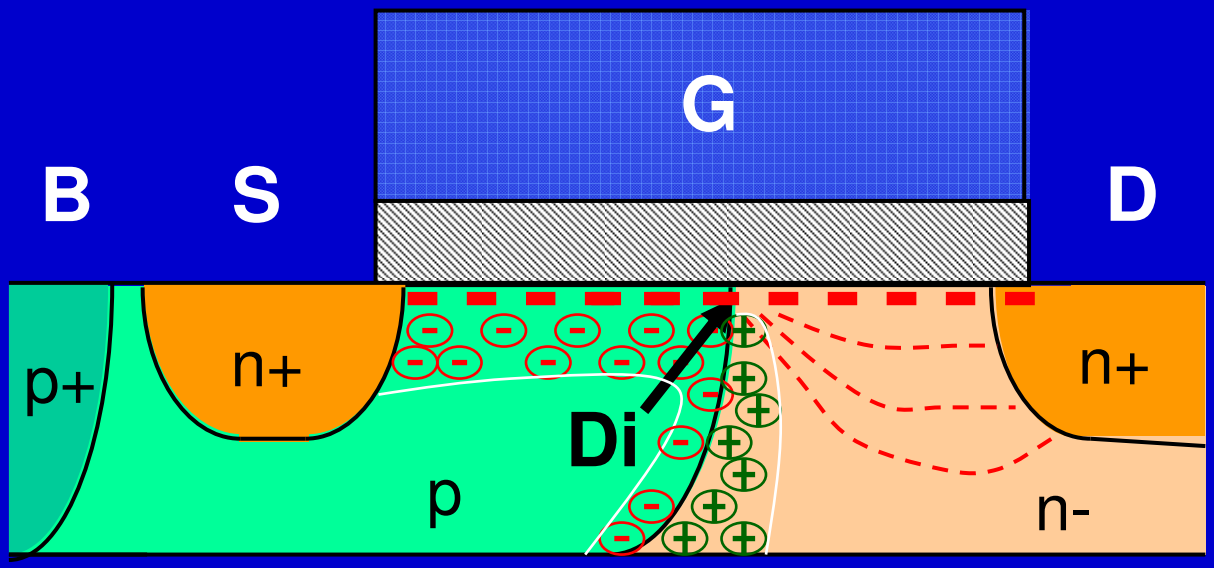
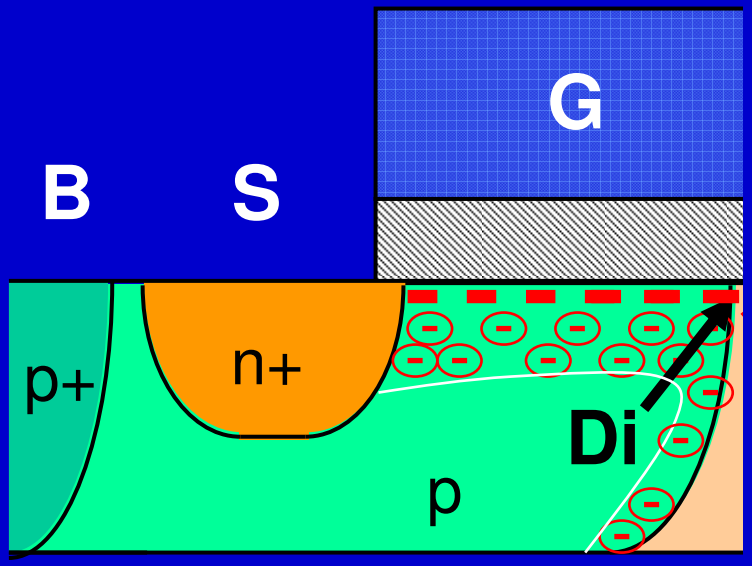
- MOS Model 20
  - DC-model
    - comparison with experimental data
  - nodal charge model
- quasi-saturation
- summary

MOS Model 20: DC-model



Continuity eq: $I_{ch} = I_{dr}$

MOS Model 20: DC-model

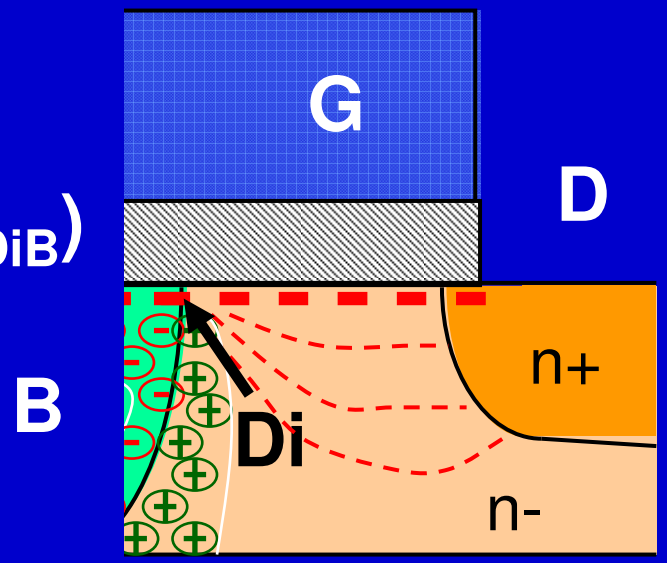


$$I_{ch} = I_{ch}\,(V_{DiS},\ V_{GS},\ V_{SB})$$

- strong inversion
- mobility reduction due to vertical field
- velocity saturation

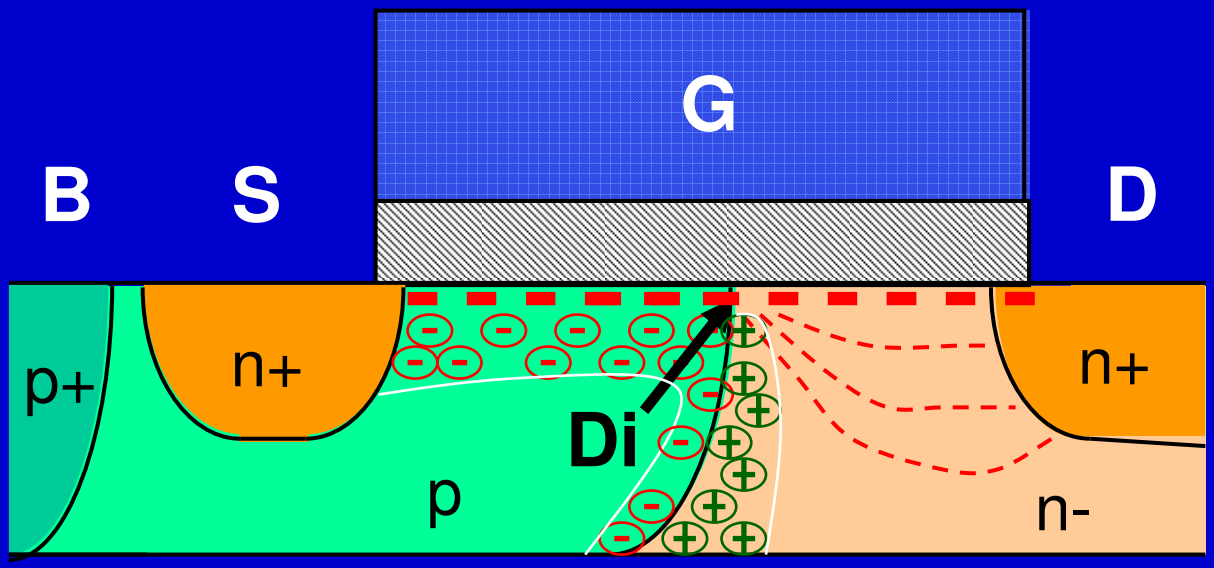
MOS Model 20: DC-model

$$I_{dr} = I_{dr}\,(V_{GDi},\ V_{GD},\ V_{DiB})$$



- accumulation
- depletion
- bulk current
- mobility reduction due to vertical field

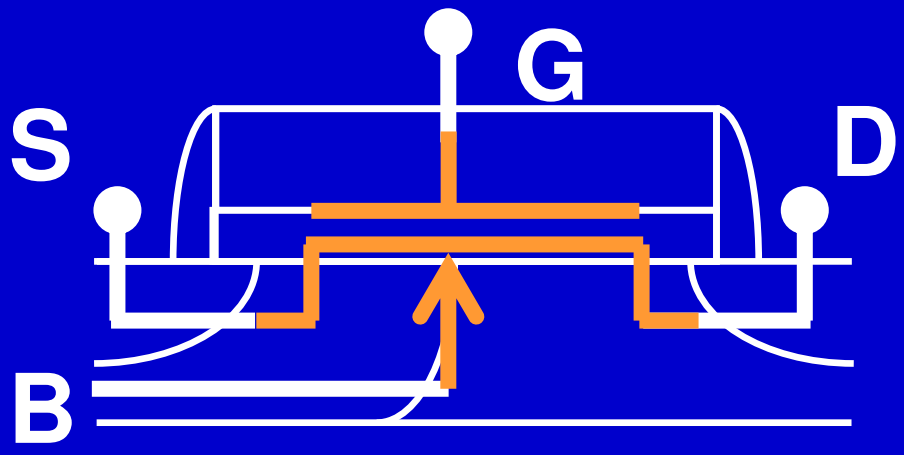
MOS Model 20: DC-model



internal node Di expressed analytically from

$$I_{ch}\,(V_{DiS},\ V_{GS},\ V_{SB}) = I_{dr}\,(V_{DiS},\ V_{DS},\ V_{GS},\ V_{SB})$$

MOS Model 20: DC-model



surface-potential based

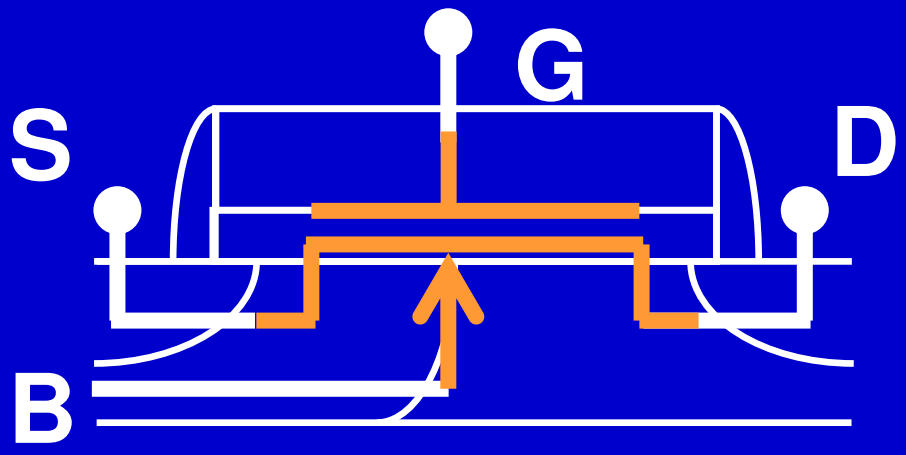
$$I_{DS} = I_{ch}(\psi_{sL}, \psi_{s0})$$

$$\psi_{s0} = \psi_{s0}(V_{SB}, V_{GB})$$

$$\psi_{sL} = \psi_{sL}(V_{DiB}, V_{GB})$$

- weak and strong inversion
- saturation in channel region
- accumulation and bulk current in drift region
- mobility reduction
- DIBL and static feedback
- weak avalanche

MOS Model 20: DC-model



- 21 dc-parameters
- temperature scaling (6 parameters)
- self-heating
- width-scaling
- length scaling

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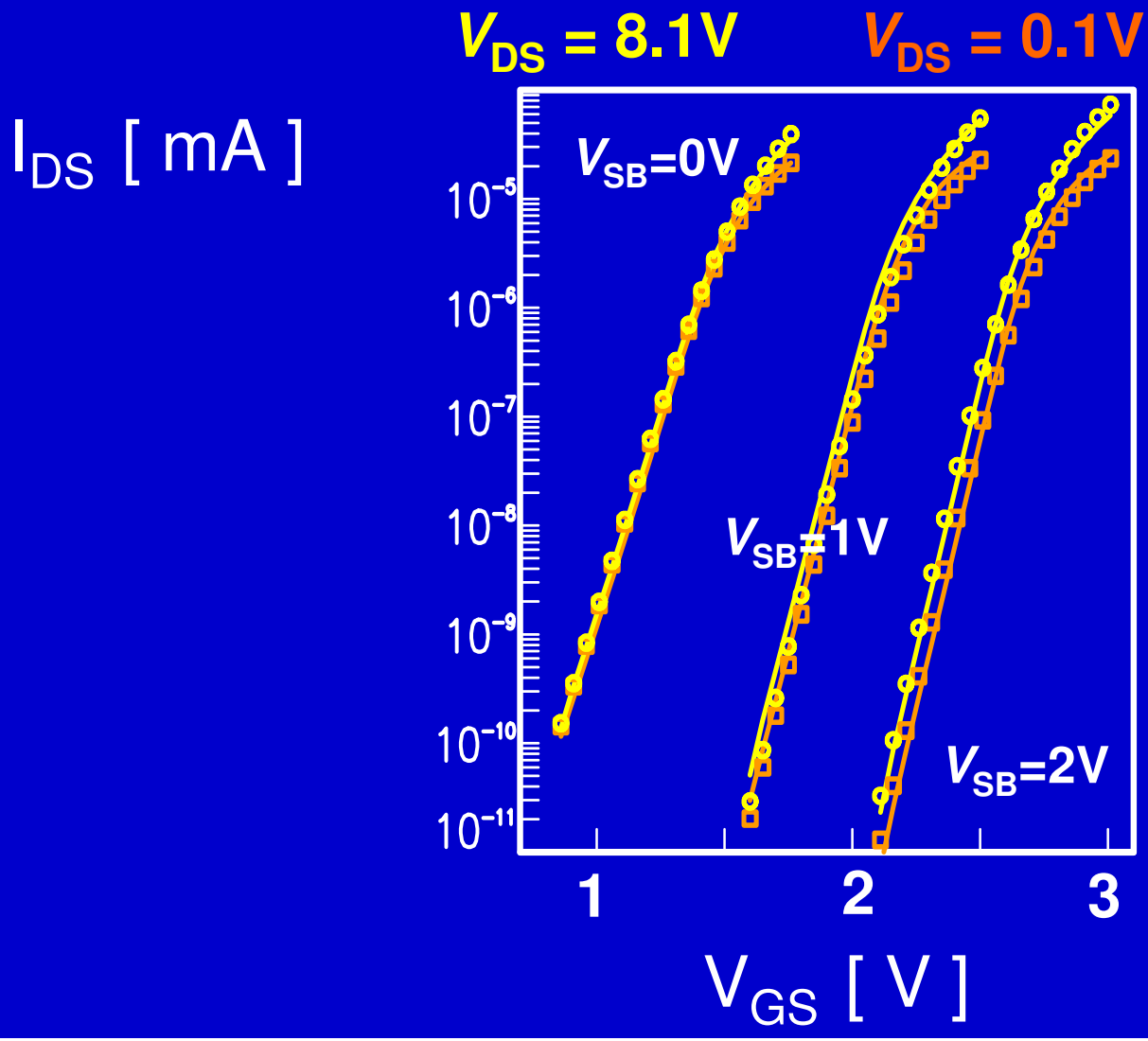
MOS Model 20: experimental data

12V SOI-LDMOS: T_{ox}= 38 nm, W= 17 μm, L= 1.6 μm, T= 25 °C



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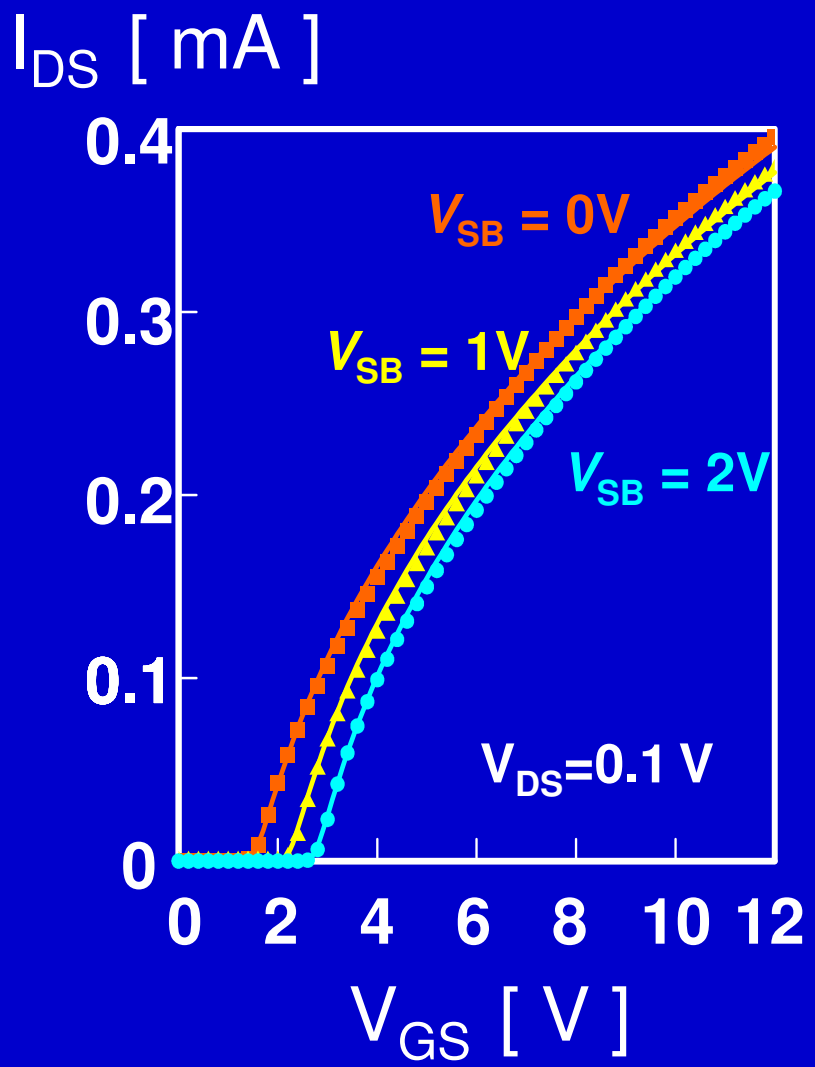

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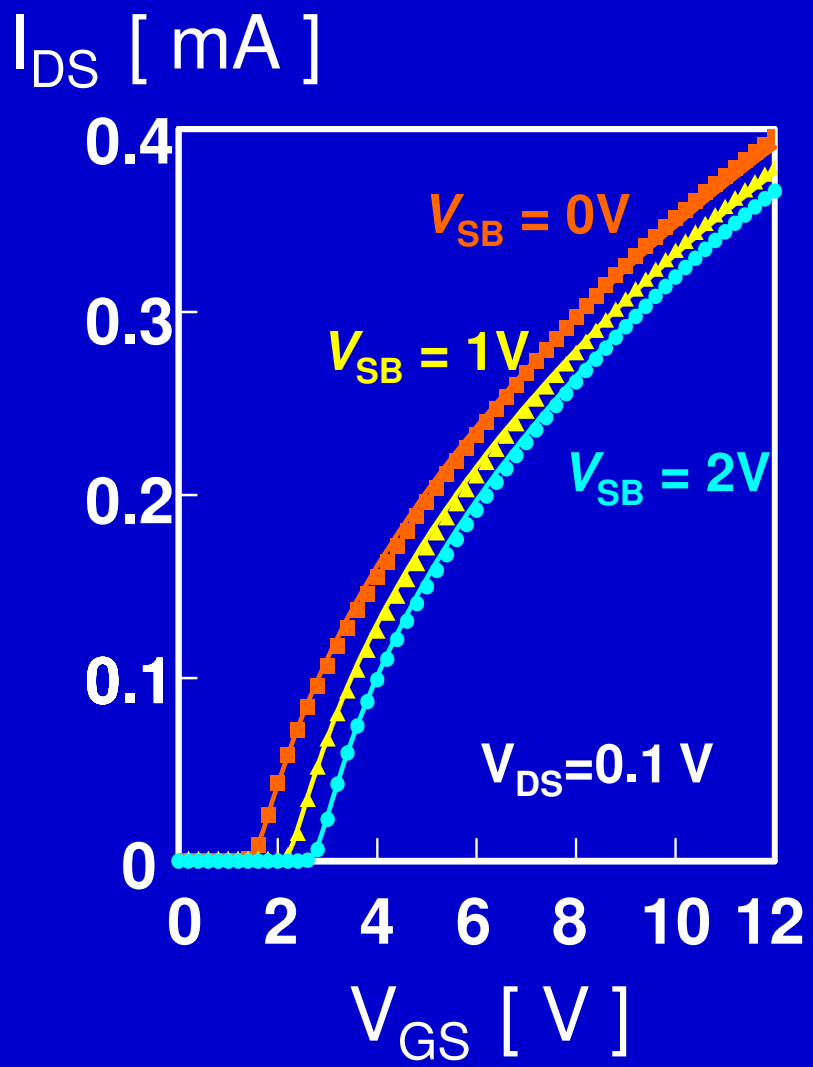

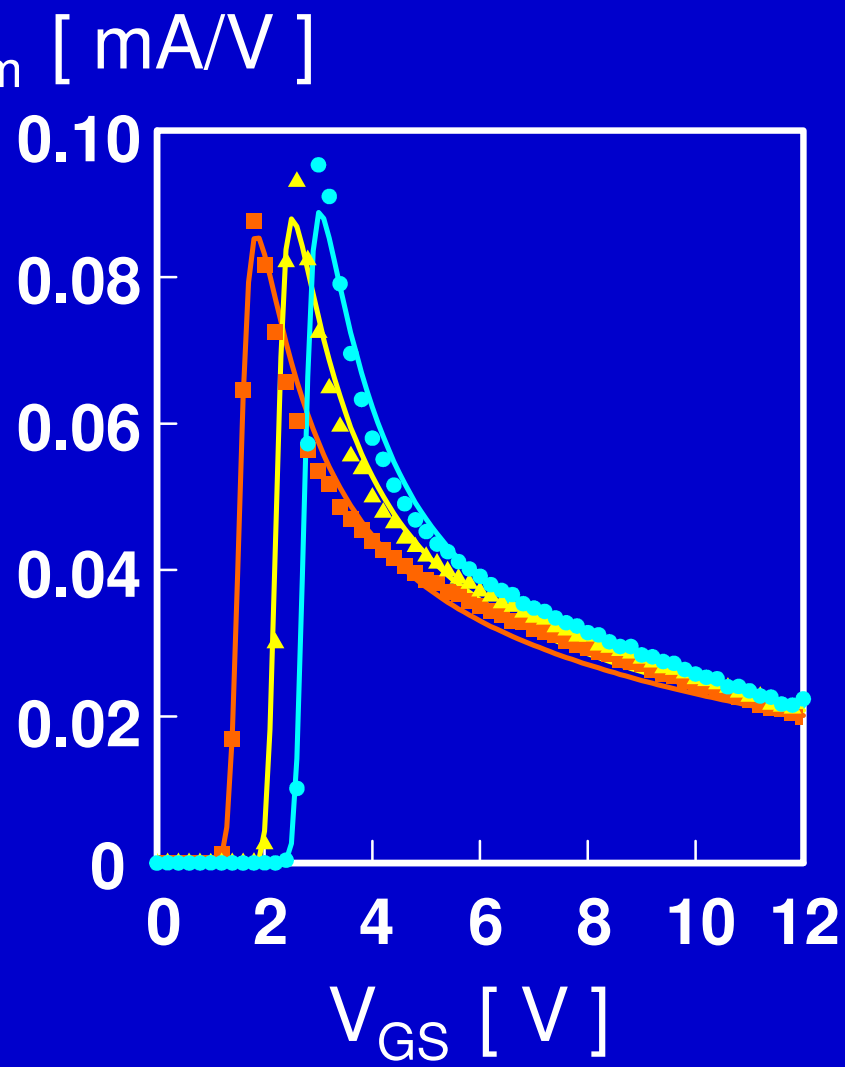

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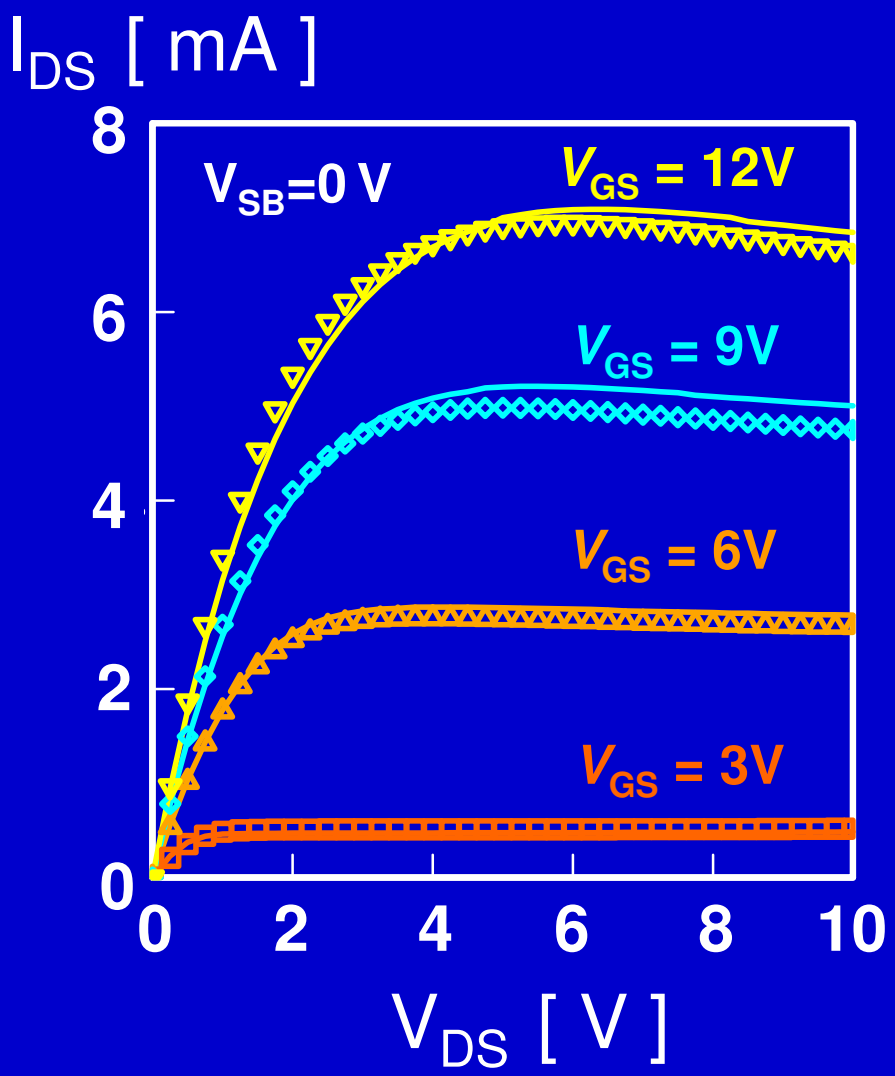

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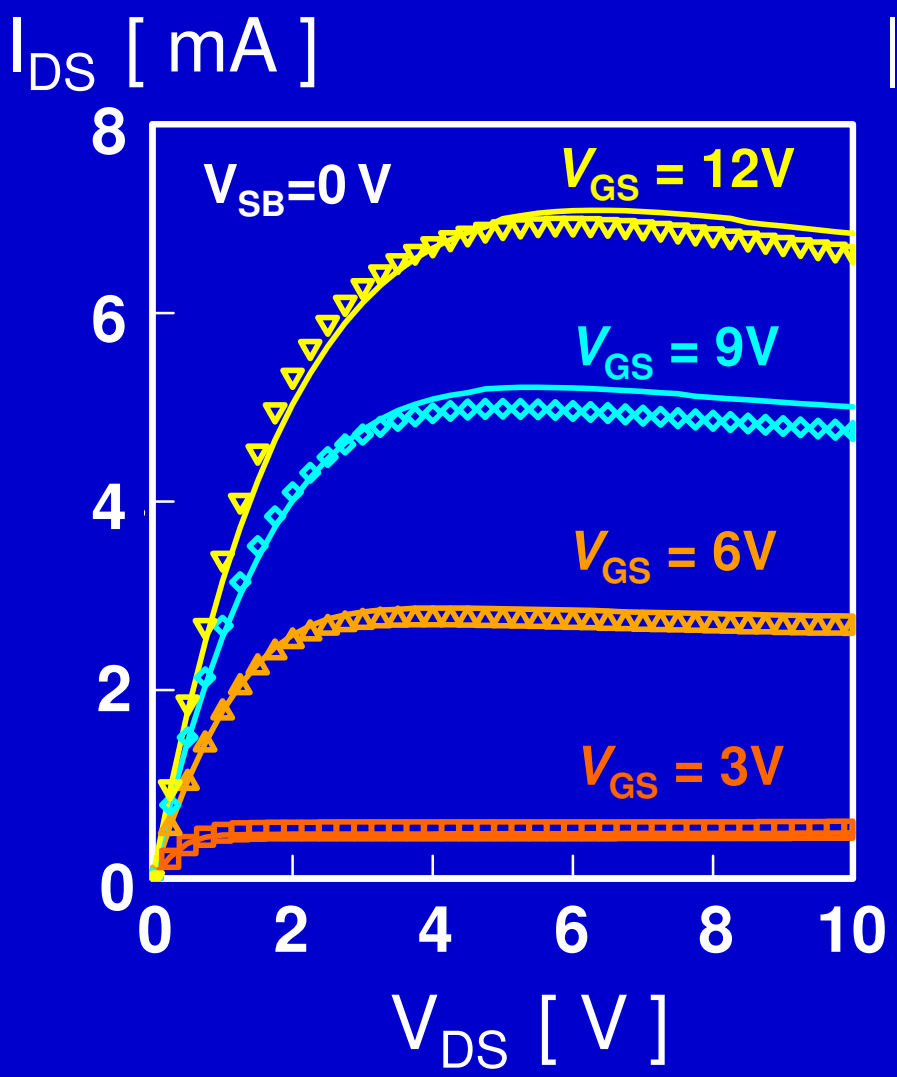

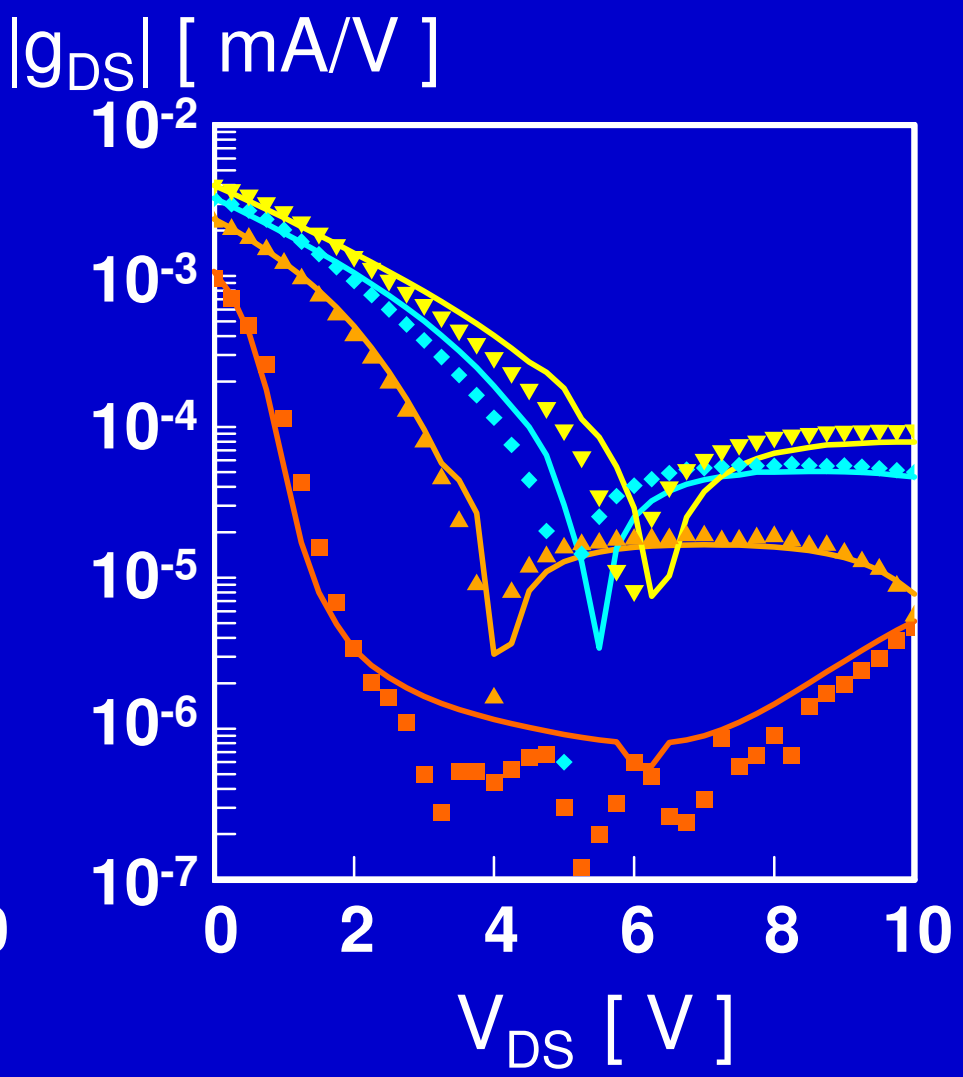

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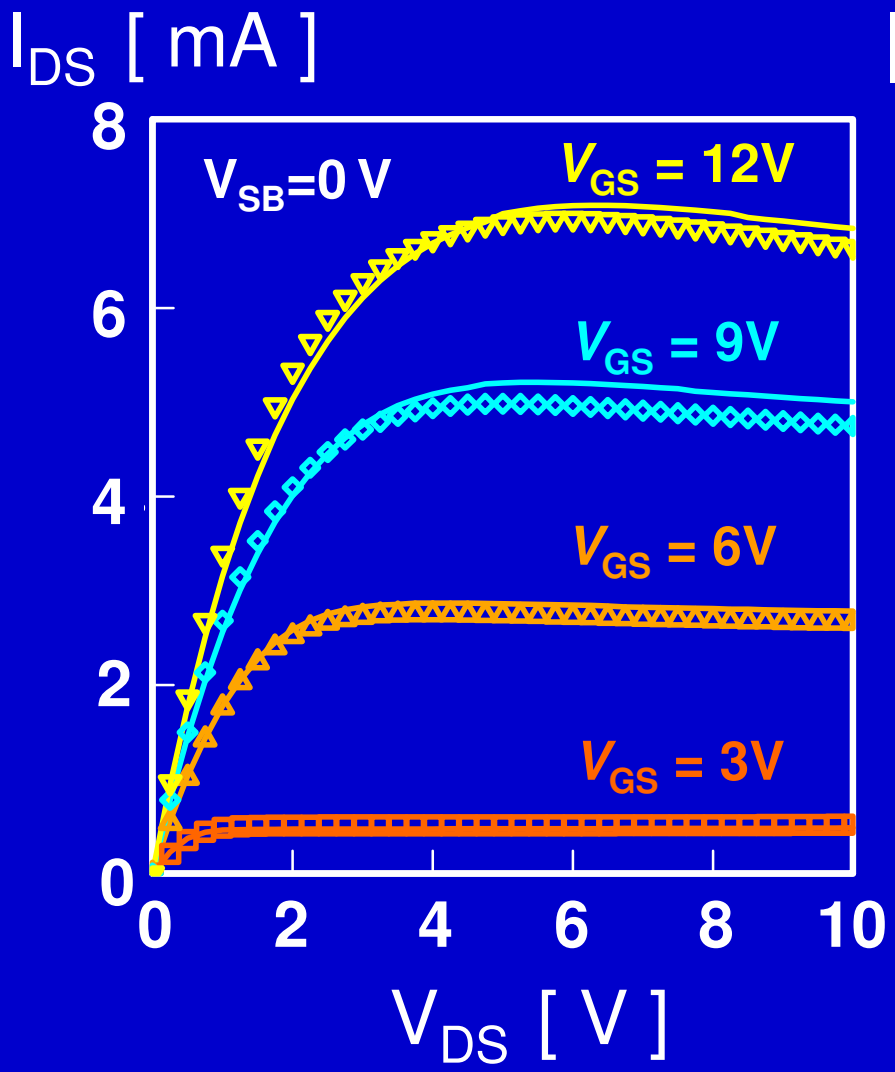

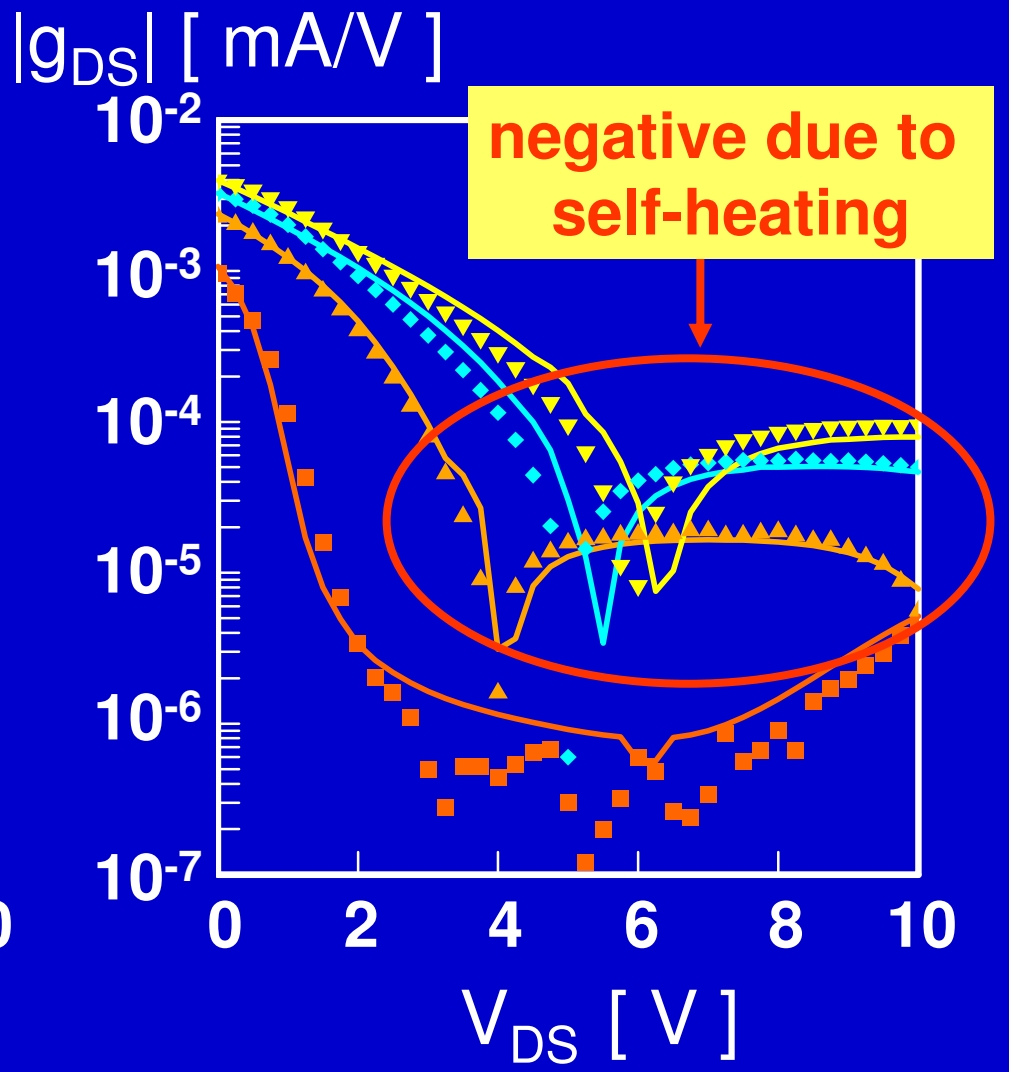

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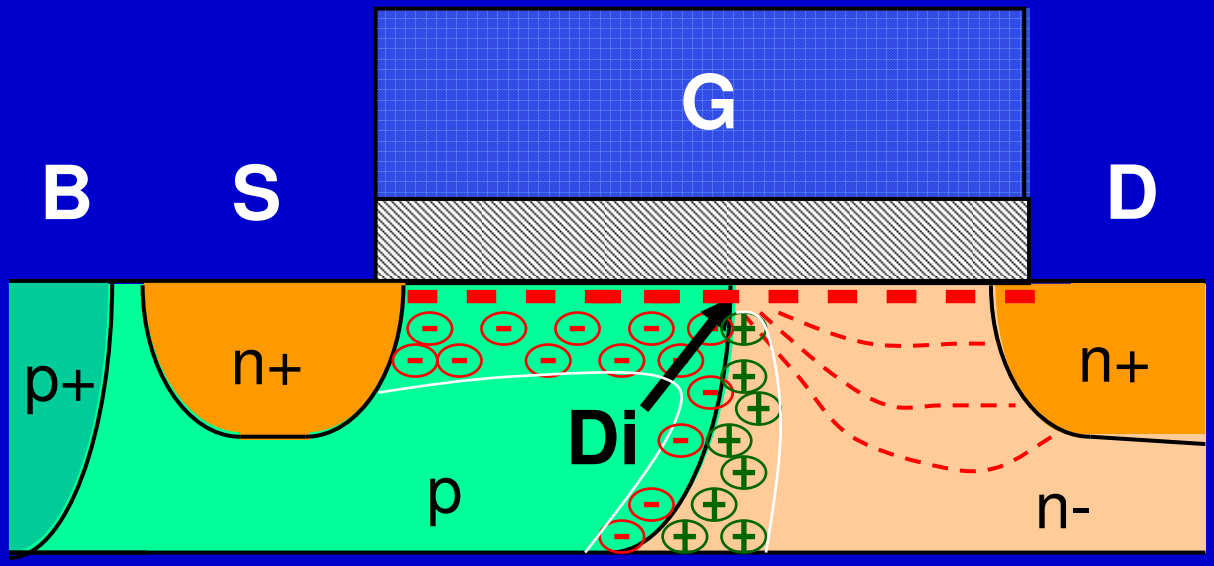
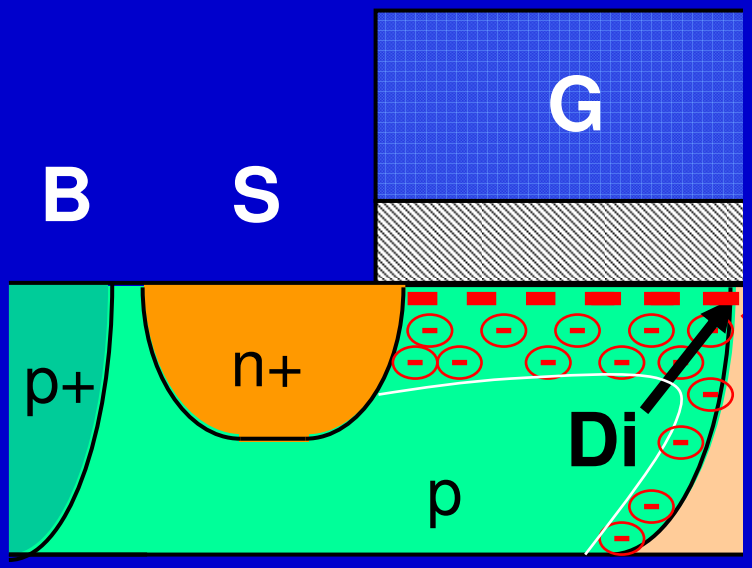
MOS Model 20: nodal charge model



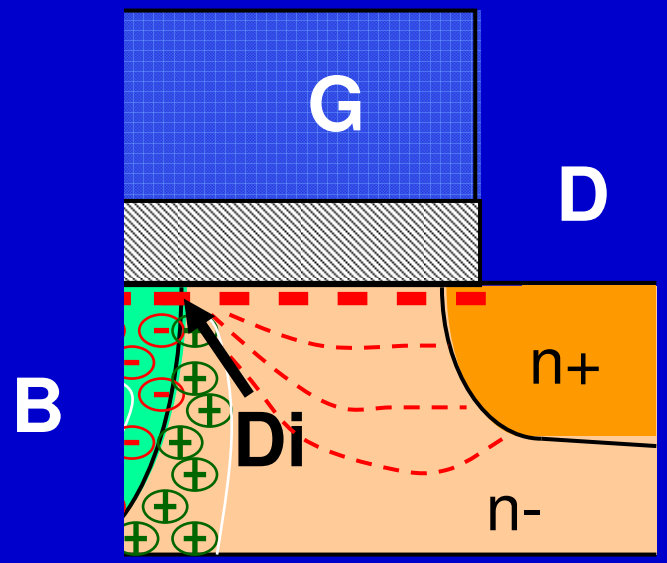
MOS Model 20: gate and bulk charges



$$Q_{G,\,channel} = -W \int_0^L \left(Q'_{inv} + Q'_{dep} + Q'_{acc} \right) \cdot dx$$

$$Q_{B,\,channel} = W \int_0^L \left(Q'_{dep} + Q'_{acc} \right) \cdot dx$$

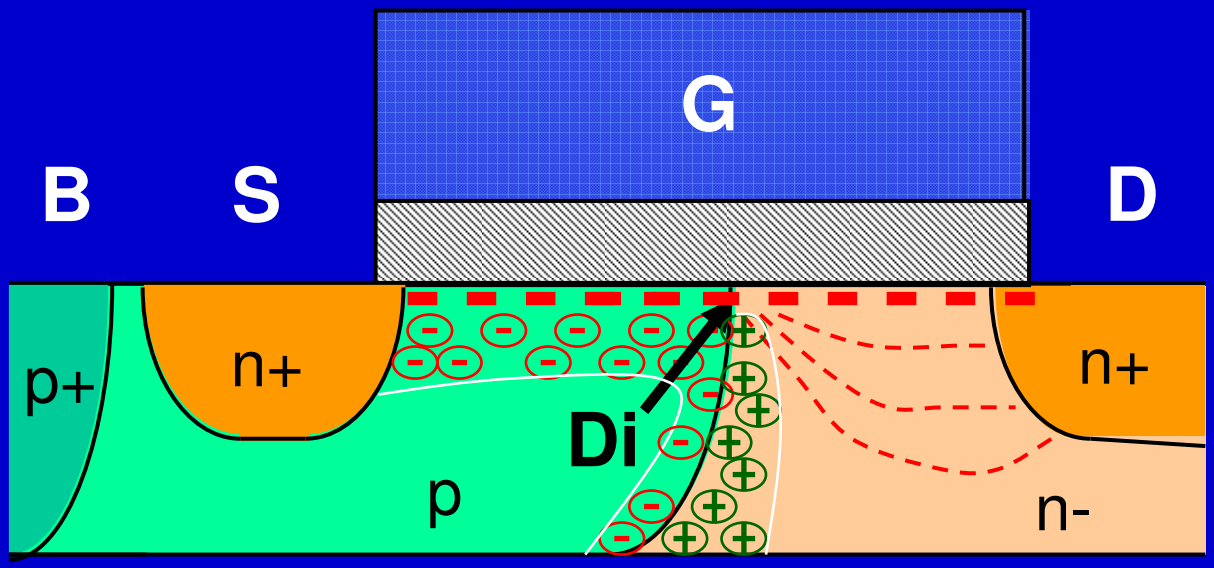
MOS Model 20: gate and bulk charges



$$Q_{G,\,\text{drift region}} = -W \int_0^{L_{dr}} \left(Q'_{inv} + Q'_{dep} + Q'_{acc} \right) \cdot dx$$

$$Q_{B,\,\text{drift region}} = W \int_0^{L_{dr}} Q'_{inv} \cdot dx$$

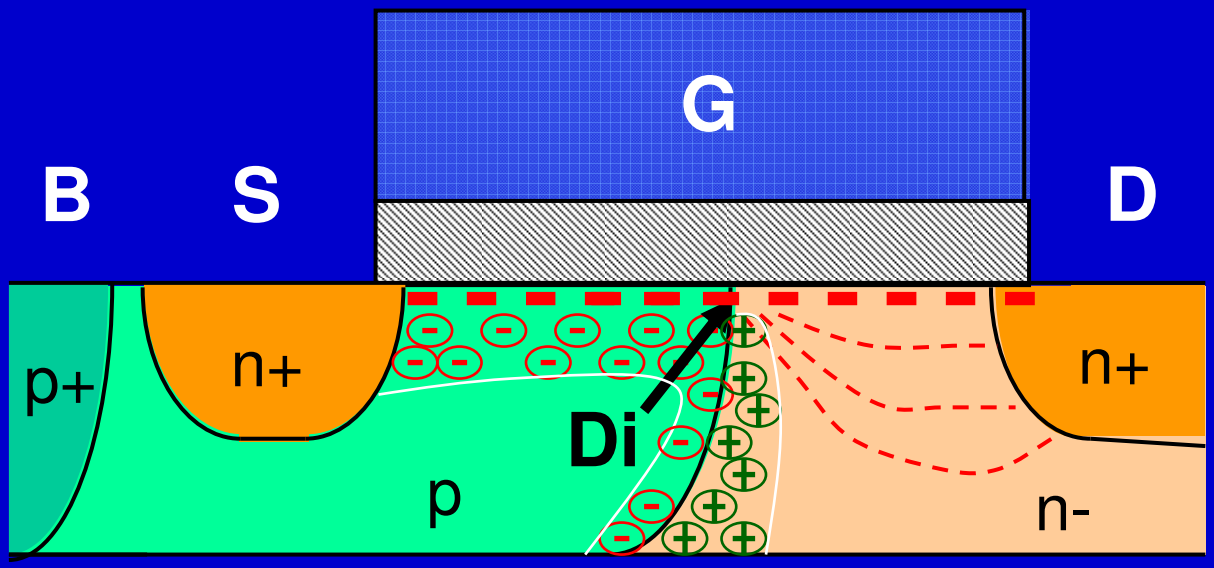
MOS Model 20: gate and bulk charges



$$Q_{G,\,LDMOS} = Q_{G,\,channel} + Q_{G,\,drift\ region}$$

$$Q_{B,\,LDMOS} = Q_{B,\,channel} + Q_{B,\,drift\ region}$$

MOS Model 20: gate and bulk charges



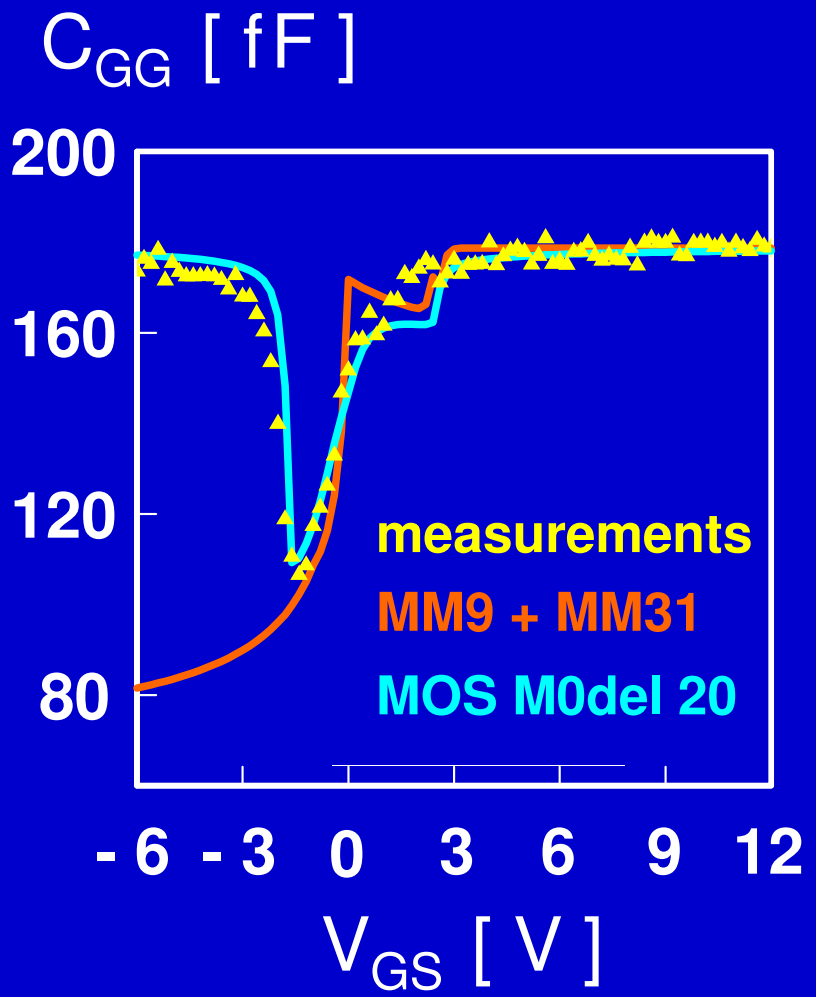
$$Q_{G,\,LDMOS} = Q_{G,\,channel} + Q_{G,\,drift\ region}$$

$$C_{ij} = \left(2 \cdot \delta_{ij} - 1\right) \cdot \frac{\partial Q_i}{\partial V_j}$$

$$Q_{B,\,LDMOS} = Q_{B,\,channel} + Q_{B,\,drift\ region}$$

MOS Model 20: experimental data

14V SOI-LDMOS: T_{ox}= 60 nm, W= 50 μm, L= 5 μm, T= 25 °C



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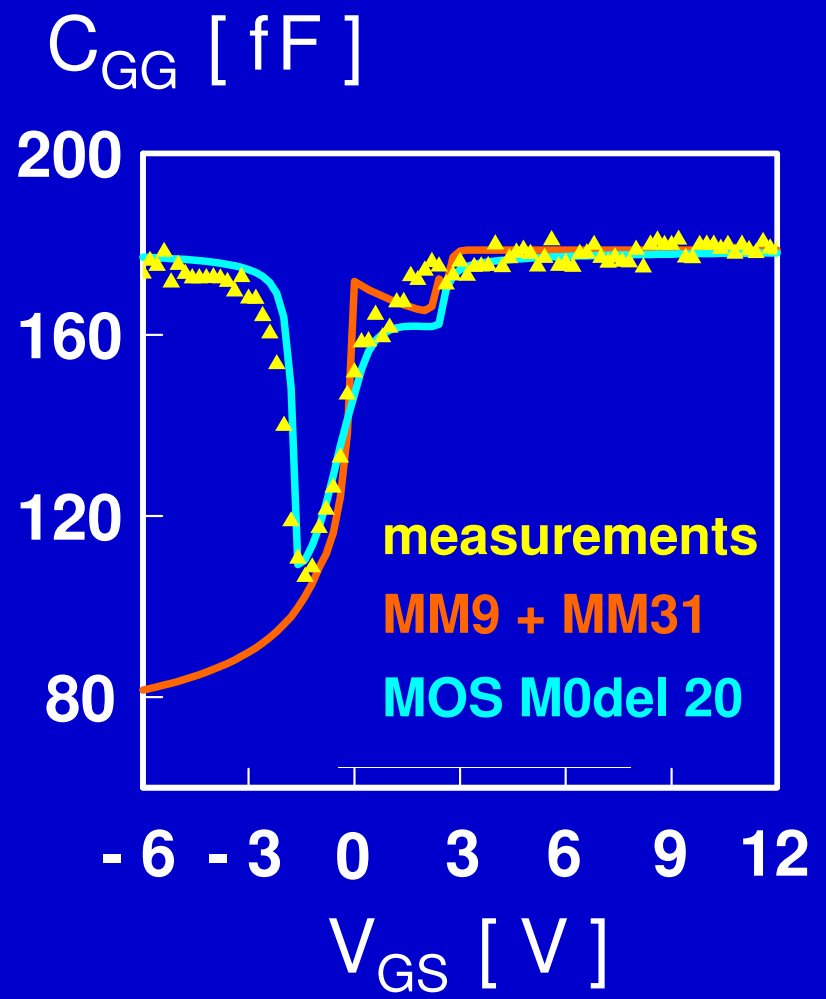
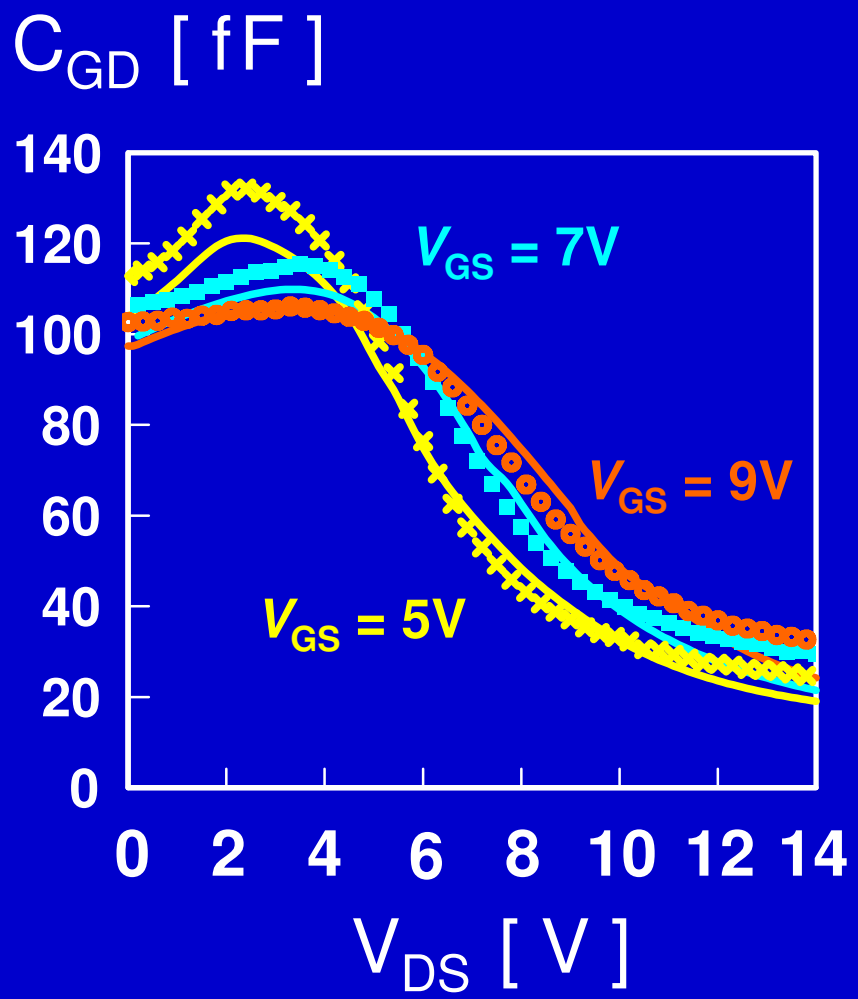
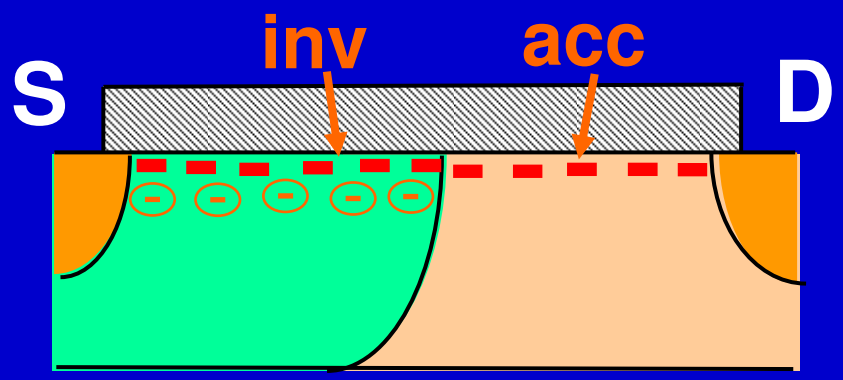




MOS Model 20: source and drain charges



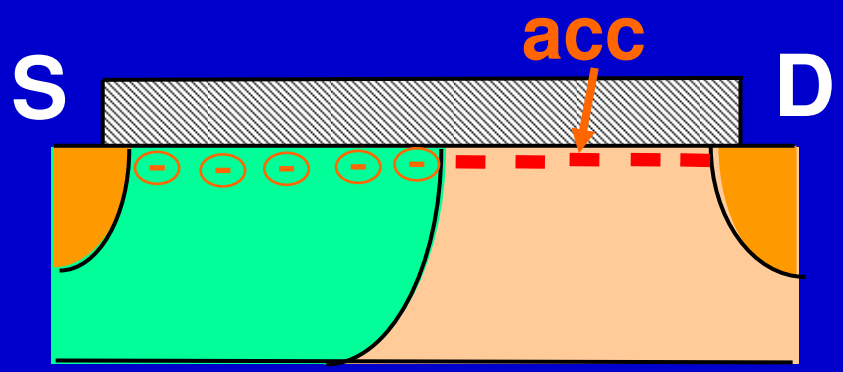
channel region in strong inversion

Ward-Dutton (uniform MOSFET)

$$Q_{D,\,LDMOS} = W\int_0^{L}\frac{x}{L+L_{dr}}Q'_{inv}\,dx + W\int_{L}^{L+L_{dr}}\frac{x}{L+L_{dr}}Q'_{acc}\,dx$$

$$Q_{S,\,LDMOS} = W\int_0^{L}\frac{L+L_{dr}-x}{L+L_{dr}}Q'_{inv}\,dx + W\int_{L}^{L+L_{dr}}\frac{L+L_{dr}-x}{L+L_{dr}}Q'_{acc}\,dx$$

MOS Model 20: source and drain charges



channel region in weak inversion

all charge in the drift region attributed to the drain

$$Q_{D,\,LDMOS} = W \int_{L}^{L+L_{dr}} Q'_{acc}\, dx$$

$$Q_{S,\,LDMOS} = 0$$

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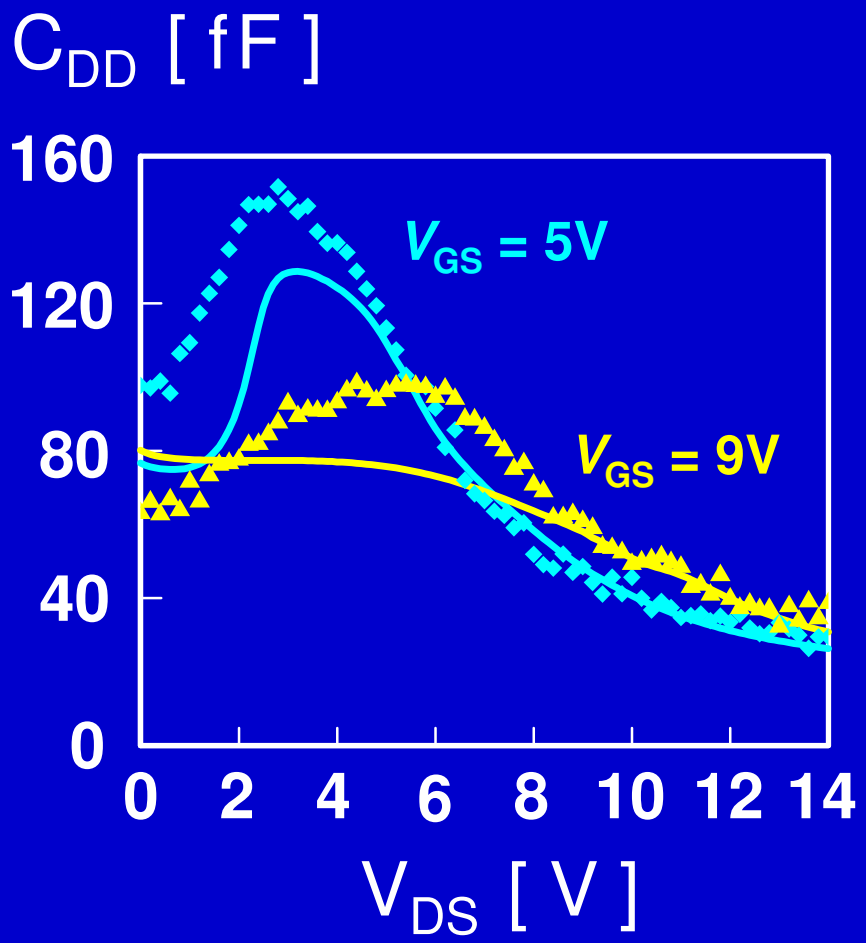

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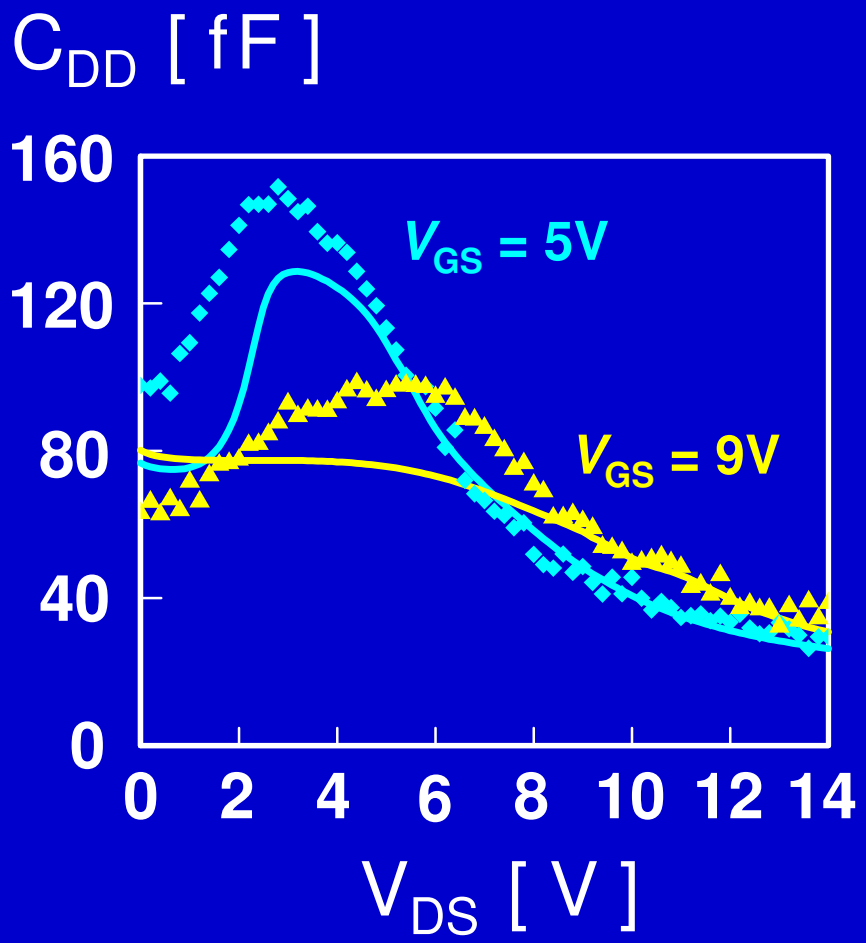

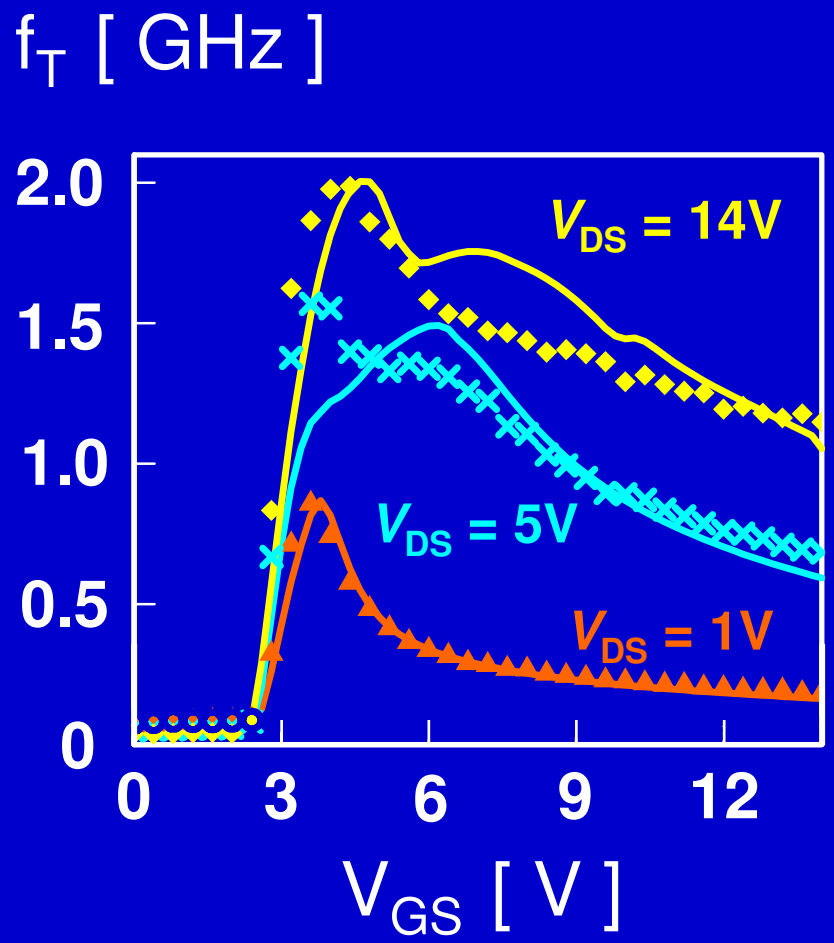

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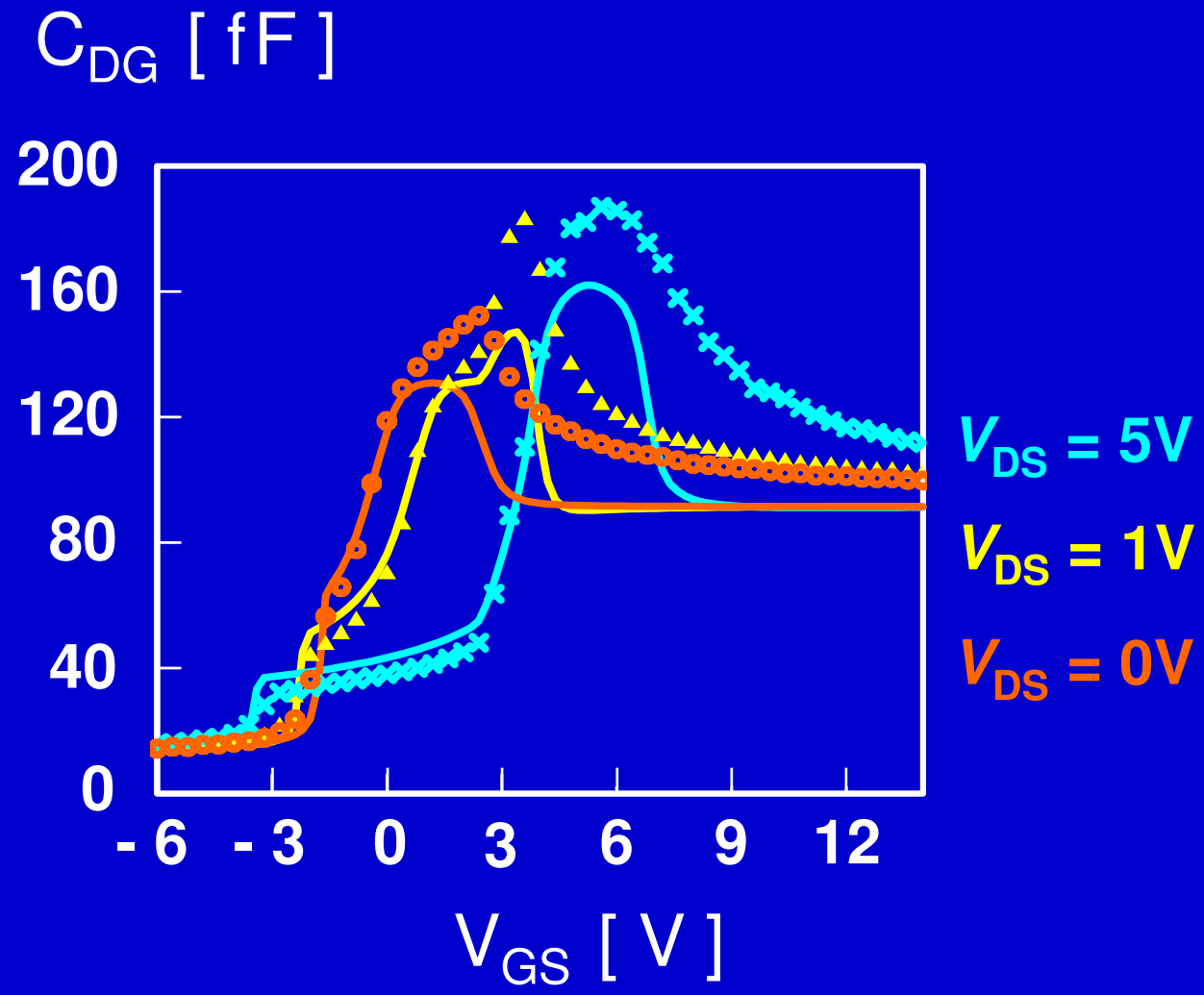

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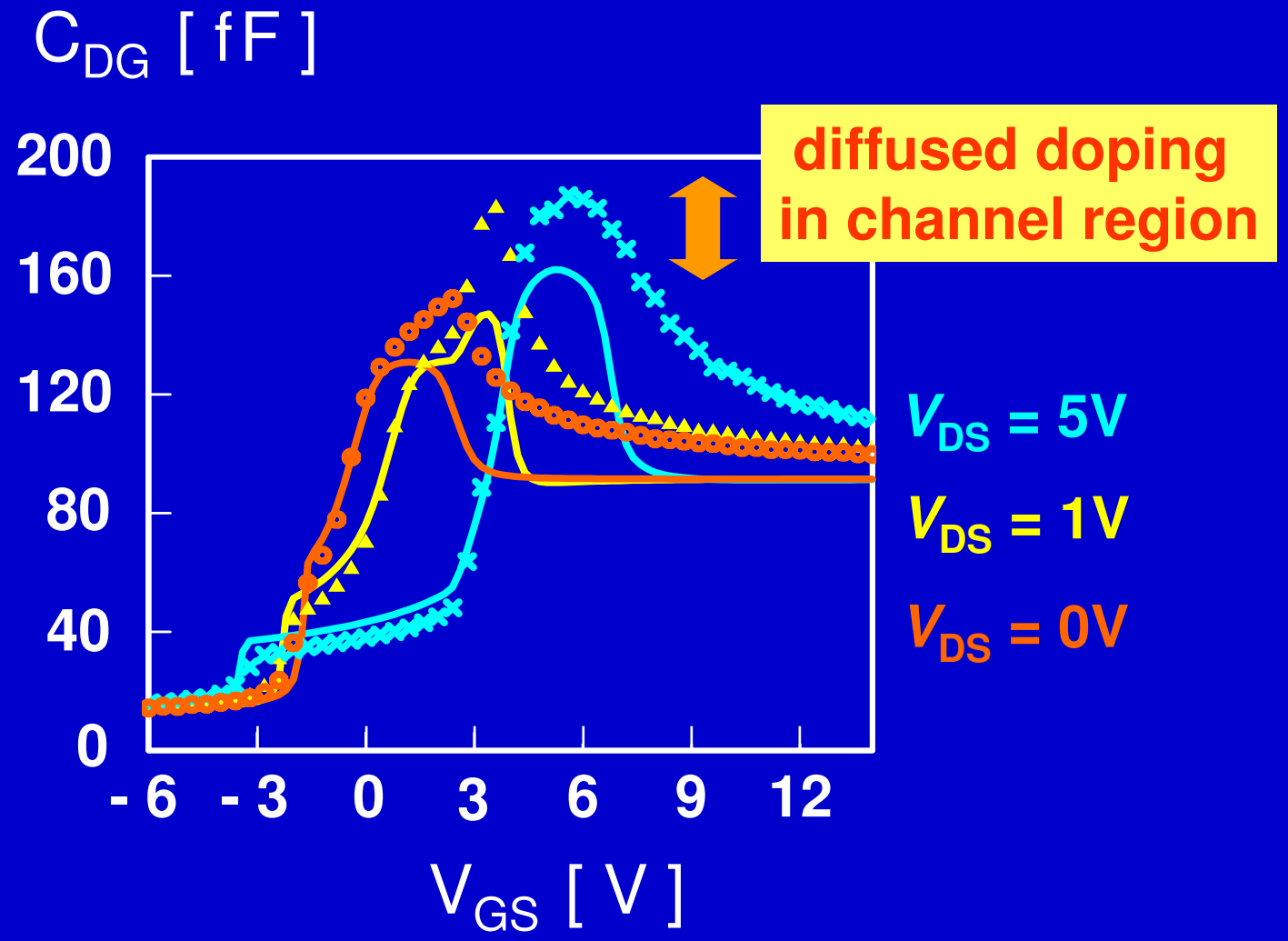

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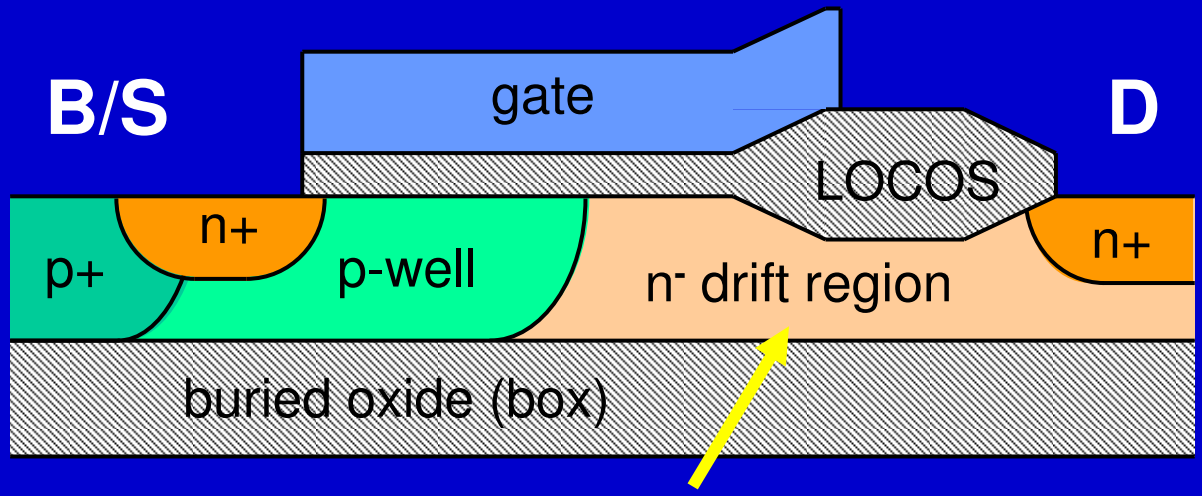
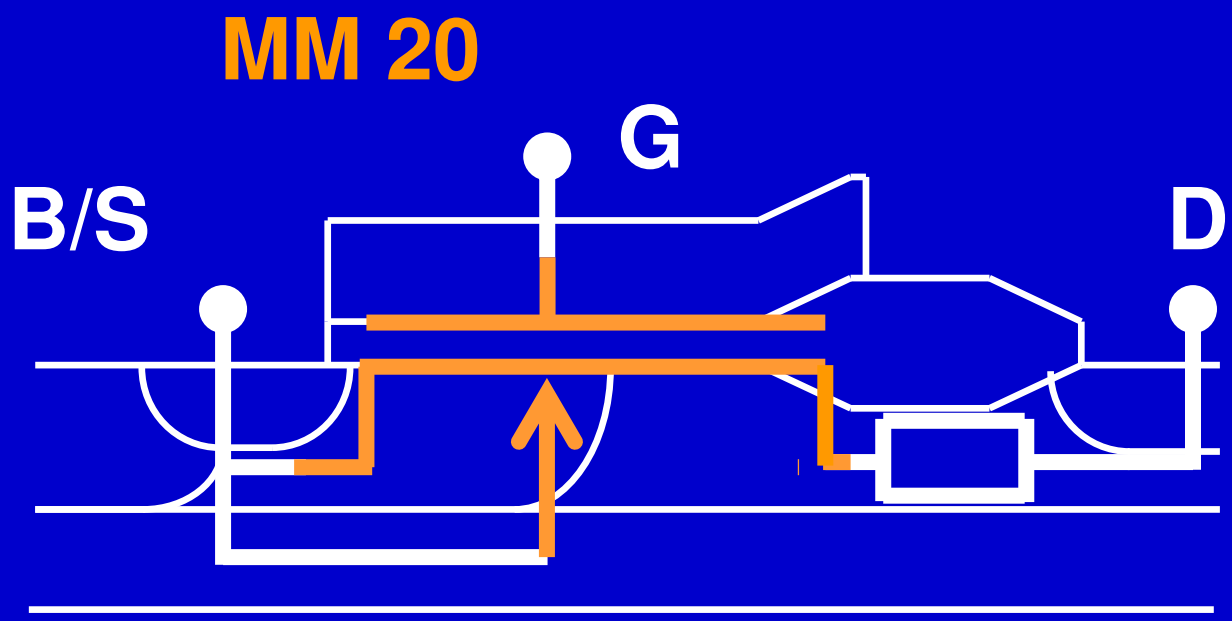
quasi-saturation

High-voltage



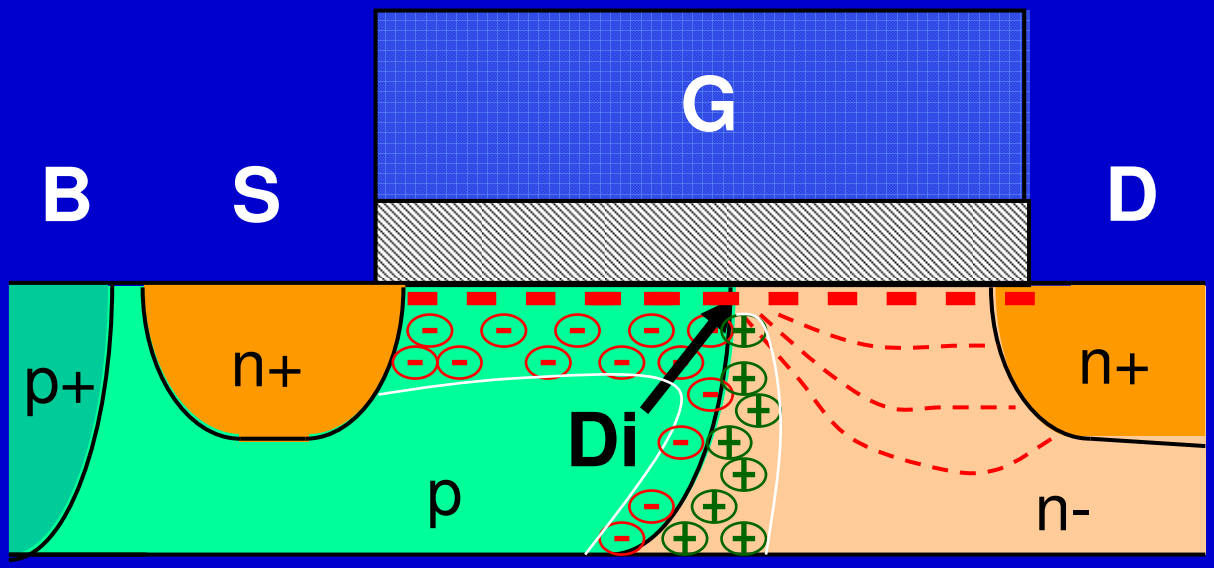
saturation may occur in drift region

quasi-saturation

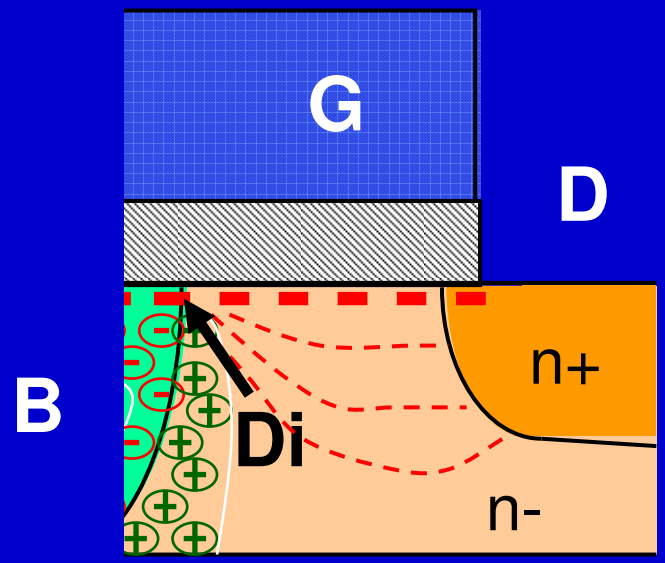


new MM 20: includes quasi-saturation

quasi-saturation

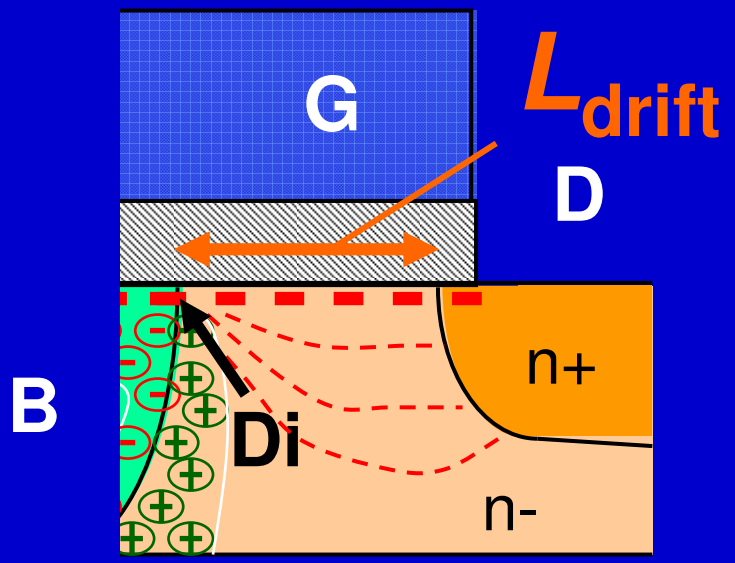


quasi-saturation



- accumulation
- bulk current
- mobility reduction due to vertical field
- depletion
- velocity saturation

quasi-saturation

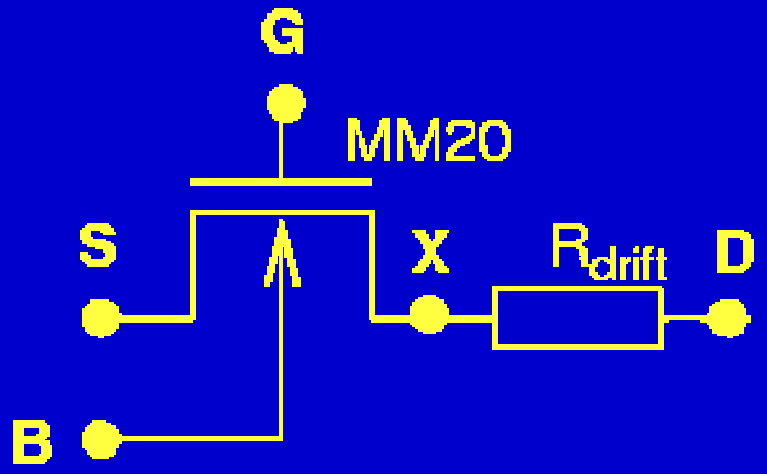


$$\mu^{drift} = \frac{\mu_{eff}}{1 + \theta_3^{drift} \cdot V_{DDi,eff}}$$

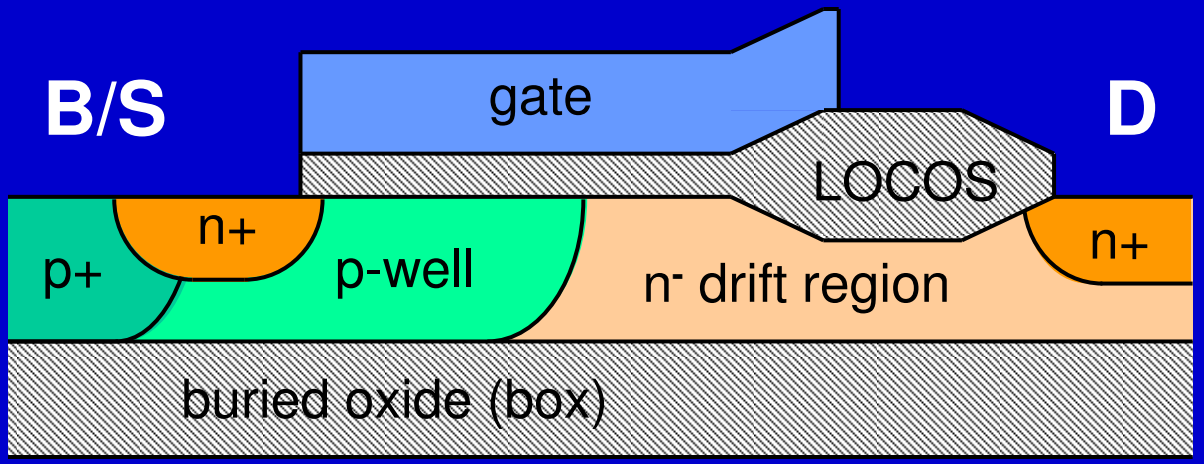
$$\theta_3^{drift} = \frac{\mu_{eff}}{L_{drift} \cdot v_{sat}}$$

quasi-saturation

sub-circuit

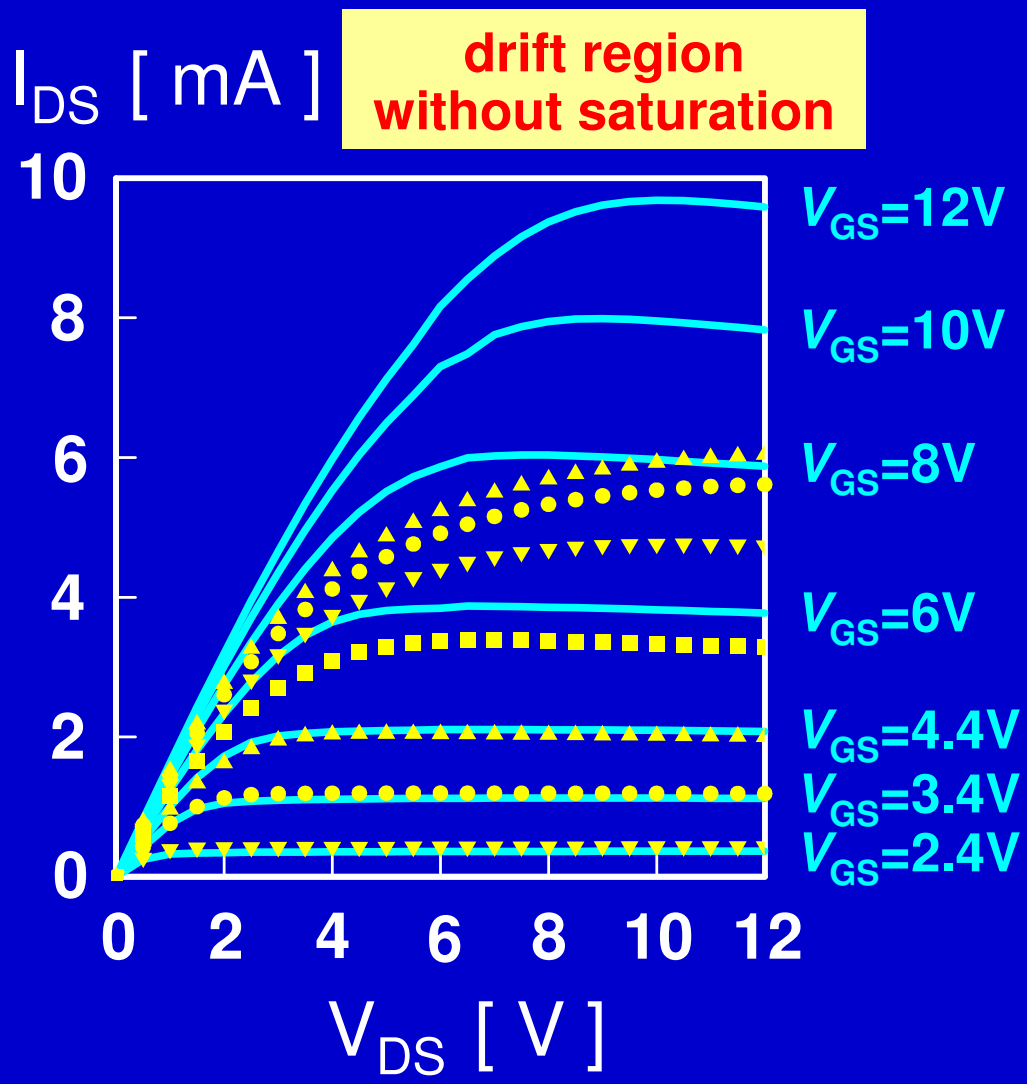


High-voltage



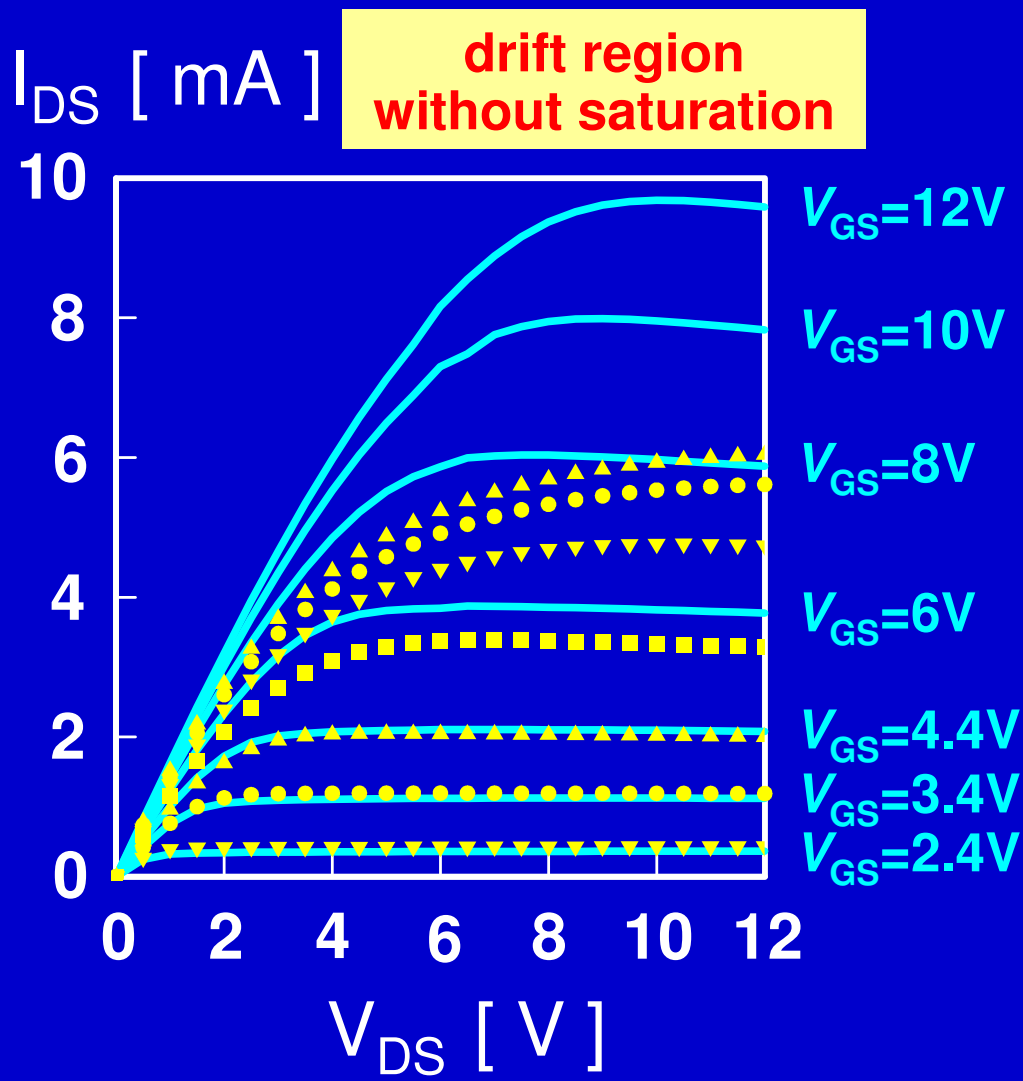
quasi-saturation

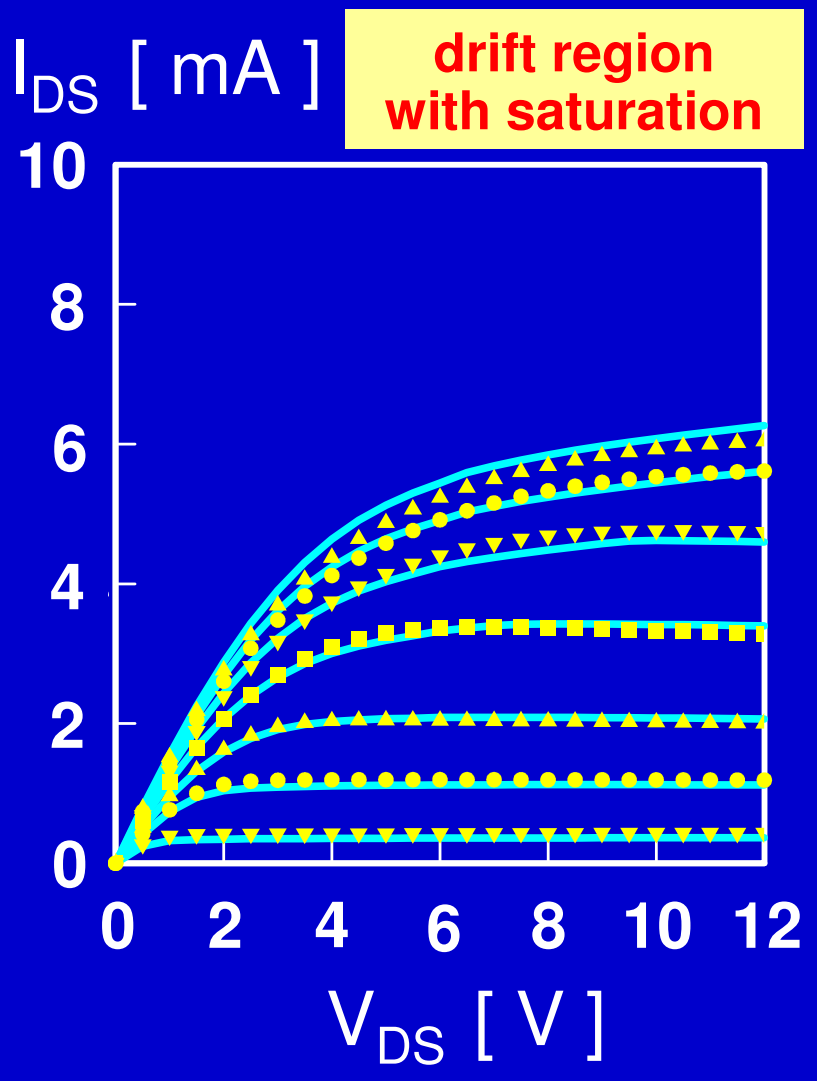
60V SOI-LDMOS: T_{ox}= 38nm, W= 20μm, L= 2.6μm, L_{locos}= 3.5μm, T= 25 °C



quasi-saturation

60V SOI-LDMOS: T_{ox}= 38nm, W= 20μm, L= 2.6μm, L_{locos}= 3.5μm, T= 25 °C





summary

MOS Model 20

- **single model**
- **for low-voltage (< 30 V) LDMOS**
- **extension to medium-voltage (< 100V) LDMOS by inclusion of quasi-saturation**
- **includes dc-, charge- and noise model**
- **accurate description of dc- and ac-currents**
- **improvement in simulation speed compared to sub-circuit model**

documentation

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  "Compact modeling of High-Voltage LDMOS Devices including quasi-saturation",

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