

Scalable Electrical Model
for a SOI-RF-LDMOS
Including Drain Drift
Region Resistance
Self-Heating Effects



FTM
SP & HV
Device Characterization & Modeling

Lorenzo Labate
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Authors

Lorenzo Labate

Paolo Villani

Roberto Stella

Enrico Novarini

STMicroelectronics

Front-End Technology and Manufacturing Division
Smart Power & Technology Platform Development
Device Characterization & Modeling Group

Lorenzo
Labate

Böblingen
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FTM-SP&HV-
Device Char. & Model.

MOS-AK
Workshop



Outlines

Introduction

- Work background
 - application, technology etc.

Modeling self-heating effects

- Choice of electrical and thermal model
- Thermal parameters relationships, principles and assumptions

Model description

Results

Conclusions

Introduction

Purpose

- An electrical model which includes thermal behaviors of intrinsic MOS and its drift region, and represents the best compromise among accuracy, simulation time and difficulty of extraction.

Device and Process

- *n*-channel RF-LDMOS
- SOI-C-RF LDMOS 8 Technology

Application

- Power amplifier for cellular phones

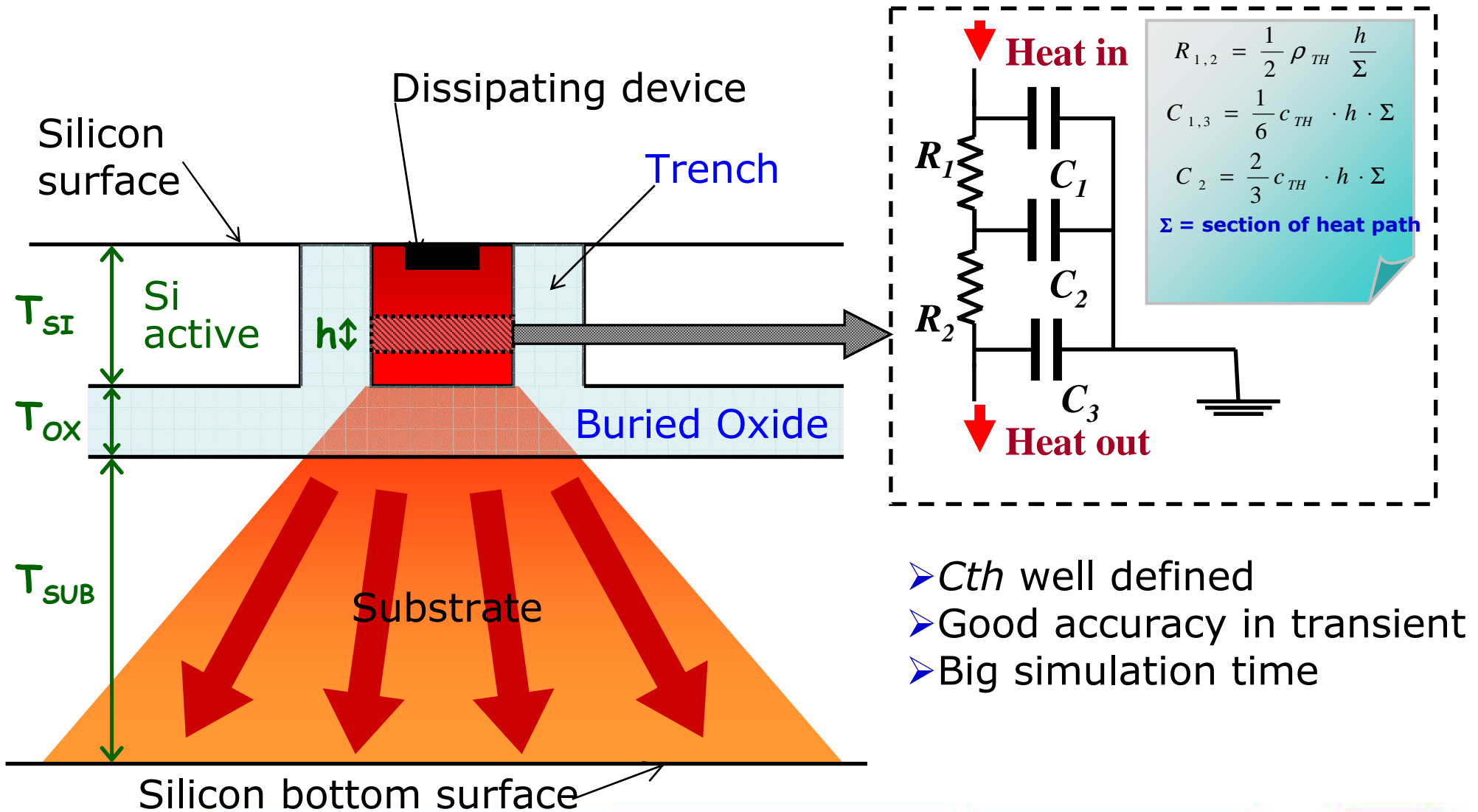
Advantages and Drawbacks for SOI Technologies

- Advantages: no parasitic effects through the substrate thanks to buried oxide (BOX). More performing devices.
- Drawbacks: Self-Heating-Effects (SHE) due to the poor thermal conductivity of buried oxide. Reduction of current capability.

Modeling Self Heating Effect

- ▣ Model for Intrinsic MOS w/ thermal node
 - Berkeley BSIMSOI
- ▣ Heat spreading model
 - 3D distributed thermal network
 - ▣ Best of Accuracy
 - ▣ Physical simulation (not our case)
 - Vertical distributed thermal network

45° heat spreading Distributed Model



Modeling Self Heating Effect/2

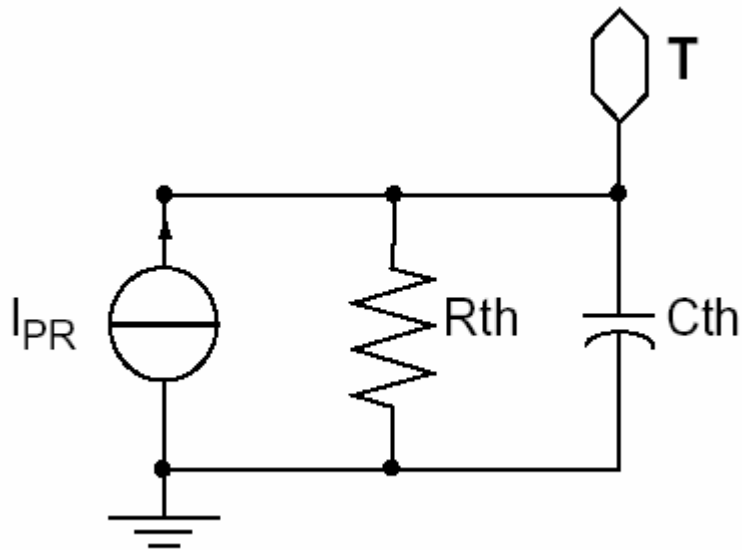
For RF application (GHz), C_{th} is insensitive

A simple thermal RC seems to be convenient:

- Advantages: Simulation time
- Drawbacks: Lower accuracy in transient simulation, not needed in RF simulation
- R_{th} can be easily calculated
 - $R_{th} = R_{th_{Si}} + R_{th_{ox}} + R_{th_{Sub}}$

Thermal Capacitance Extraction

- Based on simulations
 - Transient analysis on a power step response of a RC circuit.

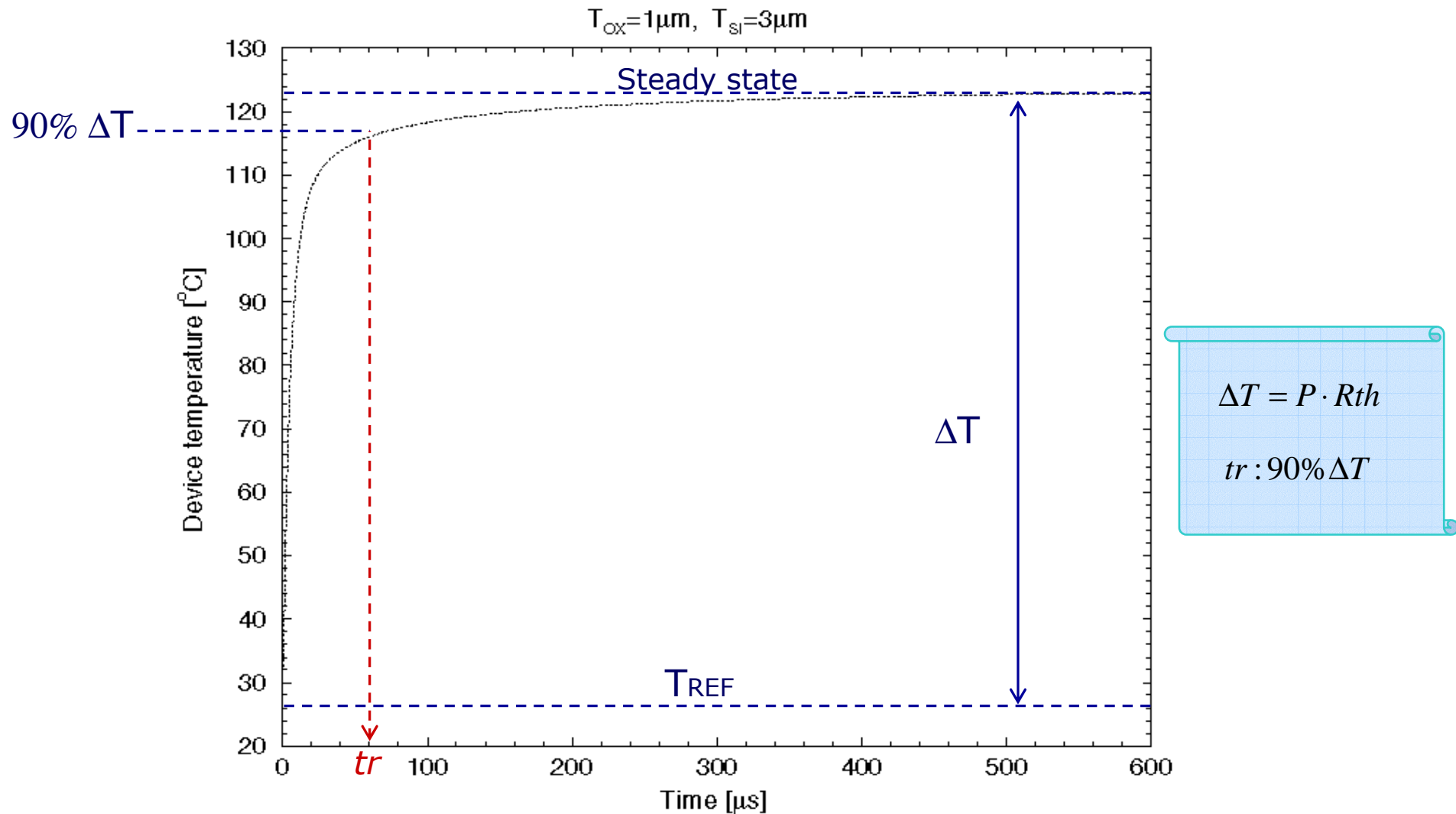


$$V(t) = P \cdot R_{th} \cdot (1 - e^{-t/\tau}) \quad [^{\circ}\text{C}]$$

$$\tau = R_{th} \cdot C_{th} \quad [\text{s}]$$

- Power generated by DMOS model:
 - I_{PR} [W]: Total dissipated power on drain/source series resistances
 - Assumption: 90% ΔT of Distributed RC is equivalent of single RC

Power Step response for a distributed thermal network



Cth Extraction/ formulae

▣ Injected power

$$I_{PR} = I_D (V_D - V_{CH}) + R_{SMET} \cdot I_S^2$$

▣ Temperature @ node T

$$V(t) = P \cdot R_{th} \cdot (1 - e^{-t/\tau}) \quad | \quad \Delta T = P \cdot R_{th}$$

▣ *tr* calculation

$$0.9 \cdot \Delta T = \Delta T \cdot (1 - e^{-tr/\tau}) \quad \left| \begin{array}{l} \tau = R_{th} \cdot C_{th} \\ tr: 90\% \Delta T \end{array} \right.$$

▣ Cth calculation

$$C_{th} = \frac{tr}{R_{th}} \cdot \ln 10 \quad \leftarrow$$

Model Scalability

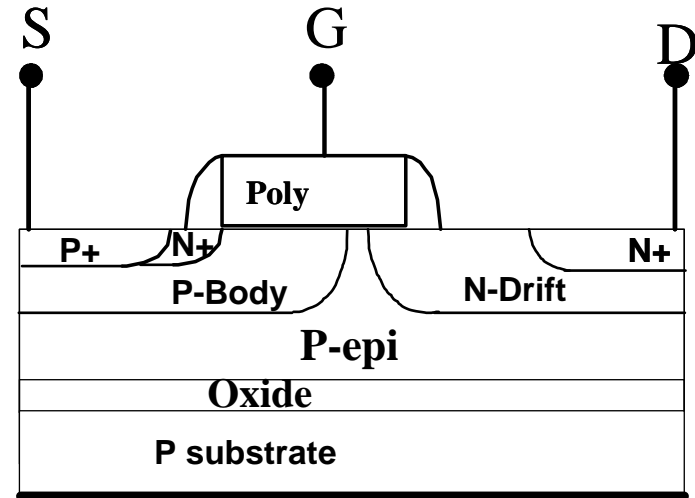
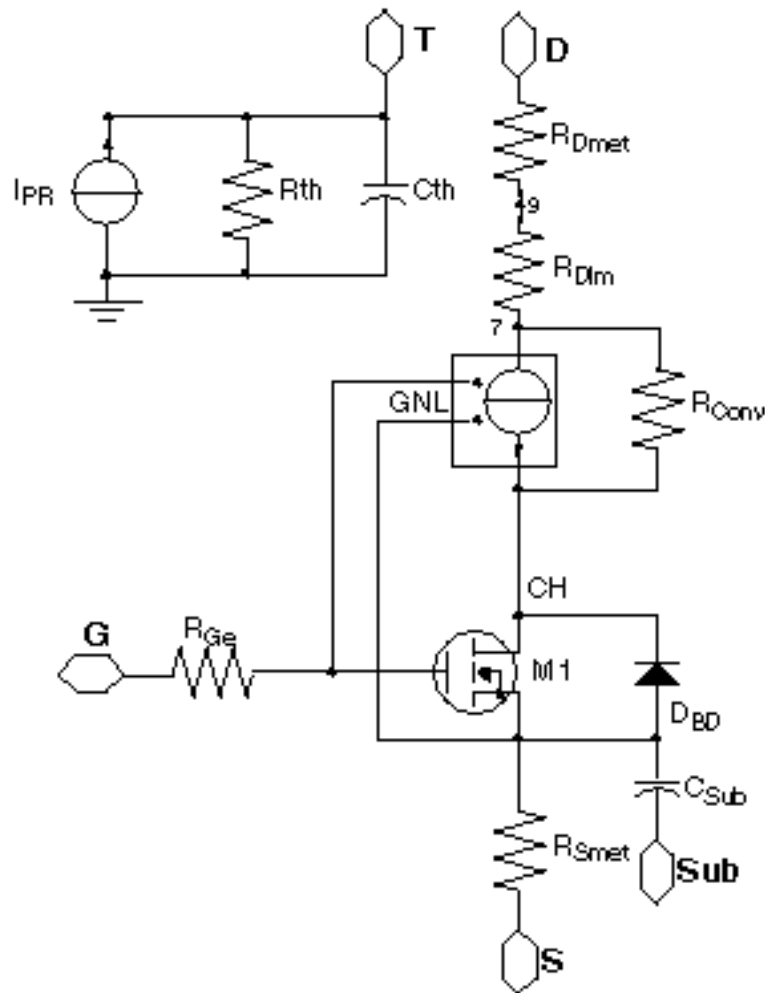
Sub circuit is composed by

- Intrinsic MOS
 - BSIMSOI -> scalable
- Drain drift resistor $f(w)$
- Metal resistors $f(w, area)$
- R_{th} $f(w, area)$
- C_{th} expression is extracted from tr vs. w fitting

$$tr = Tw_1 \cdot w + Tw_2 \cdot \left[1 - \frac{Tw_3}{\left(\frac{w}{1e-6} \right)^{xtp} + Tw_3} \right]$$

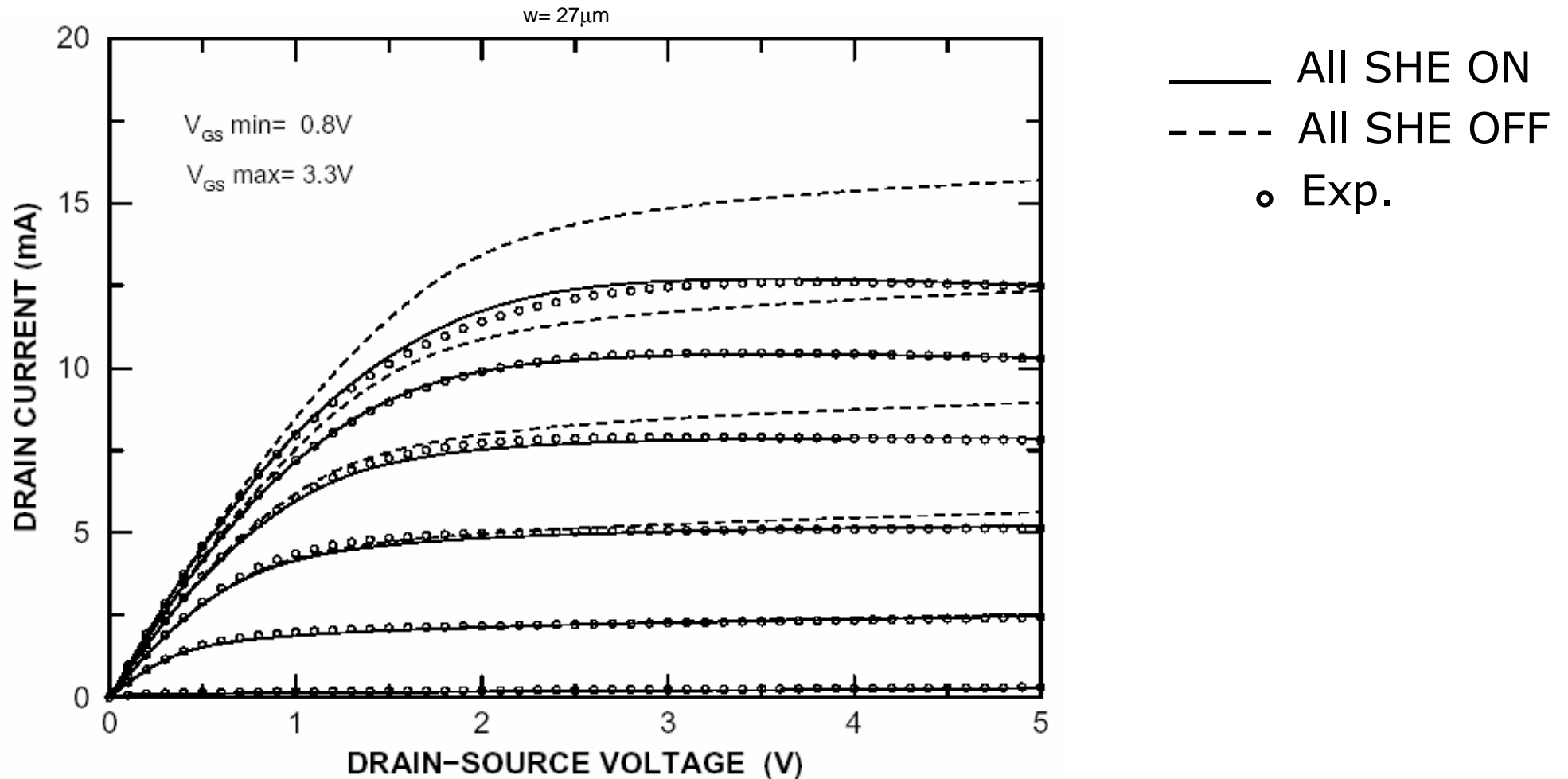
*Fitting parameters:
 Tw_1, Tw_2, Tw_3, xtp
(square device)*

SOI-C-RF LDMOS

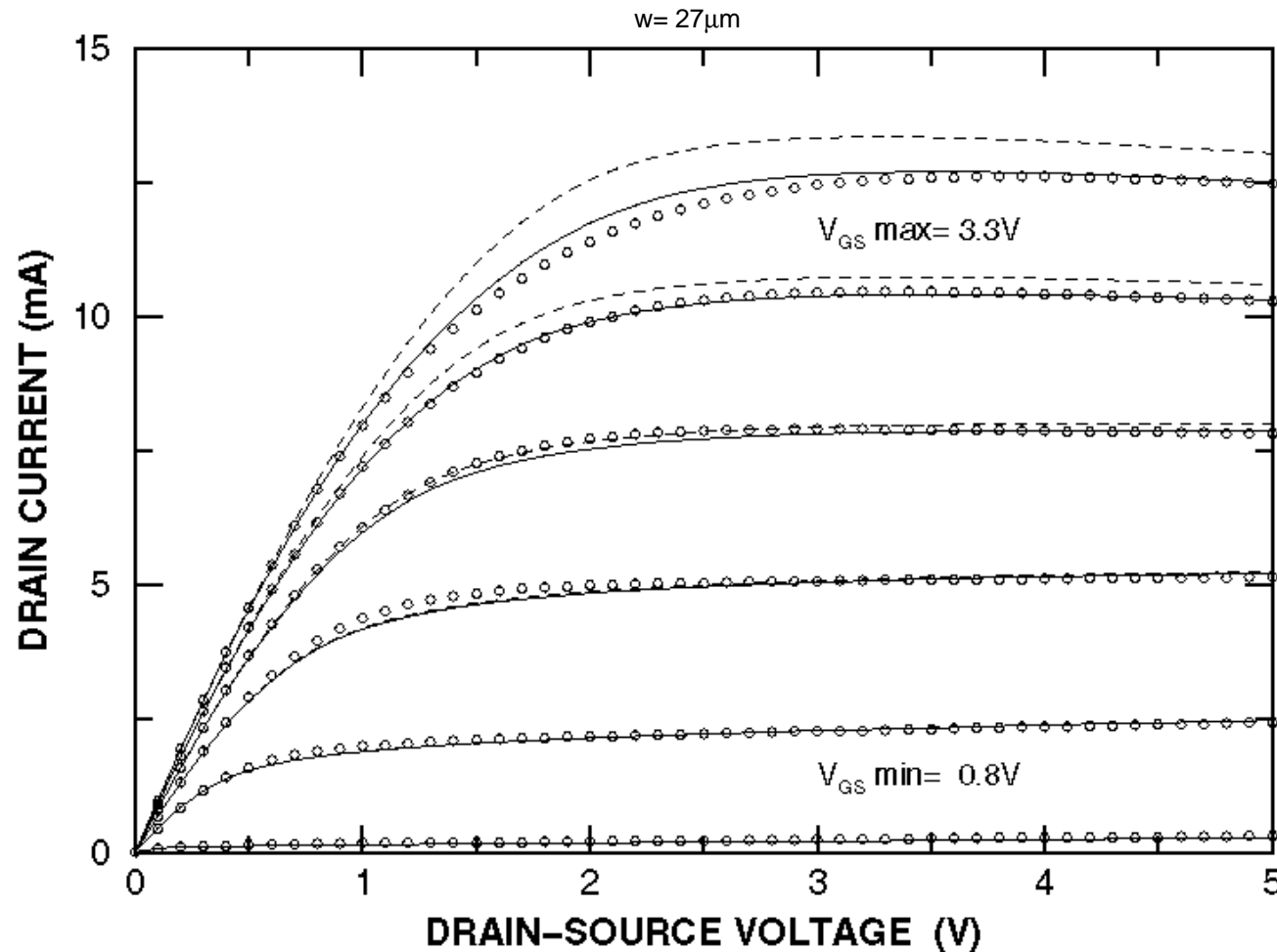


- M1: Berkeley BSIMSOI
- GNL: VCCS
 - $f(V(T), V(7-CH), V_{GS})$
- R_{Conv} : convergence Resistor
- R_{Dlm} : n^+ -layer resistance
 - $f(V(T))$
- $R_{D,Sm\text{et}}$: metal pattern resistance
 - $f(\text{layout parameters})$
- R_{Ge} : Poly-Gate resistance
- D_{BD} : Body-Drain diode

SHE Effects simulation comparison

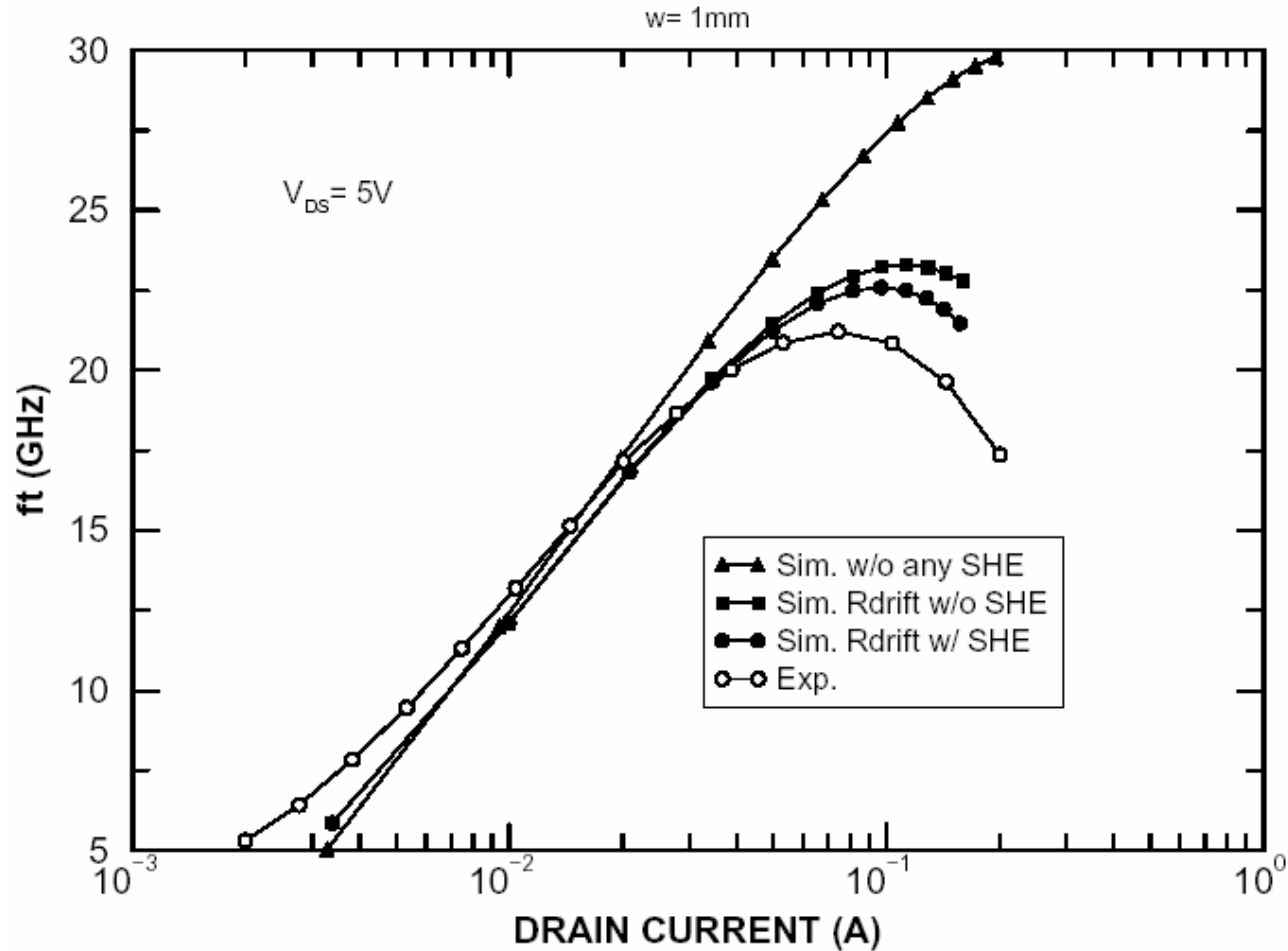


Drain Rdrift w/ and w/o SHE



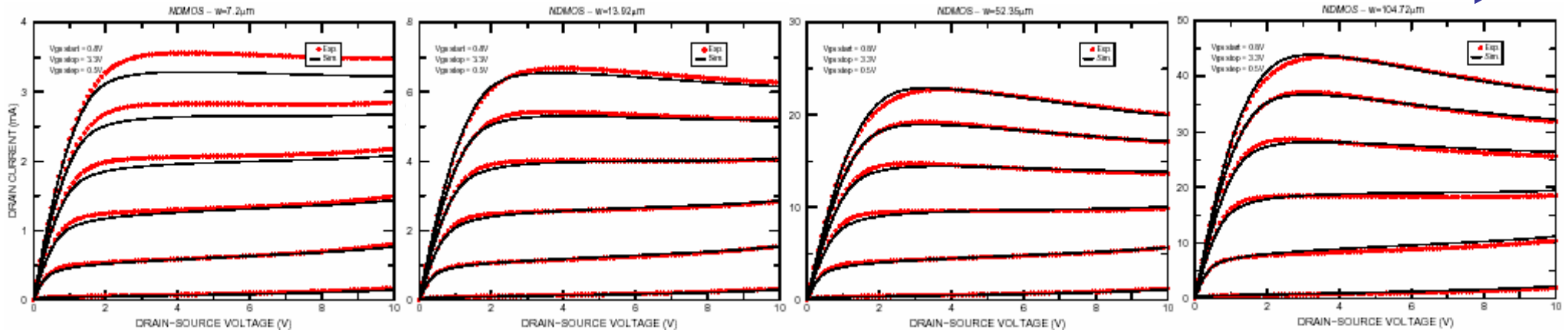
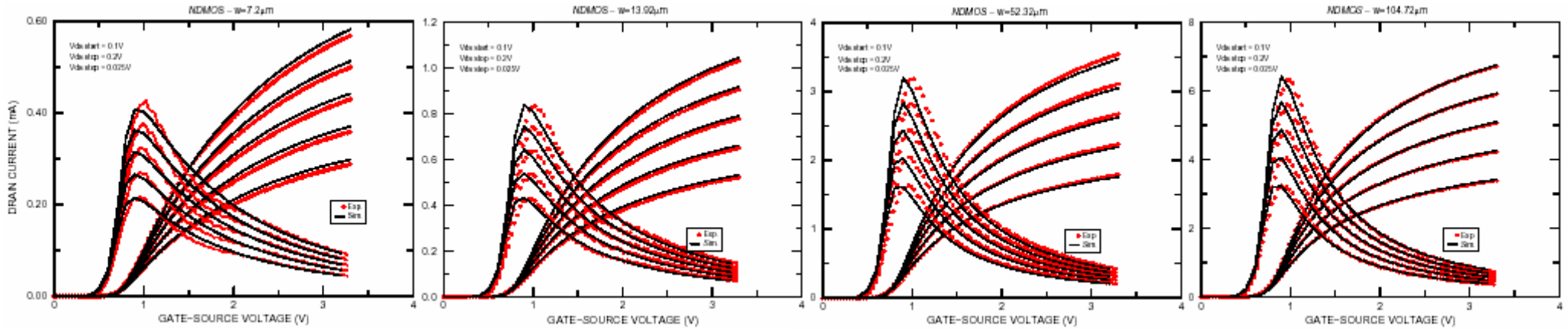
- Rdrift w/o SHE
- All SHE ON
- Exp.

SHE on RF simulation performances



Model Scalability Accuracy

— Sim.
 ● Exp.



Conclusions

- ❏ A fully scalable electrical model which takes into account self heating effects of a LDMOS has been extracted.
- ❏ The thermal effects of the resistance of drain drift region have been modeled and successfully included in the model.
- ❏ The presented approach on extracting an electrical model which take into account SHE by mean of a simple RC is very satisfying thanks to the results obtained in terms of accuracy and scalability.

References

- ❏ A. Moscatelli, C. Contiero, P. Galbiati and C. Raffaglio, "A 12V Complementary RF LDMOS Technology Developed on a 0.18mm CMOS Platform", ISPSD '04 Proceedings, Kitakyushu, Japan, May 2004, pp 37-40
- ❏ C. Angel, R. Gillon, and A.M. Ionescu, "Self-heating Characterization and Extraction Method for Thermal Resistance and Capacitance in HV MOSFETs", IEEE Electron Device Letters, Vol. 25, No.3, March 2004, pp. 141-143
- ❏ L. Labate, A. Moscatelli, R. Stella, "Robust and performing RF LDMOS Device Integrated in a VLSI BCD Silicon Technology", 2003 IEEE RFIC Symposium, Philadelphia, PA, USA, June 2003. pp. 159-162.
- ❏ On line documentation:
 - www-device.eecs.berkeley.edu/~bsimsoi/