UNIVERSITAT ROVIRA I VIRGILI

DEEEA
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COMPACT I-V MODEL FOR AMORPHOUS OXIDE TFTs

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OUTLINE

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1. Introduction

· AOS TFTs

The large scale manufacturing of a-Si:H TFTs forms the basis of the active matrix flat panel display industry. Poly-Si TFTs facilitate the integration of electronic circuits into portable active matrix liquid crystal displays, and are increasingly used in active matrix organic light emitting diode (AMOLED) displays for smart phones.

The recently developed ***Amorphous Oxide Semiconductor Thin Film Transistors (AOS-TFTs)*** have received much attention since are seen as an alternative option to poly-Si and a-Si:H for AMOLED TV and large AMLCD TV applications, respectively.

- ✓ **High mobility**
- ✓ **High on/off ratio**
- ✓ **Low processing temperatures**
- ✓ **Possibility of fabrication on large areas and flexible substrates**

1. Introduction

Among AOS materials, amorphous In-Ga-Zn-O (a-GIZO) and more recently Hf-In-Zn-O (HIZO) TFTs have been systematically studied.

However, they need to be well understood and optimized since problems in these transistors are present, such as:

- Problems related to the stability with bias.
- Temperature and illumination effects.

In some cases, a parallel displacement of the transfer curves is observed, while in others, a hump or deformation on the curve appears after DC bias stress.

Another pending task is the development of models suitable for designing with these transistors, which are frequently described using the same expressions as for MOS transistors

1. Introduction

· Objective

In this work we present MOTFT, a compact model for AOS TFTs valid also for GIZO and HIZO devices with and without gate bias-stress effect (**hump**).

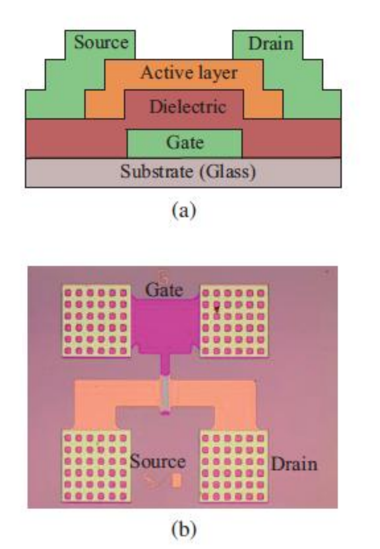
It is based on the Unified Model and Extraction Method (UMEM) [*], which has been adapted to different types of TFTs.

We present the MOTFT Verilog-A code implementation in Electronic Design Automation tools (EDA). It is shown that a good agreement is obtained with experimental data.

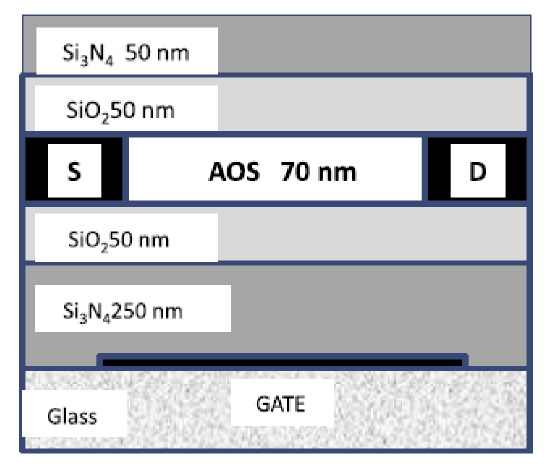
[*]
-A. Cerdeira, M. Estrada, R. Garcia, A. Ortiz-Conde, and F.J.G. Sanchez, *Solid-St. Electron*, vol.45, no. 7, pp.1077-1080 (2001).
-M. Estrada, I.Mejía, A. Cerdeira, J. Pallarès, L. F. Marsal, and B. Iñiguez, *Solid-State Electron.*, vol.52, no.5, pp.787–794, (2008).

2. Experimental and simulation tasks

Experimental data were obtained and device simulation was performed in Silvaco ATLAS were used to validate the model.



(a) a-GIZO TFT structure
(b) Fabricated device [*].



AOS TFT cross section used in simulations [**]

The active layer is n-type, with impurity concentration NB=1×10^{16} cm^3

[*] G. Bahubalindruni, et al. 20th Telecommunications forum TELFOR 2012, Serbia Belgrade.
[**] M. Estrada, A. Cerdeira, B. iñiguez, Microelectron Reliab 52, pp.1342-5 (2012).

3. AOS TFT model

· UMEM

Unified Model and Parameter Extraction Method (UMEM) where the mobility is calculated by solving:

- Poisson's equation assuming an exponential DOS and Qfree<<Qloc
- Free carrier transport in AOS TFTs

Multiple Trapping and Release

Estrada, M., Cerdeira, A., Puigdolers, J., et al.: 'Accurate modeling and parameter extraction method for organic OTFTs', Solid-State Electron., 2005, 49, (6), pp. 1009–1016.

M.Estrada, I.Mejía, A.Cerdeira, J.Pallares,L.F.Marsal, B.Iñiguez; "Mobility model for OTFTs made of different materials" *Sol State Electron*, 52(2008)787-794

M. Shur and M. Hack, "Physics of amorphous silicon based alloy field-effect transistors", *J. Appl. Phys.*, vol. 55, pp. 3831 (1984).

3. AOS TFT model

· Above Threshold

ABOVE THRESHOLD

Channel length modulation

$$I_{ds} = \mu_{FET} C_i \frac{W}{L} \frac{(V_{GT})(1+\lambda V_{DS})V_{DS}}{\left[1+\left(\frac{V_{DS}}{\alpha_{sat} V_{GT}}\right)^{m}\right]^{1/m}}$$

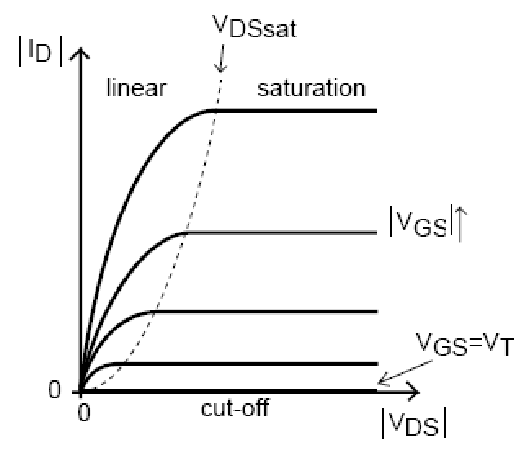
Saturation parameter

Sharpness of the knee region

where

Empirical parameters defining the variation of mobility with Vgs above threshold

$$\mu_{FET} = \mu_0 \frac{(V_{GS}-V_T)^{\gamma_a}}{V_{aa}^{\gamma_a}}$$



3. AOS TFT DC model

· Above Threshold

In [*] extraction procedure based on the properties of the integral function *H(VGS).* was developed and applied, first, to a-Si:H devices model :

$$H_{above}(V_{GS}) = \frac{\int_0^{V_{GS}} I_D(V_{GS})\,dV_{GS}}{I_D(V_{GS})} = \frac{1}{2+\gamma a}(V_{GS}$$

Parameters extracted from the transfer curve in linear regime, and with the ***slope*** and the abscissa intercept of the H function.

$$Va = \left(\frac{\frac{W}{L} C_i V_{D1}}{slope^{1+\gamma a}}\right)^{\frac{1}{\gamma a}}$$

→ Now we can model the field dependent mobility μ_{FET}

Subsequently, parameters R, m, λ, α are extracted as indicated in:

-A. Cerdeira, M. Estrada, R. Garcia, A. Ortiz-Conde, and F.J.G. Sanchez, *Solid-St. Electron*, vol.45, no. 7, pp.1077-1080 (2001).

3. AOS TFT model

· Subthreshold

SUBTHRESHOLD

To model the subthreshold region of devices, the drain current can be described as [*]:

$$I_{bt}(V_{GS}, V_{DS1}) = K \frac{(V_{GS} - V_{FB})^{1+\gamma_b}}{{V_{bb}}^{\gamma_b}} V_{DS1}$$

γ_b depends on the temperature T and on the characteristic temperature of the deep states distribution (T_2)

$$\gamma b = \frac{2T_2}{T} - 2$$

Vbb is obtained as indicated in [**]

[*] L. Resendiz, M. Estrada, and A. Cerdeira, *Solid State Electron* 2003;47:135–1358.
[**] A. Cerdeira, M. Estrada, B. S. Soto-Cruz, and B. Iñíguez, *Microelectron Reliab* vol. 52, pp.2532-2536 (2012).

3. AOS TFT model

· Distribution of localized states in the mobility band

Distribution of acceptor type traps

Conduction band energy

$$g_a(E) = g_{ta}\exp\left(\frac{E-E_C}{kT_1}\right) + g_{da}\exp\left(\frac{E-E_C}{kT_2}\right)$$

$$T_1 = \frac{(\gamma_a+2)}{2}T$$

Tail acceptor density of states

Deep acceptor density of states

$$T_2 = \frac{(\gamma_b+2)}{2}T$$

The V_{GS} variation above threshold modifies the population of the tail states.

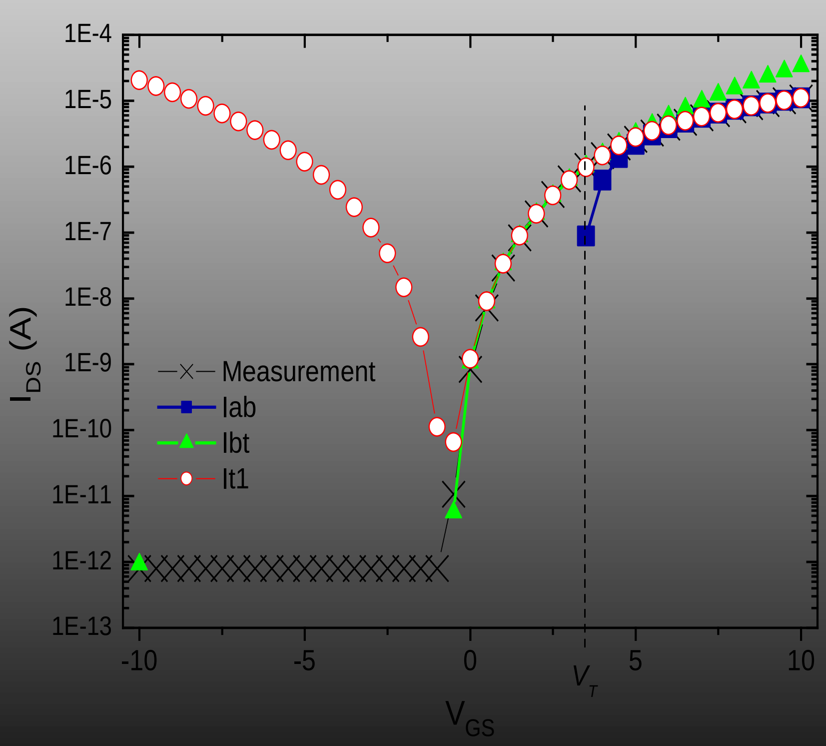
The V_{GS} variation in subthreshold modifies the population of the deep states.

3. AOS TFT model

· Subthreshold and above Threshold regions

To join the subthreshold and the above threshold regions, an expression I_{t1} is obtained where the *tanh* function is applied to sew $I_{ab}(V_{GS}, V_{DS})$ and $I_{bt}(V_{GS}, V_{DS})$.

$$I_{t1} = |I_{bt}| \left[\frac{1-\tanh\left[\left(V_{GS}-(hi+V_0)\right)Q_0\right]}{2}\right] + |I_{at}| \left[\frac{1+\tanh\left[\left(V_{GS}-(hi+V_0)\right)Q_0\right]}{2}\right]$$



Typical non-stress transfer characteristic of a HIZO TFT in linear regime.

W=160 µm, L=20 µm, V_{DS}=0.1 V

Experimental data is compared with I_{t1}, which is composed of the above threshold region ($V_{GS} > V_T$), modeled by *Iab*, and the subthreshold region, modeled by *Ibt*.

3. AOS TFT model

· Deep subthreshold

DEEP SUBTHRESHOLD

Well below V_T, in deep subthreshold regime where I_{t1} can no longer model the drain current, diffusion becomes the predominant charge transport mechanism and the current shows an exponential dependence with the gate voltage for V_{GS} which can be expressed as [*]:

$$I_{s1} = I_{bt}(V_{GS}, V_{DS1})e^{\frac{V_{GS}-(V_{FB}+V_1)}{S1}2.3}$$

The region where a hump may be present in stressed devices corresponds to a part of the deep subthreshold region where the slope is different due to the presence of the back interface charges, can be represented by another exponential behavior with an inverse slope S_2

$$I_{s2} = I_{bt}(V_{FB}+V_2, V_{DS1})e^{\frac{V_{GS}-(V_{FB}+V_2)}{S2}2.3}$$

where $(V_{FB} + V_2)$ is the gate voltage below V_T where the **hump starts.**

[*] A. Cerdeira, M. Estrada, B. S. Soto-Cruz, and B. Iñíguez, *Microelectron Reliab* vol. 52, pp.2532-2536 (2012).

3. AOS TFT model

· Deep subthreshold

To sew the deep subthreshold region (I_{s1}) and the hump (I_{s2}), an expression I_{snl} is used

$$I_{snl} = I_{s2l} + \frac{1}{2}\left[(I_{s1l} \cdot hump - I_{s2l} - u) - \sqrt{[I_{s1l} \cdot hump - I_{s2l} - u]^2 - 4uI_{s2l}}\right] = ln(I_{snl})$$

And then an expression ***It2*** will describe the entire subthreshold region by joining the subthreshold (***Ibt***) and the deep subthreshold (***Isnl***)

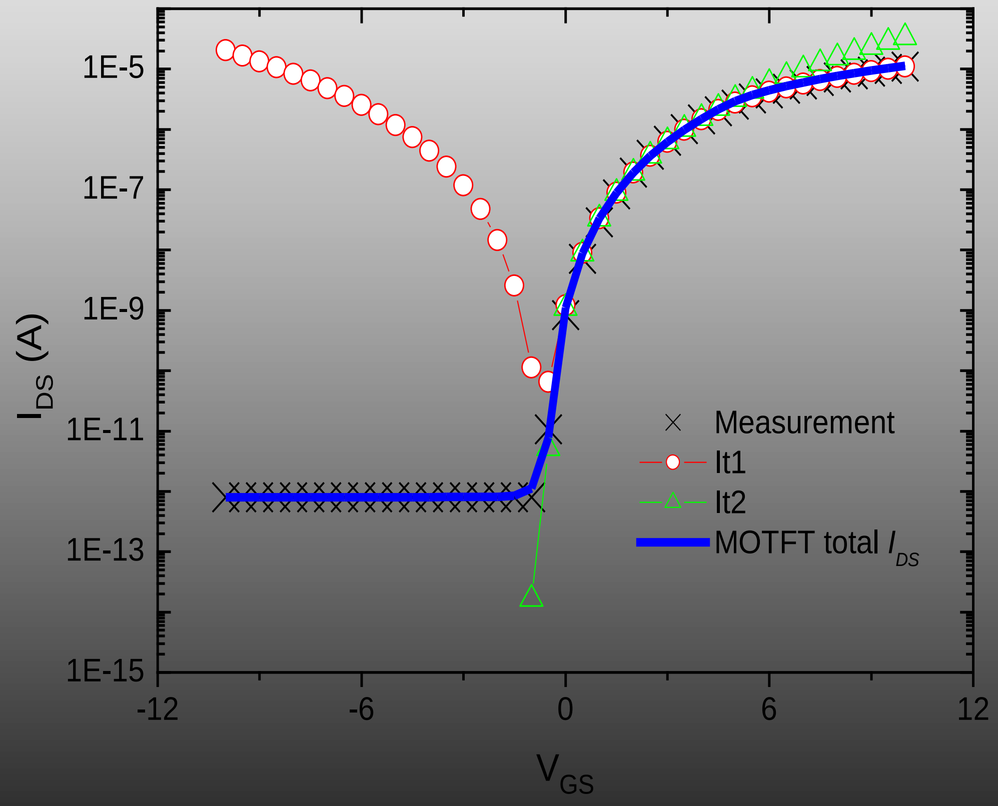
$$I_{t2} = |I_{sn}|\left[\frac{1 - tanh\left[\left(V_{GS} - (V_{FB} + V_2)\right)Q_1\right]}{2}\right] + |I_{bt}|\left[\frac{1 + tanh\left[\left(V_{GS} - \left(V_{fb} + V_2\right)\right)Q_1\right]}{2}\right]$$

3. AOS TFT model

· Deep subthreshold

Finally an expression to describe the total I_{DS} is obtained

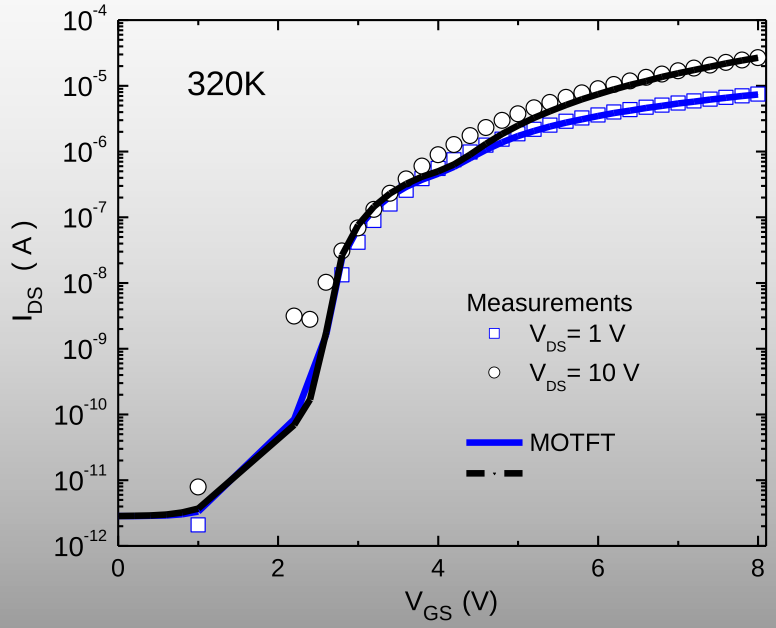
$$I_{DS} = \pm \left[|I_0| + |I_{t2}| \left[\frac{1 - tanh[(V_{GS} - (V_T + V_0))Q_0]}{2} \right] + |I_{t1}| \left[\frac{1 + tanh[(V_{GS} - (V_T + V_0))Q_0]}{2} \right] \right]$$

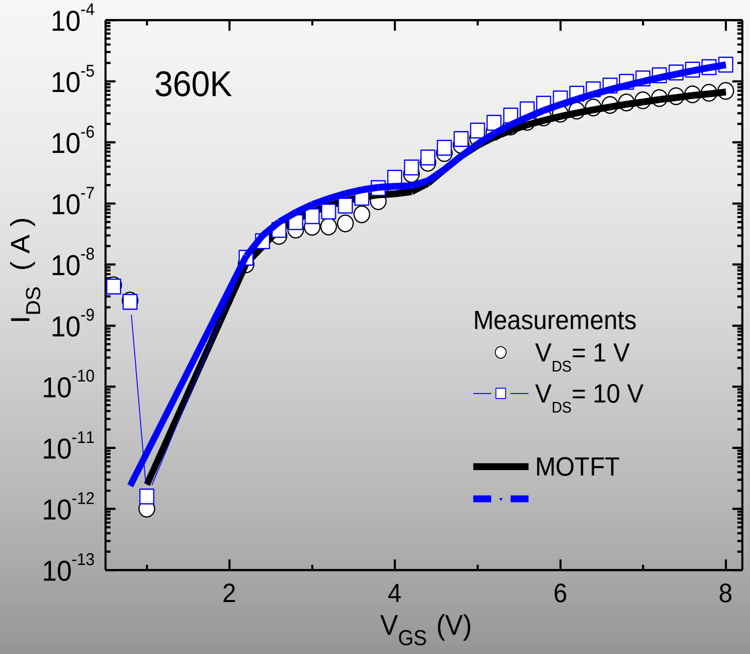


Non-stressed transfer characteristic of a HIZO TFT in linear regime (V_{DS}=0.1 V) modeled by MOTFT.

3. AOS TFT model

· Temperature dependence





γ_a and γ_b decrease with increasing T

T2 still increases with increasing T

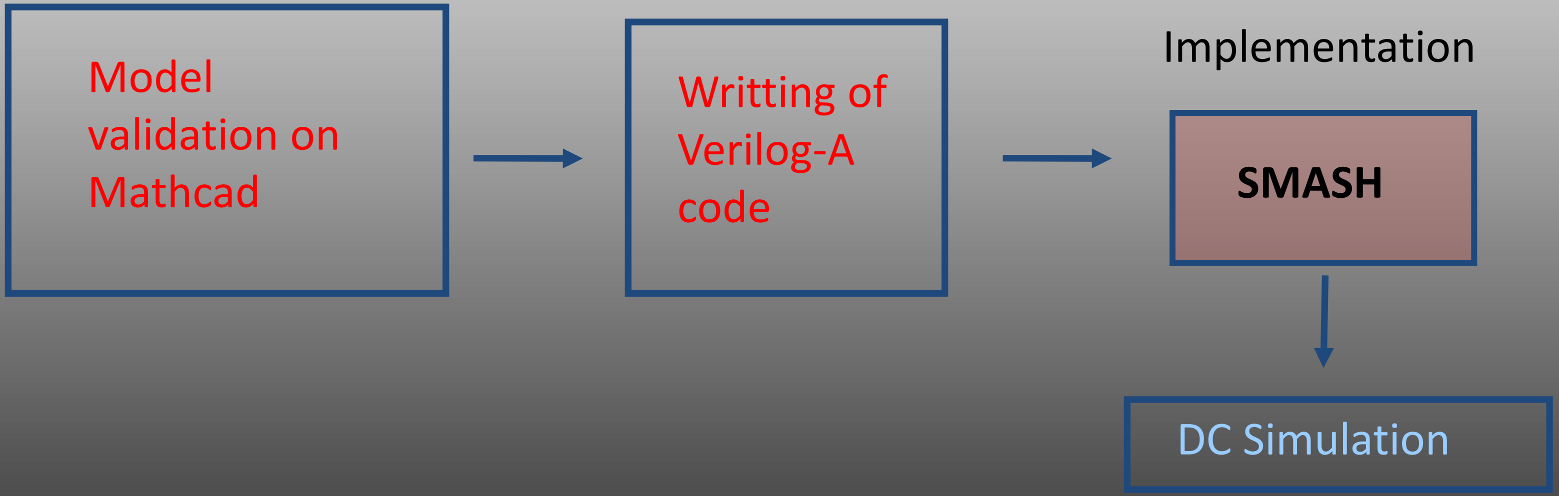
VT increases linearly with increasing T

GIZO TFT W=160 µm L=20 µm

4. Implementation of UBCM in EDA tools

SMASH (from DOLPHIN) is an all-in-one mixed signal, mullti level, multi-language simulator.

Mixed Signal → Analog and continuous signal and discrete-logic signals



Model validation on Mathcad

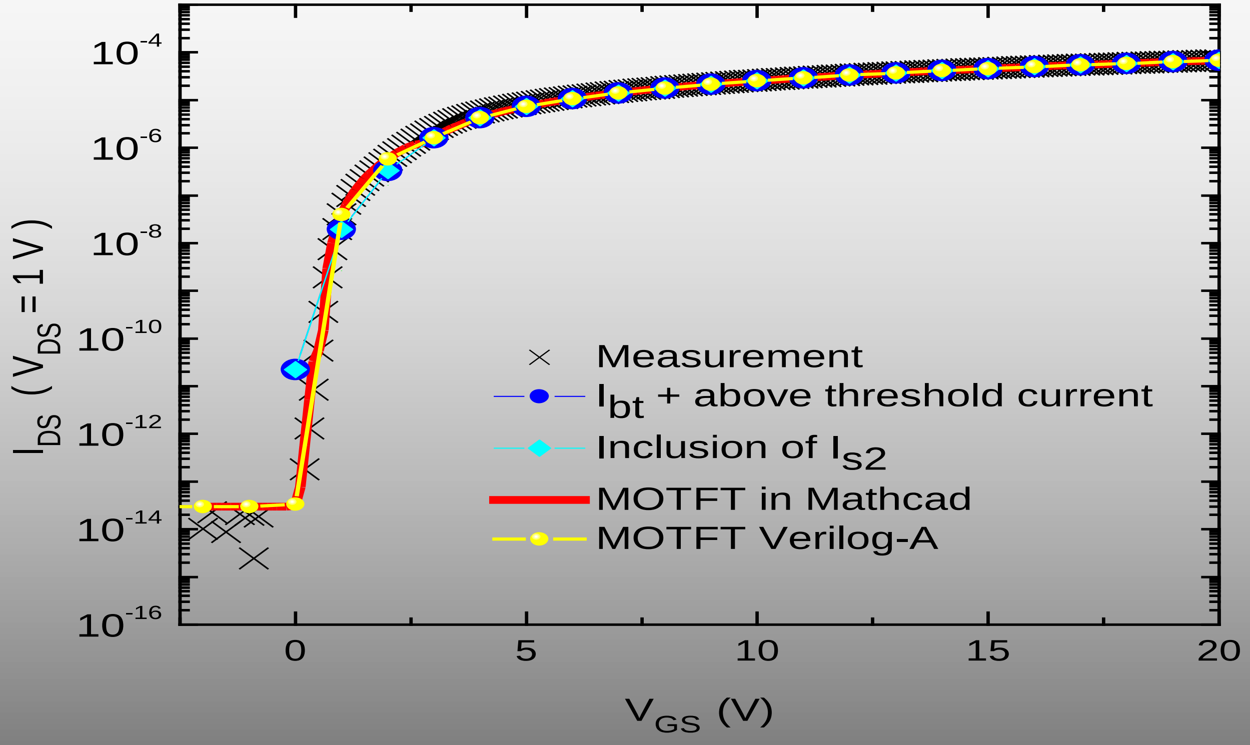
Writting of Verilog-A code

Implementation

SMASH

DC Simulation

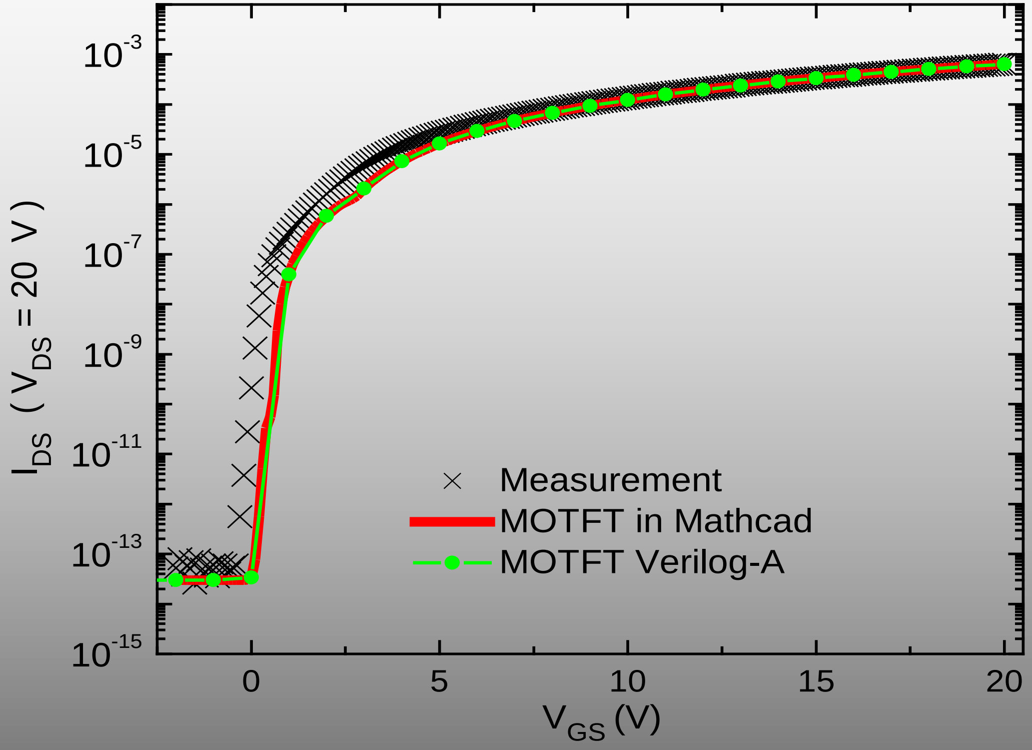
4. Implementation of UBCM in EDA tools



GIZO TFT W=160 µm L=20 µm Vds=1 V

4. Implementation of UBCM in EDA tools

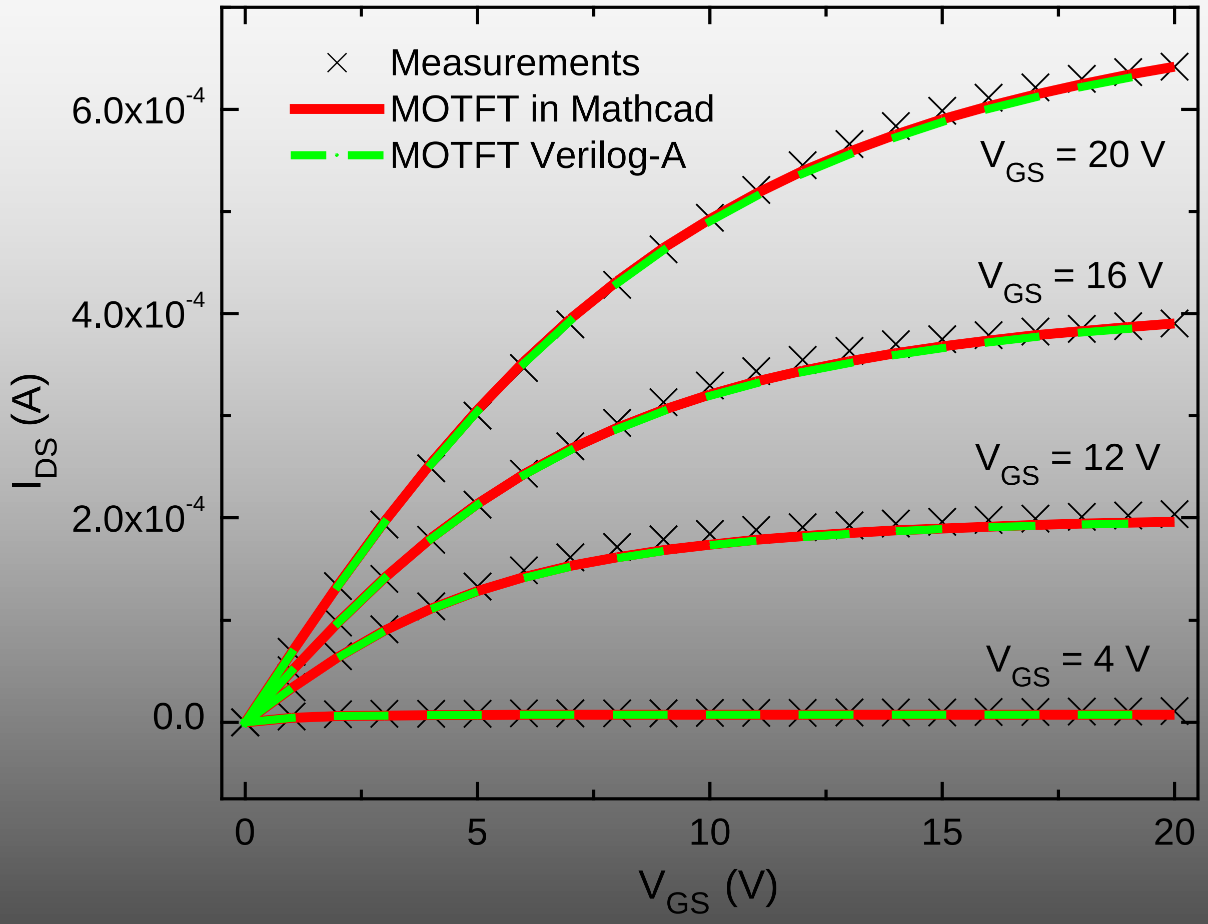
- SMASH



GIZO TFT W=160 µm L=20 µm Vds=20 V

4. Implementation of UBCM in EDA tools

- SMASH



GIZO TFT W=160 µm L=20 µm

5. Conclusions

MOTFT, the UMEM-based compact model for amorphous oxide semiconductor TFTs is used to model the drain-to-source current of GIZO and HIZO TFTs.

These devices might show typically a gate bias-stressed hump in their transfer characteristics which can be modeled by MOTFT.

For validation, experimental transfer and output characteristics of GIZO and HIZO TFT was compared with MOTFT, showing a good agreement even at different temperatures, which makes it useful for circuit design applications.

We implemented the MOTFT Verilog-A code in Electronic Design Automation tools (EDA) and it is shown that a good agreement is obtained with experimental data.

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