Modeling of Passive CMOS Components

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Outline

- Motivation
- CMC R3 Model and Extraction
- Modeling of Capacitors
- Selected Topics
- Summary

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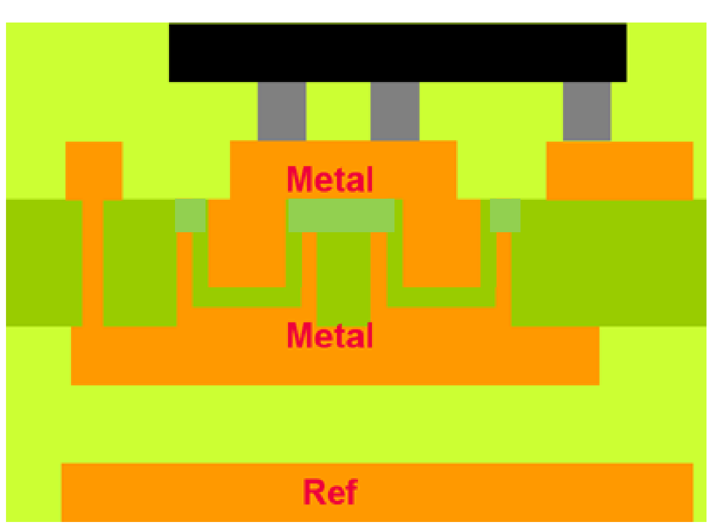
Motivation: Why are Passives so important ?

- Reducing the BOM–List (external component => integrated)
- After the digital shrink => the Analog will remain
- „More than Moore“ (3d, customized technologies, extended T-Profile)
- Key building components
  for Bandgaps, OPAMPs
  and other



Lit(1)

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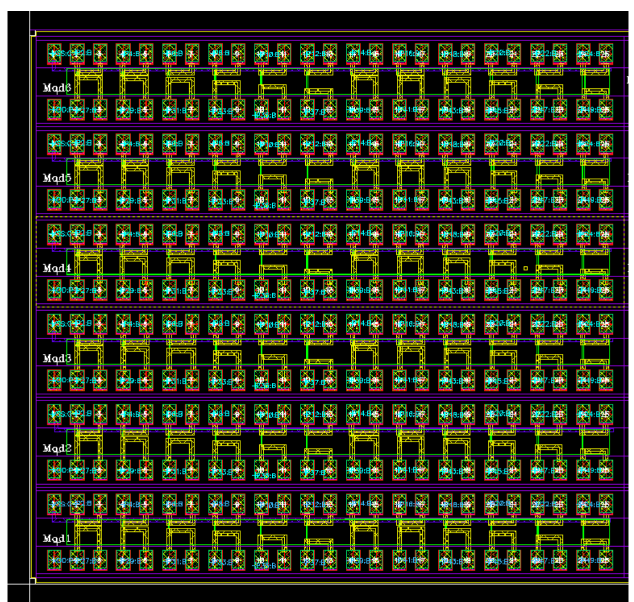
CMC R3 Model

- $I(V, V_c) = G(V, V_c)\, V$

$$G = \frac{1 - df\sqrt{d_p - 2V_c + V}}{r_\mu\, R_0 (1 - df\sqrt{d_p})}$$

d_f effective depletion pinching factor
r_μ effective μ reduction factor
d_p effective depletion potential
R_0 Zero bias resistance
V applied resistor voltage
V_c voltage resistor body to substrate

Lit(2)



130 nm Node Testchip-Layout

CMC 3 Model incorporates :

- self heating
- velocity saturation
- depletion pinching

$= f(W, L, V, V_c, T, \text{thickness})$

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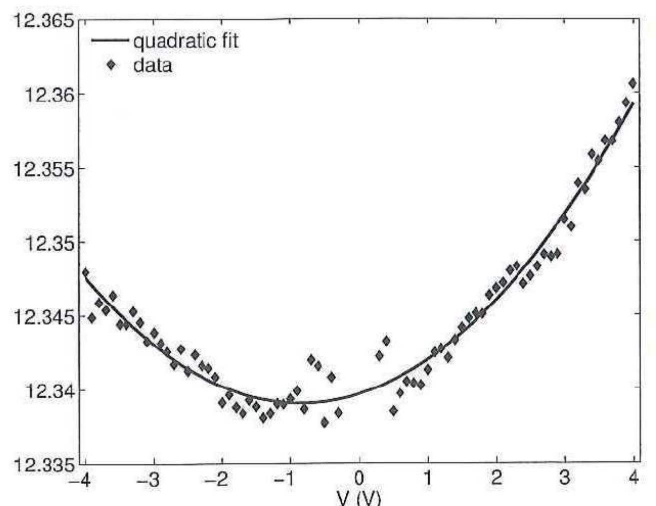
CMC R3 Model Extraction for Poly resistors



Lit(3)

$$\frac{1}{G}\left(\frac{\partial G}{\partial V}\right) \approx -\frac{d_f}{2\sqrt{d_p}}$$

1. With assumption : Highly linear & $V\text{-}2V_c \ll d_p$

2. For poly resistors with thick dielectric layer on substrate we can conclude (see Lit.(2)):

$$d_f\sqrt{d_p} = \frac{1}{1+\frac{t_b \varepsilon_{ox}}{t_{ox}\varepsilon_s}}$$

Thermal resistance R_{TH} can be calculated from:

$$\frac{G(Vr,0)}{G(0,0)} = 1 - \frac{T_{C1} R_{TH} W L}{R_{sh}} \left(\frac{V_r}{L}\right)^2$$

T_{C1} : 1st resistor body TC
R_{sh} : Resistor sheet resistance

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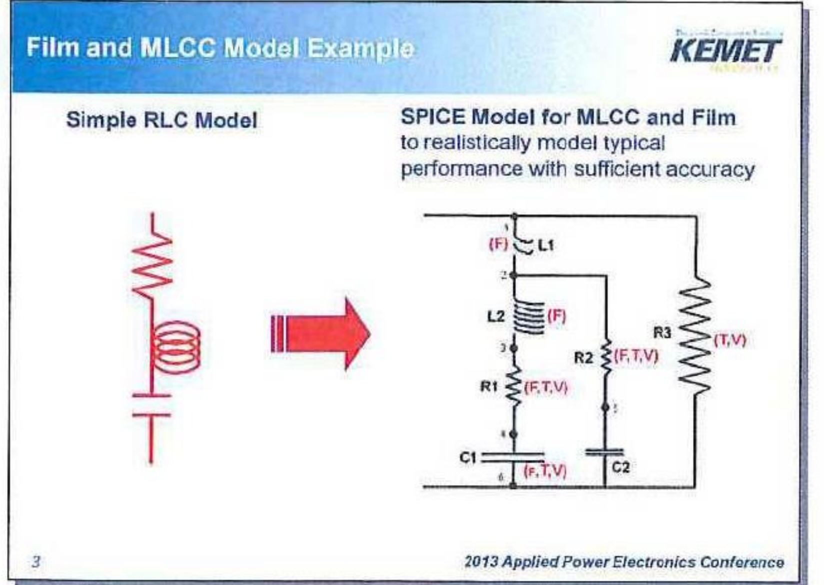
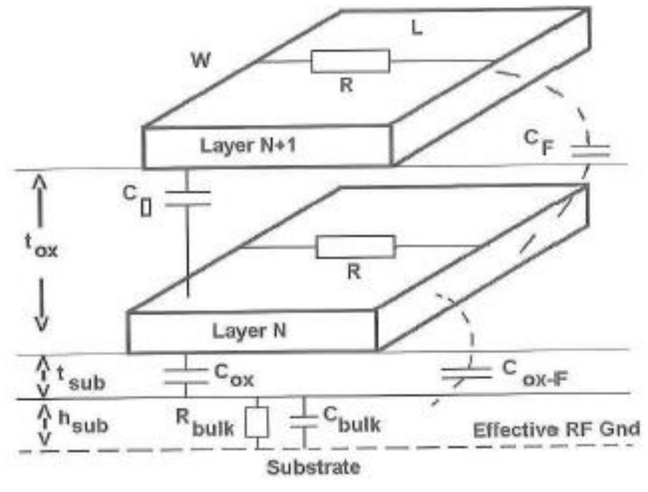
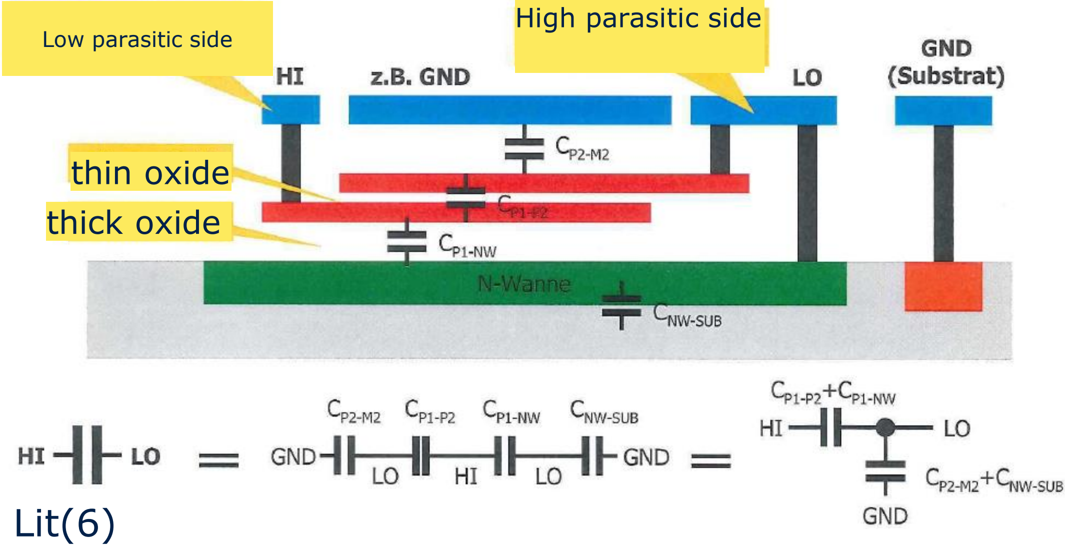
Modeling of Capacitors : example





$C_{tot}=WLC_{\square}+2(W+L)C_F$ Lit(5)

A „simple“ passive component
but fixed size
therefore not scalable
Lit(4)



Lit(6)

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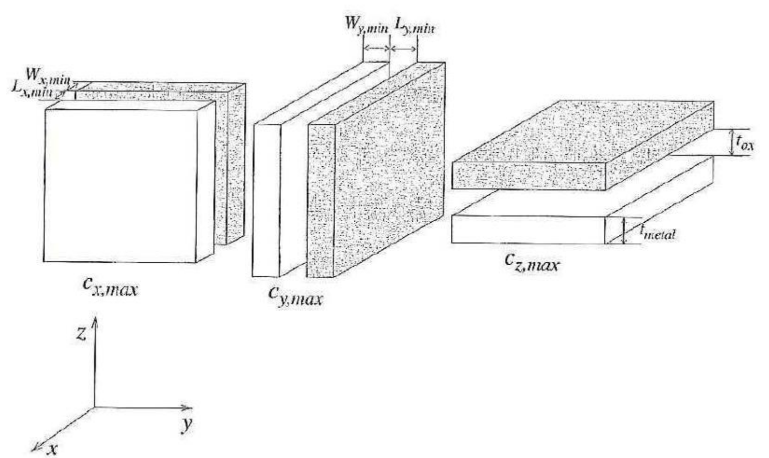
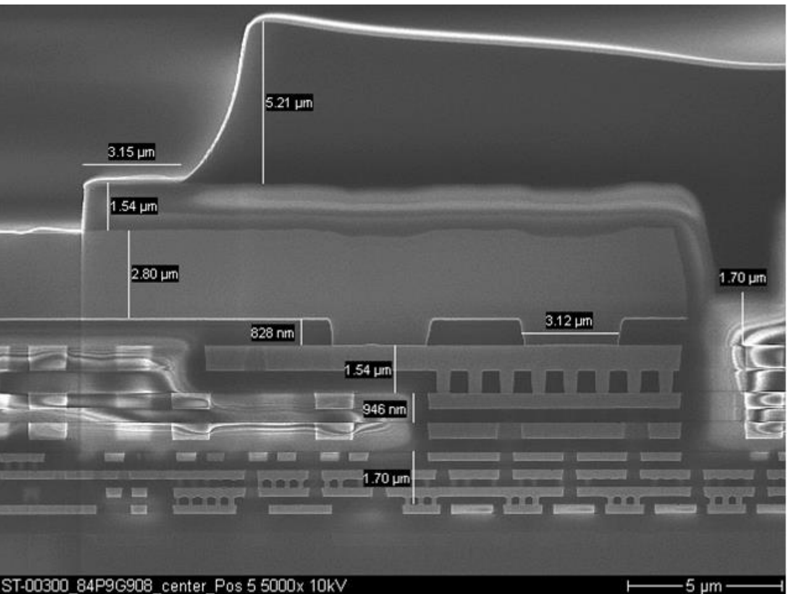
BEOL capacitors in newer nodes





Theoretical maximum capacity
density of parallel plates is given by (Lit.7) :

$$c_{max}=\varepsilon_r\varepsilon_0\left[\frac{2}{L_{min}(Lmin+Wmin)}+\frac{1}{t_{ox}(tox+tmetal)}\right]$$

Trend towards:
-VPP Caps
-Wire Caps

Known Issues:

- Designrules/Manufacturing
- Trends towards low k
- Reliability issues

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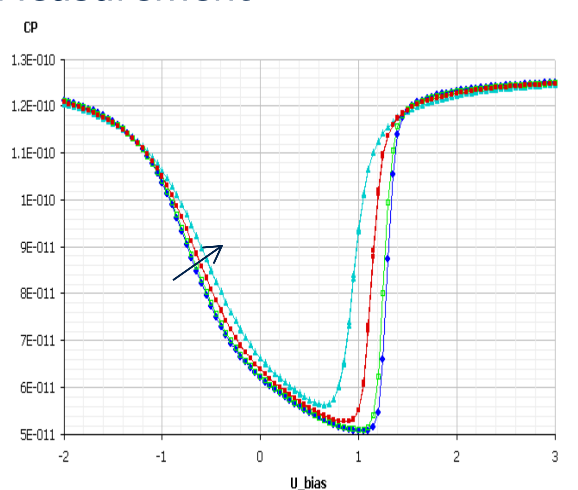
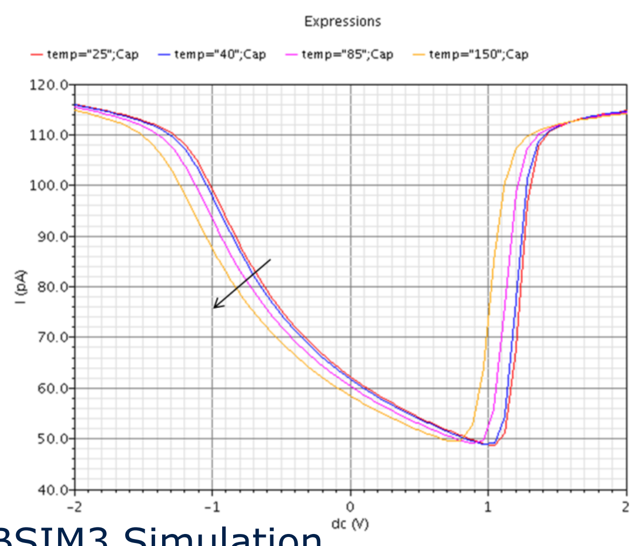
Selected Topic:
BSIM3 can‘t cover TC‘s of MOSCAPs



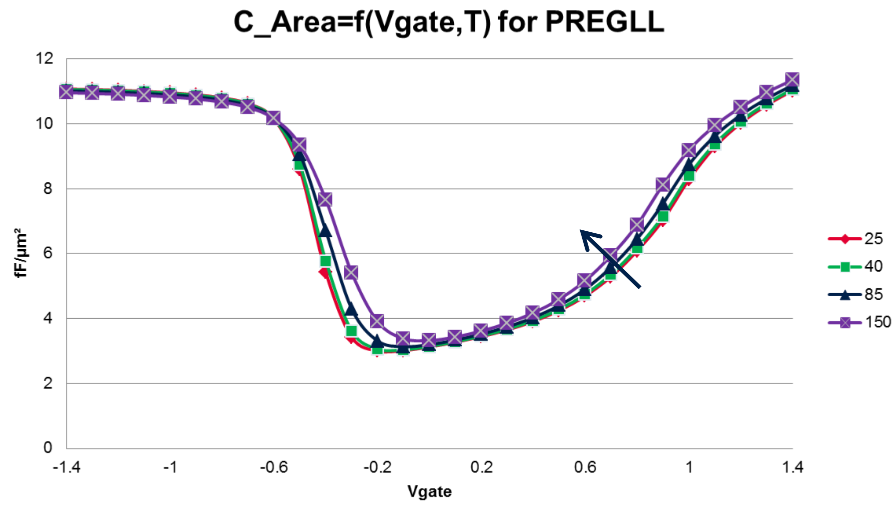
Measurements : - VFB ↗ T ↗
- VTH ↘ T ↗

BSIM3 has only TCs for VTH (kt1, kt1l) and none for VFB
BSIM4 provides TCs for both voltages (Lit.8)

=>BSIM 3 can‘t cover TC‘s in accumulation



BSIM3 Simulation



BSIM4 Simulation

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Selected Topic: Cu Wire Interconnect Resistance in 65 nm and smaller nodes

- Electron mean free path ~ 40 nm
- Wire dimensions in newer nodes approaching this value

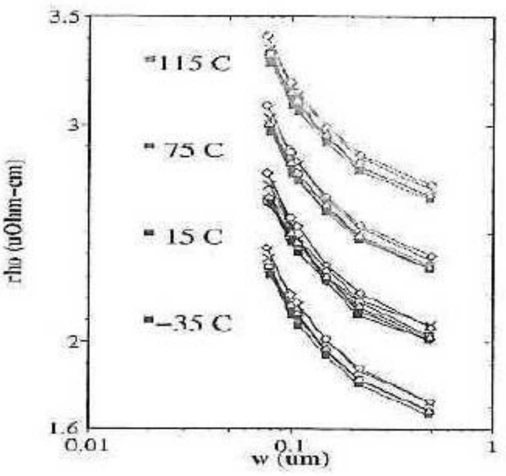

Fig. 6. Measured Cu wire resistivity for M1 (testsite 1).

Effects which play a role :

- Surface roughness
- Scattering
  - Surface
  - Grain boundary

$$R(T) = \rho(T)\frac{L}{wh}$$

$$\rho(T)=\rho_0\left(1+t_{cr\text{—}bulk}(T)(T-T0)+\frac{a}{w}+\frac{\beta}{h}+\frac{b}{wh}\right)$$

(Lit.9)

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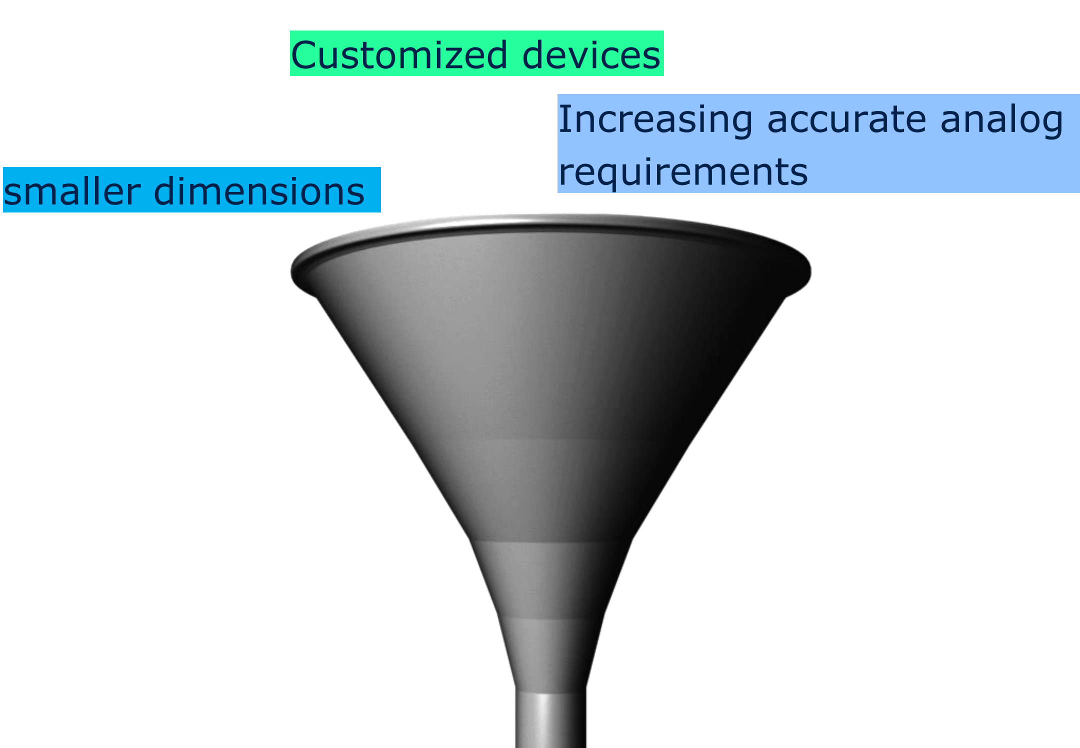
Summary



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