

# A Multi-Gate CMOS Compact Model – BSIMMG

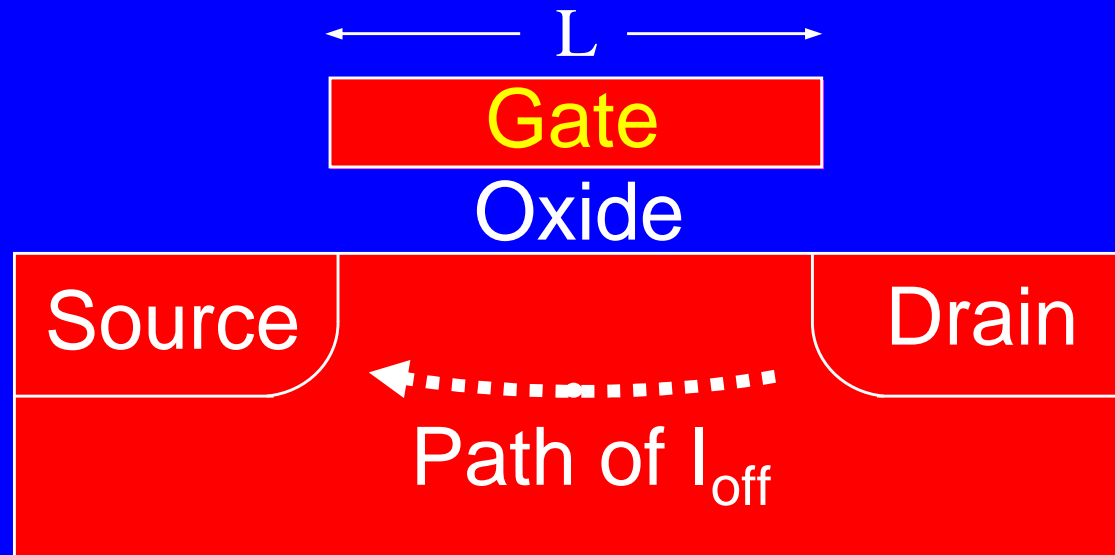
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University of California, Berkeley

# Acknowledgments

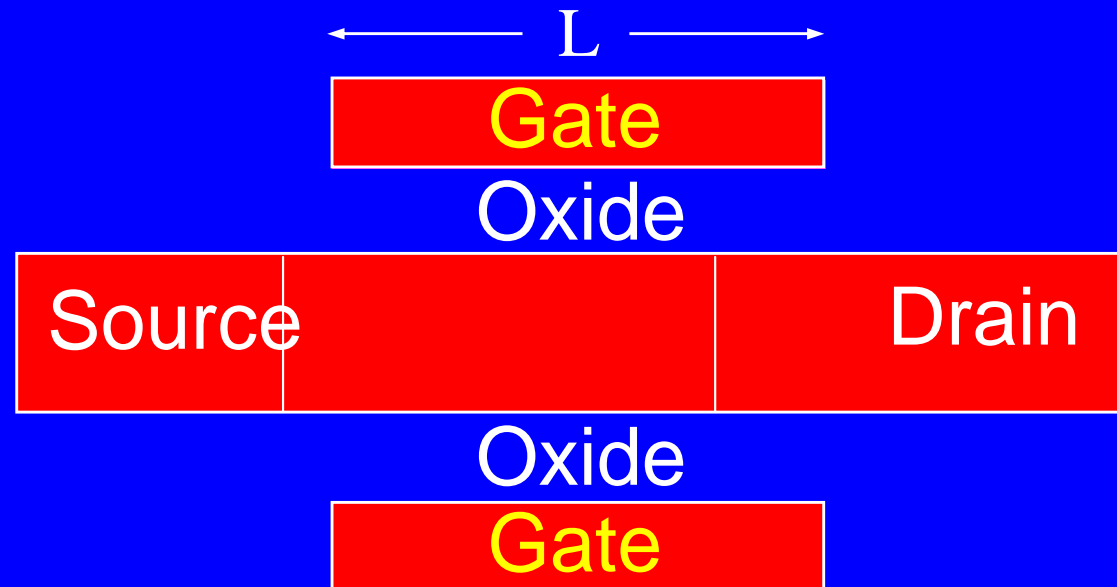
- **Support**
  - Semiconductor Research Corporation
  - IMPACT, UC Discovery and its industrial sponsors
  - SOITEC
- **Test Chip Fabrication**
  - Texas Instrument and ATDF
  - TSMC
- **Technical Discussions**
  - Wade Xiong (TI)

# Difficult to suppress leakage in scaled transistors



- Need thinner oxide to suppress leakage in scaled CMOS
- Gate leakage is an issue!

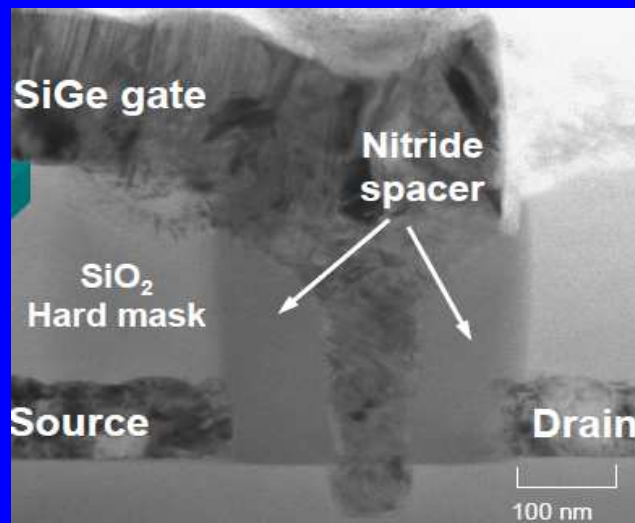
# Solution: Multi-gate MOSFETs



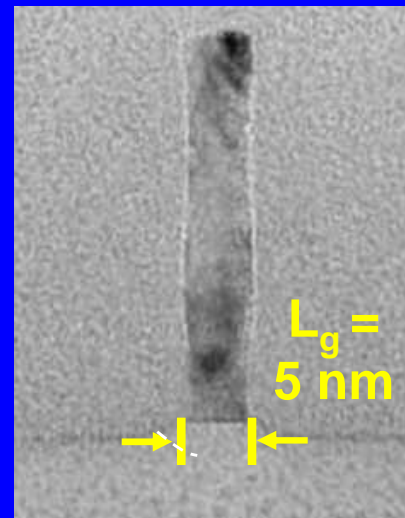
- Leakage is suppressed by multiple-gates
- Scale body thickness instead of oxide thickness

# Multi-gate Examples

## FinFET



X Huang et al., IEDM  
1999 (UC Berkeley)

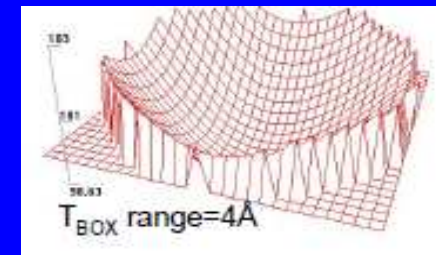


F.-L. Yang et al., VLSI  
2004 (TSMC)

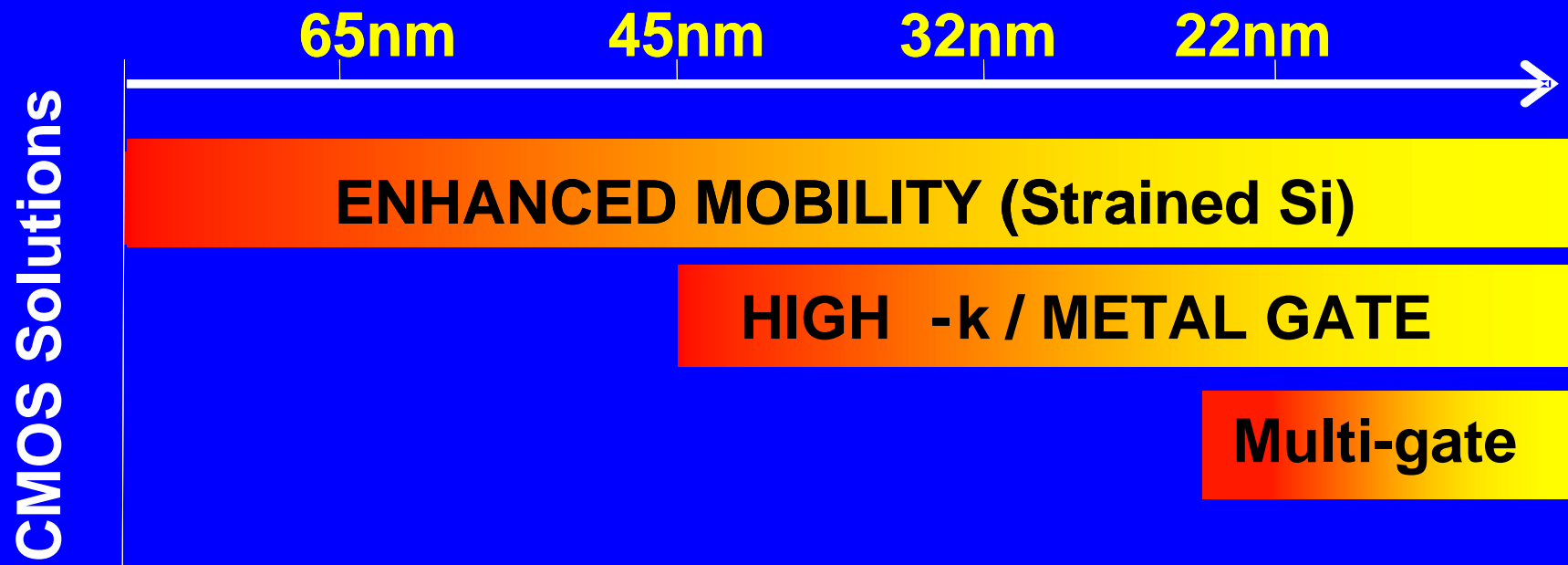
## UT2B



$T_{\text{Si}} = 7 \text{ nm}$   
 $T_{\text{box}} = 10 \text{ nm}$



F. Andrieu et al. VLSI 2010  
(LETI / ST / IBM / SOITEC)



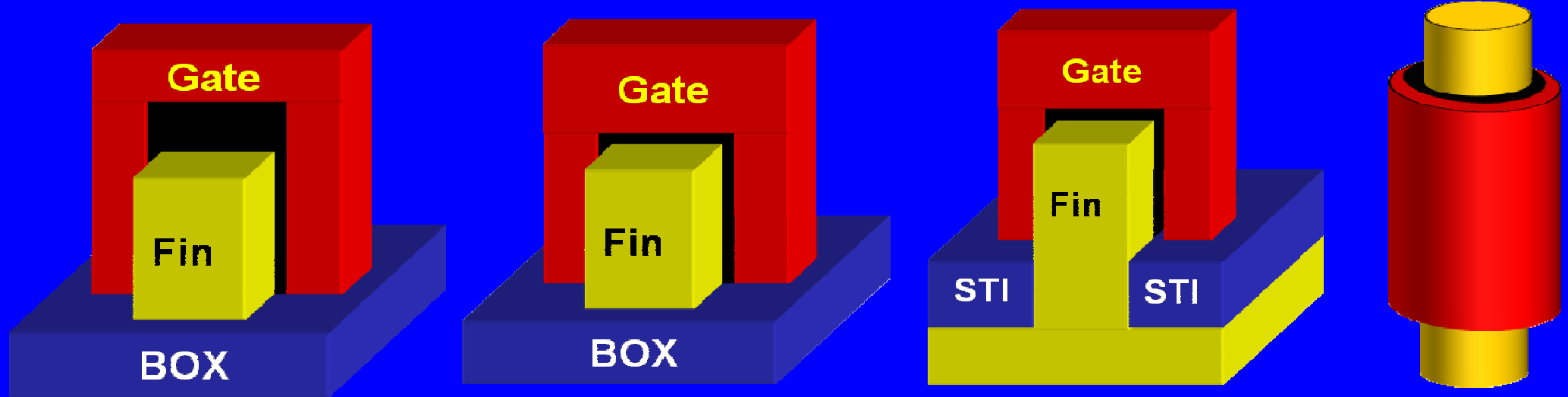
- Multi-gate FETs can extend CMOS scaling.
- **BSIM-MG compact model has been developed.**

# Outline

- **BSIM-CMG: Common Multi-gate MOSFET Model**
- **BSIM-IMG: Independent Multi-gate MOSFET Model**
- **Modeling of Real Device Effects**
- **Experimental Verification**
- **Summary**

# Common-Multi-Gate Modeling

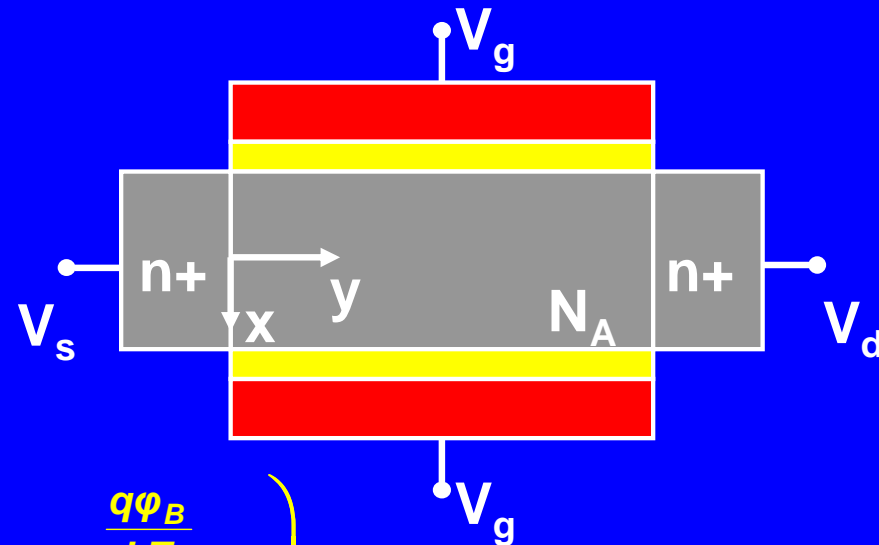
- **Common Multi-gate (BSIM-CMG):**
  - All gates tied together



- Surface-potential-based core I-V and C-V model
- Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates
- Physics-based model verified against TCAD and measurements

# Surface Potential Calculation (DG)

- Surface potential obtained by solving the 1D Poisson's equation



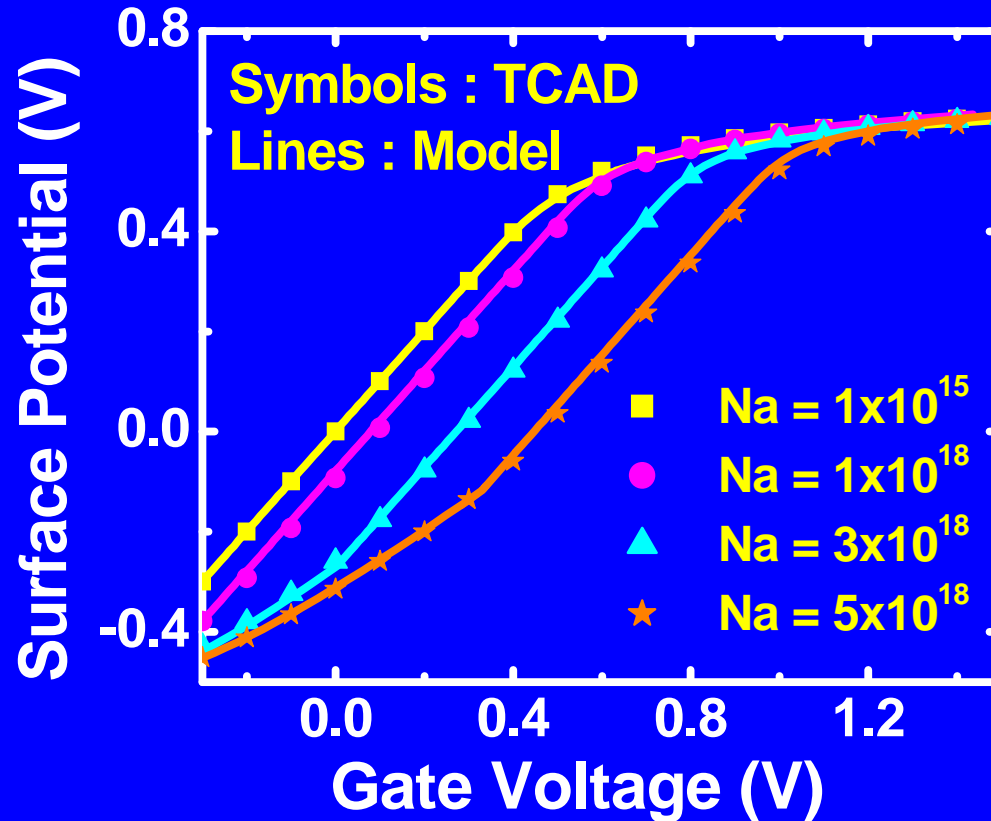
$$\frac{\partial^2 \psi}{\partial x^2} = \frac{qn_i}{\epsilon_{Si}} \cdot \left( \underbrace{e^{\frac{q\psi}{kT}} - e^{-\frac{q\phi_B}{kT}} - e^{-\frac{qV_{ch}}{kT}}}_{\text{Inversion Carriers}} + \underbrace{e^{\frac{q\phi_B}{kT}}}_{\text{Body Doping}} \right)$$

- A Perturbation approach is used to handle finite body doping

M. V. Dunga et al., TED 2006

$$\underbrace{\psi}_{\text{Net Surface Potential}} = \underbrace{\psi_{inv}}_{\text{Inversion Carriers only}} + \underbrace{\psi_{pert}}_{\text{Perturbation due to finite doping}}$$

# Surface Potential Calculation

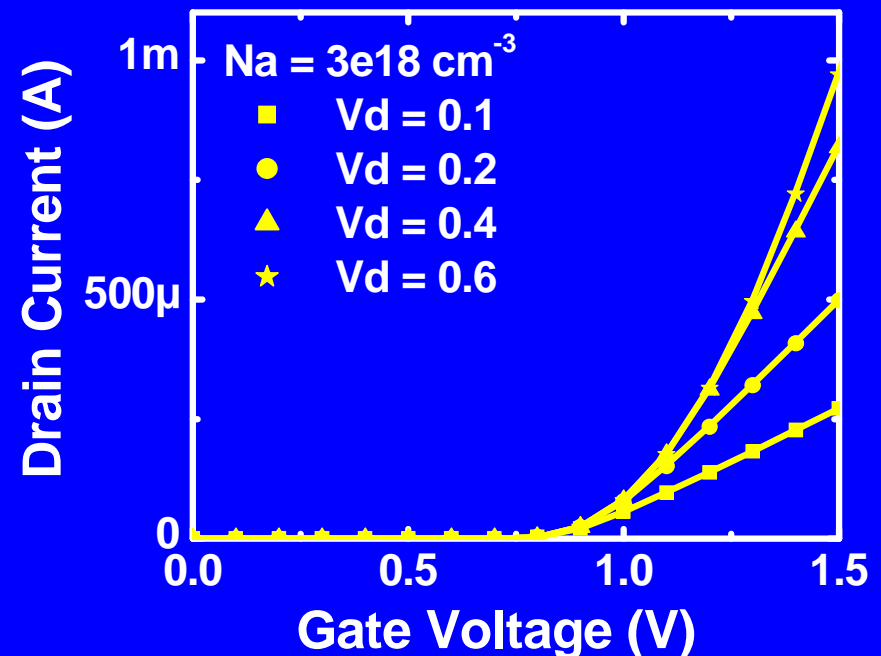
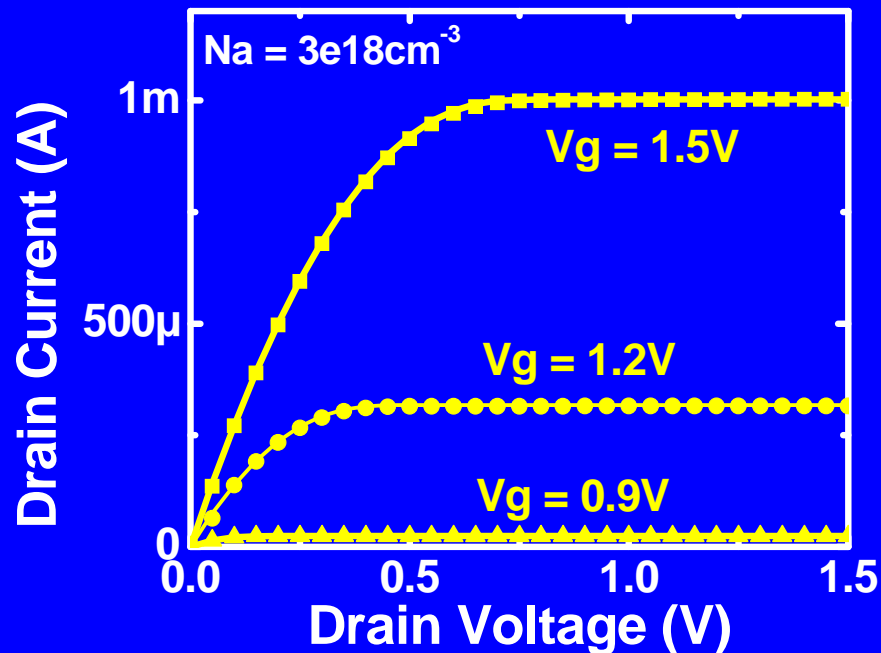


- Model matches 2D TCAD very well without fitting parameters in **both fully-depleted and partially-depleted regimes.**

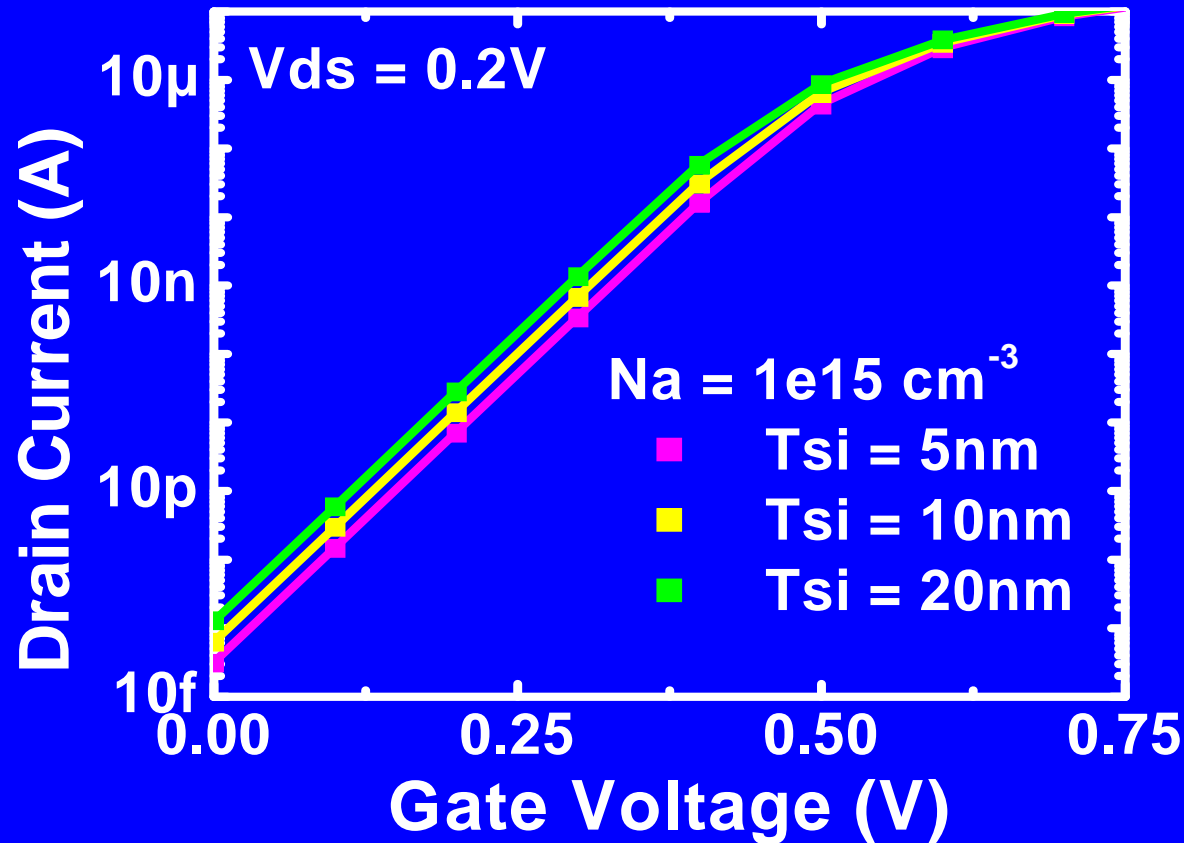
# I-V Model & Verification

- Drain current derived from drift diffusion

$$I_d = \mu \frac{W_{eff}}{L} \left[ \frac{Q_i^2}{2C_{ox}} + 2V_t Q_i - V_t \cdot (5C_{Si}V_t + Q_B) \ln(5V_t C_{Si} + Q_B + Q_i) \right]_d^s$$



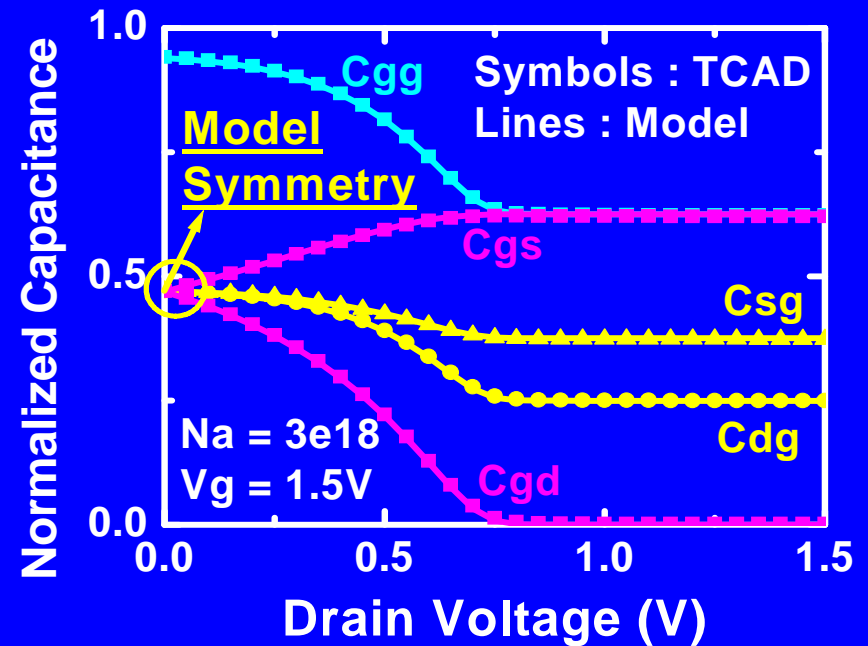
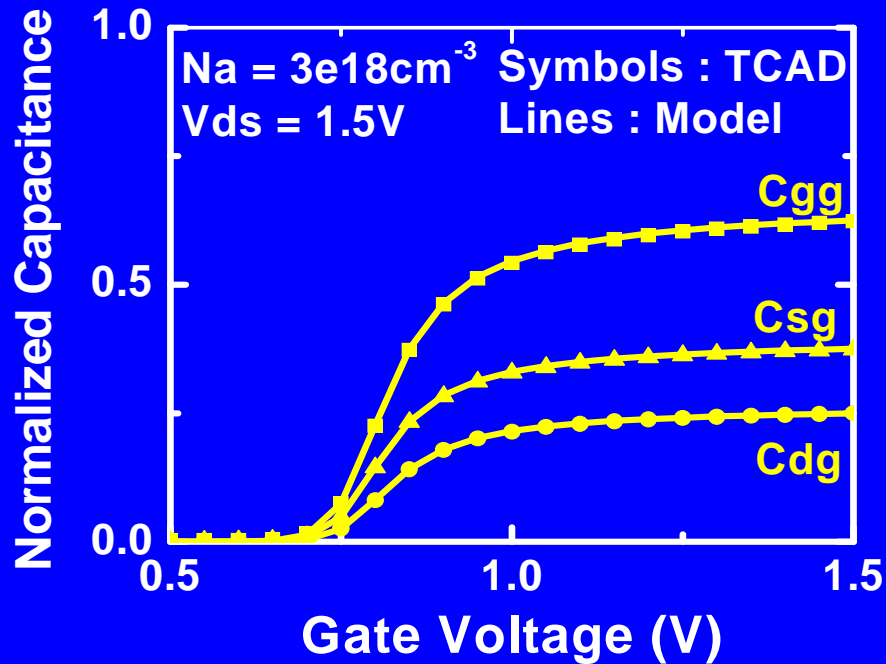
# Drain Current in Volume Inversion



Lines: Model  
Symbols: TCAD

In volume inversion  $I_d \propto T_{si}$  in sub-threshold.

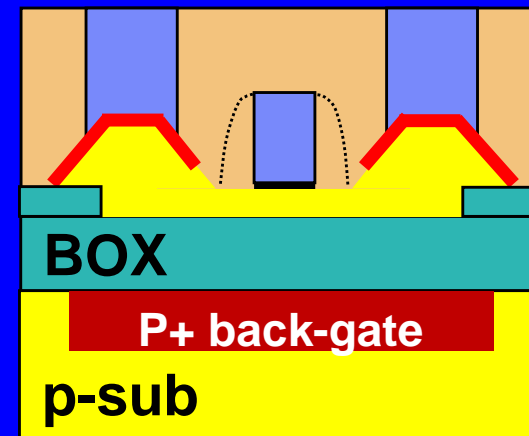
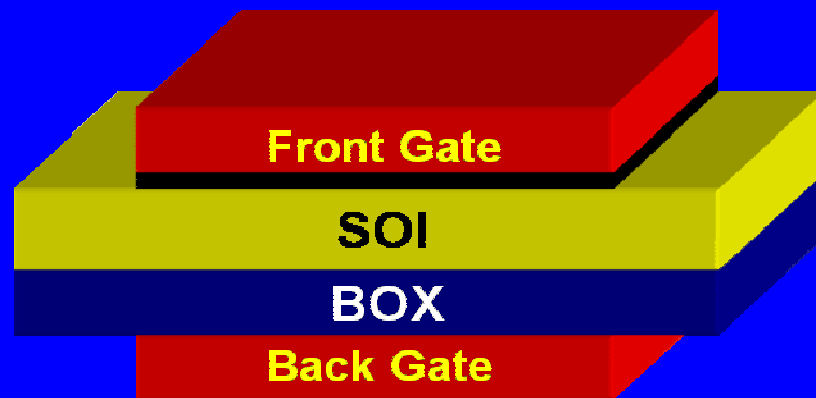
# C-V Model Verification



- C-V model agrees well with TCAD without any fitting parameters.
- The transcapacitances exhibit the correct symmetry behaviors.

# Independent Multi-Gate Modeling

- Independent Multi-gate (BSIM-IMG):
  - Separate Front- and Back-Gates
  - Asymmetric gate stacks: workfunction,  $T_{ox}$ , ...



Target device: BG-ETSOI or UTBB

- Physical surface-potential-based core I-V and C-V model agrees with TCAD without fitting parameters.

# Surface Potential

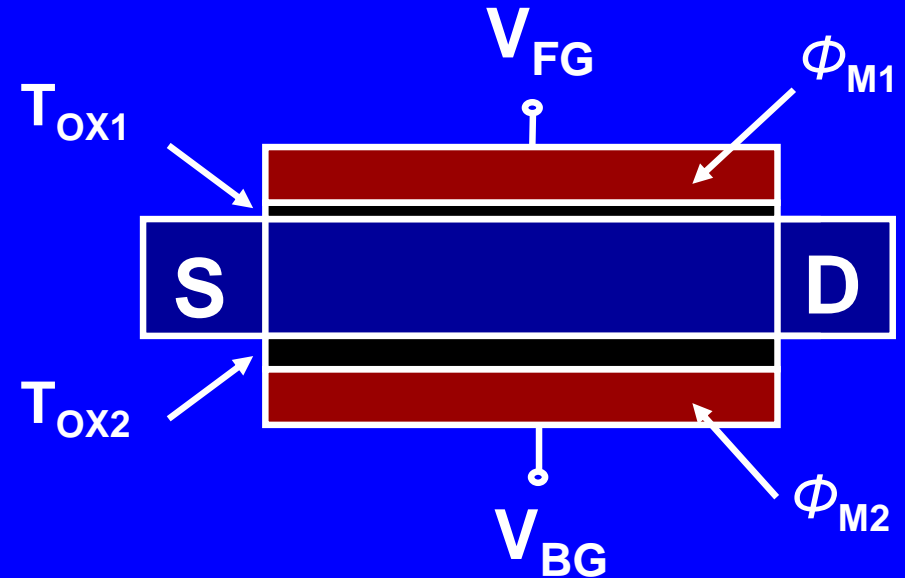
- Analytical Solution for  $\Psi_s$  is known

Y. Taur, TED 2001

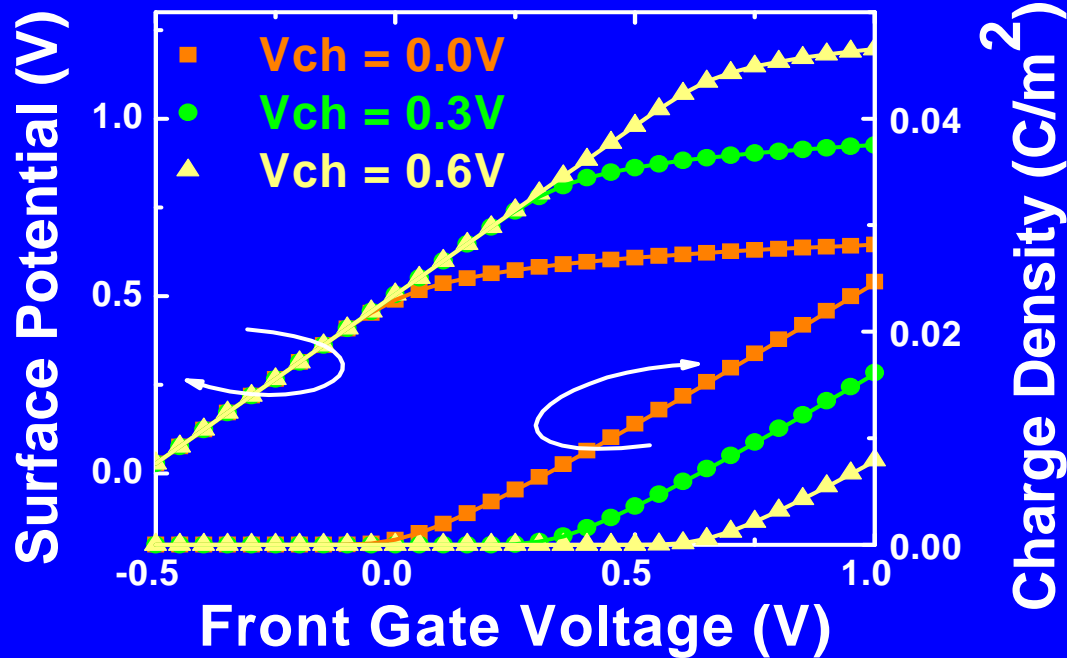
H. Lu et al., TED 2006

- Newton iteration needed for  $\Psi_s$  calculation
- Approximation for front-, back-surface potential and charge developed
  - Better computational efficiency

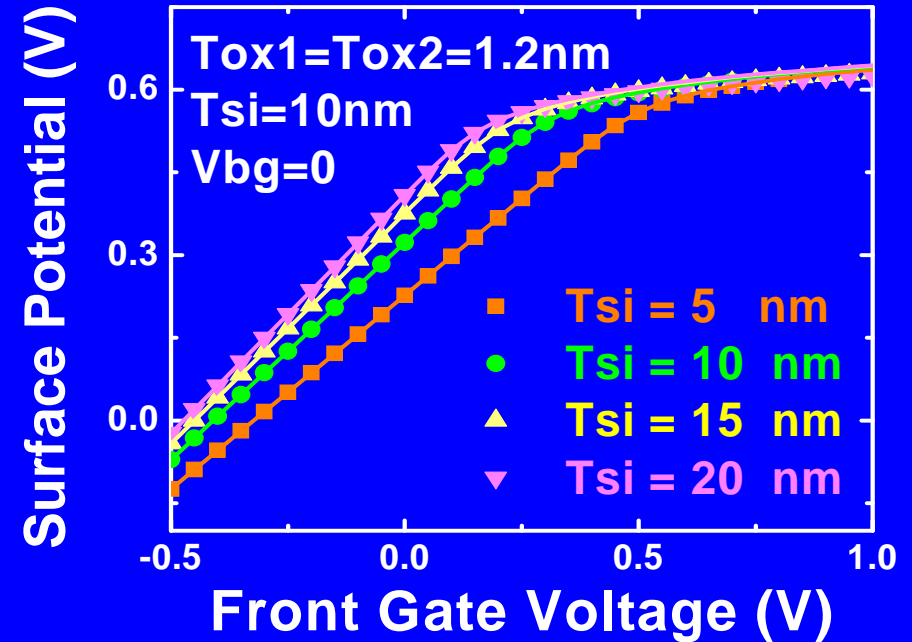
D. Lu, UCB Master's Report



# Surface Potential Verification



Symbols: Exact Poisson Lines: Model



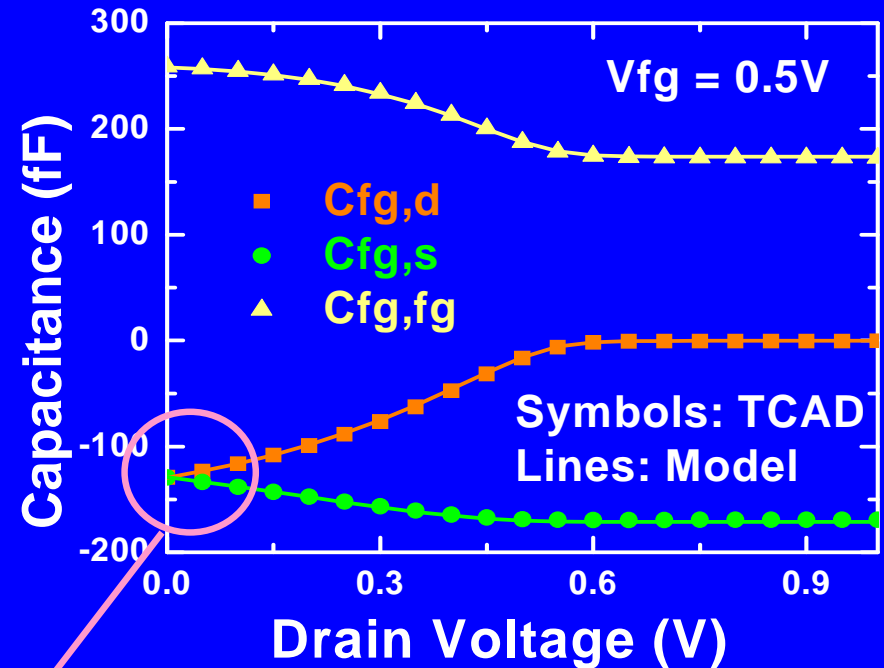
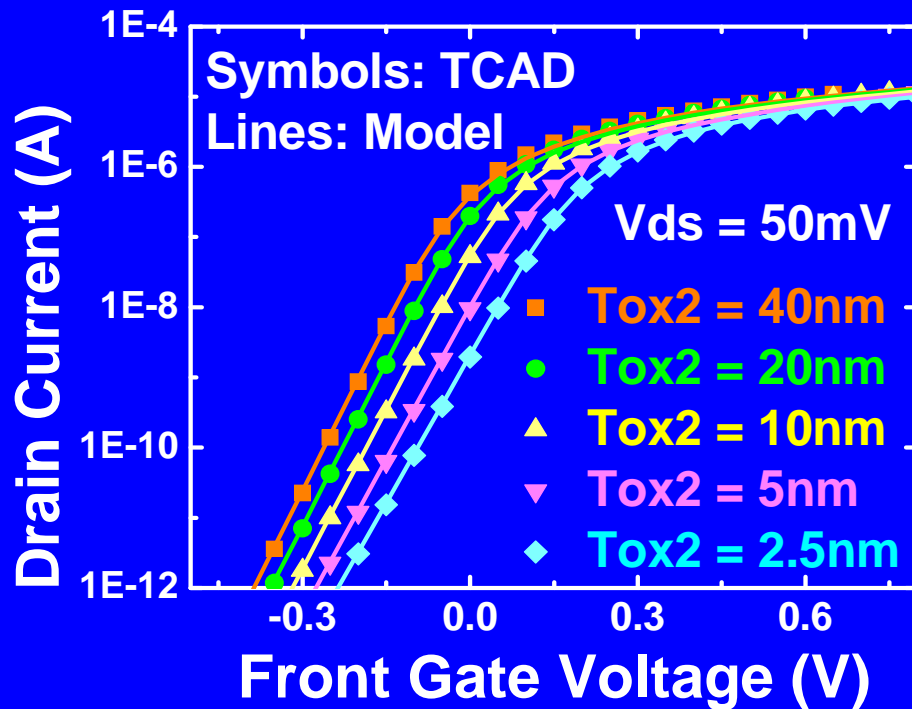
Symbols: TCAD Lines: Model

- Analytical  $Q_s$ ,  $\Psi_{SF}$  agrees with Exact Poisson Solution & TCAD without fitting parameters.
- Scalability of the model is demonstrated.

# Core I-V and C-V Model

- Physical I-V and C-V model agrees well with TCAD
- Transcapacitances exhibit correct symmetry

D. Lu et al., IEDM 2007



$Tox1 = 1.2\text{nm}$      $Tox2 = 40\text{nm}$   
 $Tsi = 15\text{nm}$      $V_{bg} = 0$

Model Symmetry

# Real-Device Effects Modeled

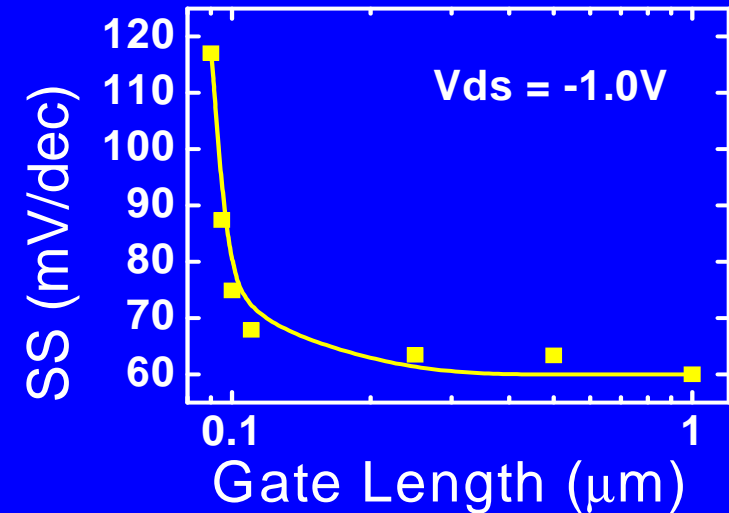
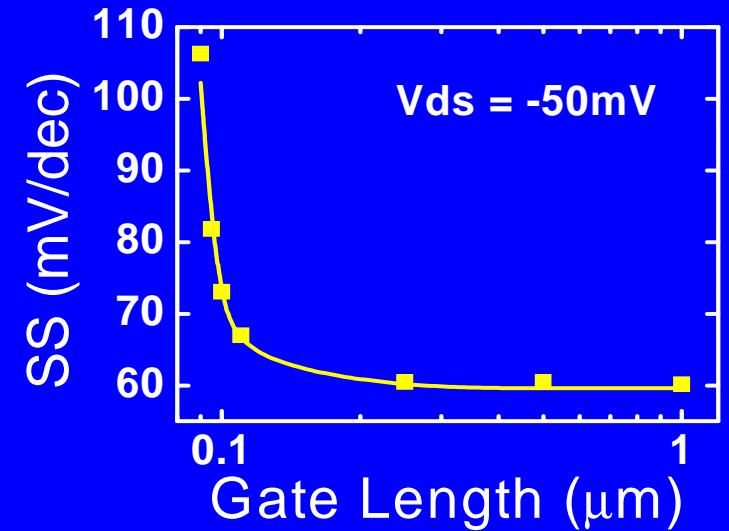
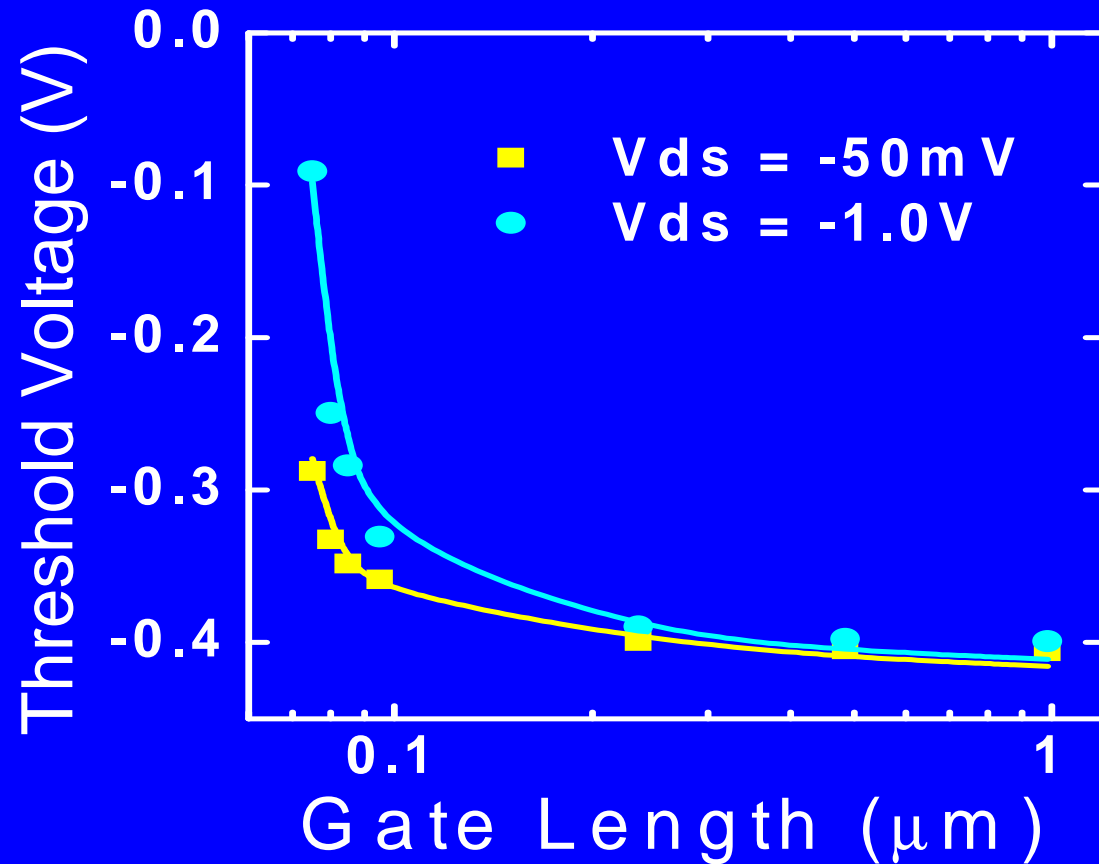
- Quantum effects (charge centroid model)
- Short Channel Effects --  $V_{th}$  roll-off, Sub-threshold swing degradation, DIBL, CLM
- Mobility Degradation
- Velocity Saturation
- GIDL, GISL and Junction Leakage
- Gate Tunneling Current
- Temperature effects
- Parasitic Capacitance
- Series Resistance
- Etc.

# Short Channel Effects

$$\Delta V_{th}, \text{DIBL}, \text{SS} \sim \frac{1}{\cosh\left(\text{CONST} \cdot \frac{L_G}{\lambda}\right) - 1}$$

- Z. Liu et al., TED 1993

Symbols: Measurements  
Lines: Model



SS: Subthreshold Swing

$V_{th}$  Definition:  $I_{th} = 300\text{nA} * W / L$

# Scale Length for Various Modes

- Double-gate

$$\lambda_{\text{DG}} = \sqrt{\frac{\epsilon_{\text{si}}}{2\epsilon_{\text{ox}}} \left( 1 + \frac{\epsilon_{\text{ox}} T_{\text{FIN}}}{4\epsilon_{\text{si}} T_{\text{ox}}} \right) T_{\text{FIN}} T_{\text{ox}}}$$

- K. Suzuki et al., TED 1993

- Triple-gate

$$\lambda_{\text{TG}} = \frac{1}{\sqrt{\frac{1}{\lambda_{\text{DG}}} + \frac{1}{4H_{\text{eff}}^2}}}$$

$$H_{\text{eff}} = \sqrt{\frac{H_{\text{fin}}}{8} \cdot \left( H_{\text{fin}} + 2 \frac{\epsilon_{\text{si}}}{\epsilon_{\text{ox}}} T_{\text{ox}} \right)}$$

- Cylindrical-gate

$$\lambda_{\text{CG}} = \sqrt{\frac{\epsilon_{\text{si}}}{2\epsilon_{\text{ox}}} \left( 1 + \frac{\epsilon_{\text{ox}} R}{2\epsilon_{\text{si}} T_{\text{ox}}} \right) R \cdot T_{\text{ox}}}$$

- Independent-gate

$$\lambda_{\text{F}} = \sqrt{\frac{\epsilon_{\text{si}}}{\epsilon_{\text{ox}}} T_{\text{si}} T_{\text{ox}1}}$$

Leakage path at front surface

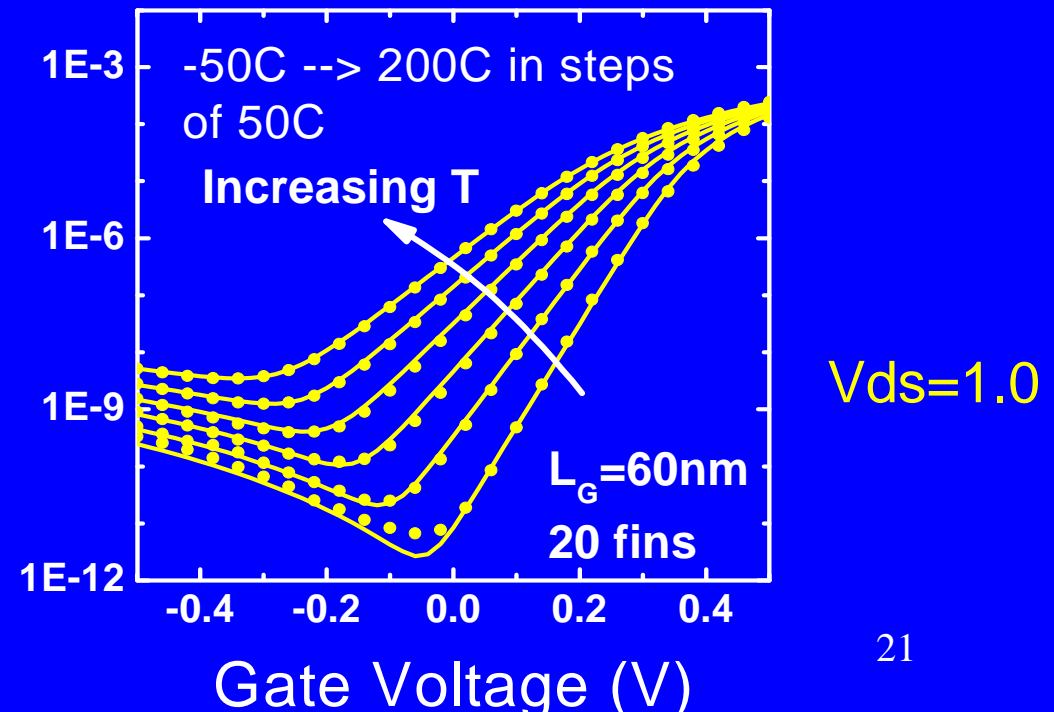
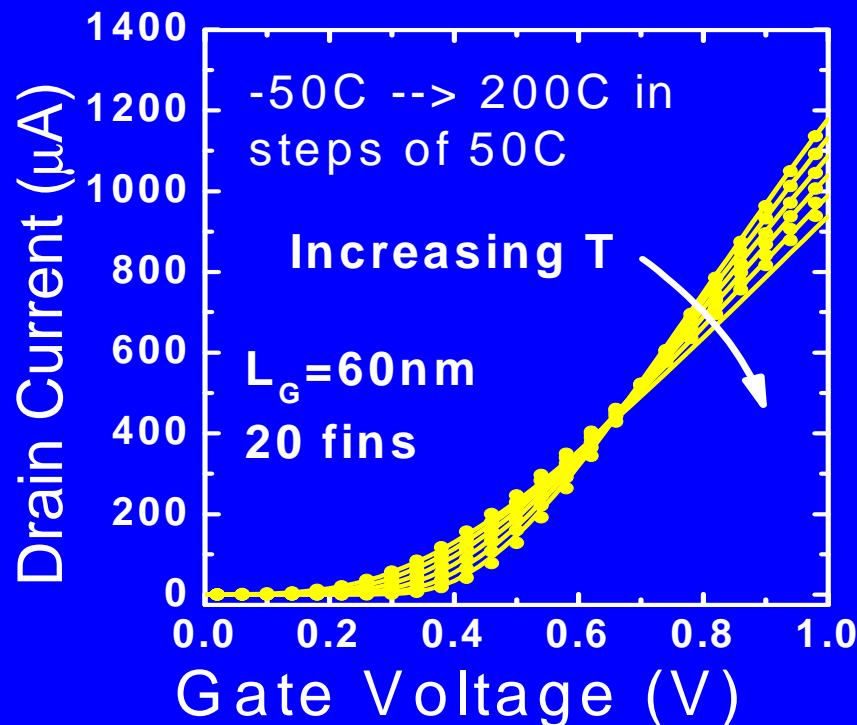
$$\lambda_{\text{M}} = \sqrt{\frac{\epsilon_{\text{si}}}{\epsilon_{\text{ox}}} T_{\text{si}} T_{\text{ox}1} + \frac{3}{8} T_{\text{si}}^2}$$

Leakage path in the center

# Temperature Effects

- Temperature dependence are well-modeled
  - Mobility temperature dependence:  $\mu_0(T)$ ,  $\mu_A(T)$
  - Saturation Velocity temperature dependence:  $V_{SAT}(T)$
  - Subthreshold Swing =  $nkT/q$
  - GIDL Leakage:  $BGIDL(T)$
  - A few others

**Symbols: SOI FinFET data**  
**Lines: Model**

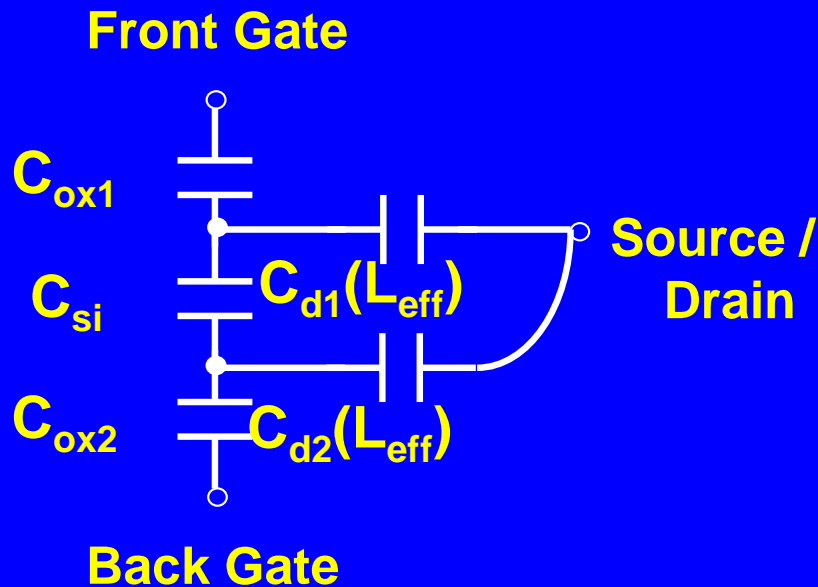


# Length Dependent $\gamma$ Model for Independent-gate

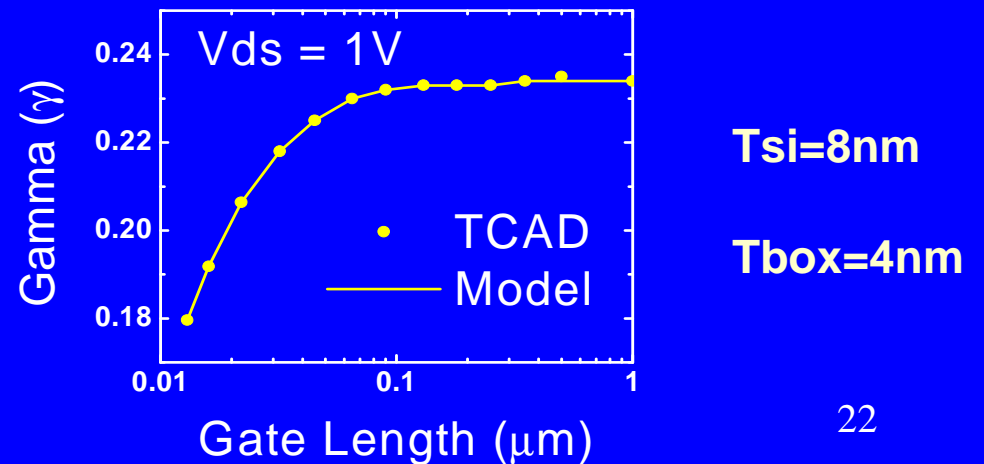
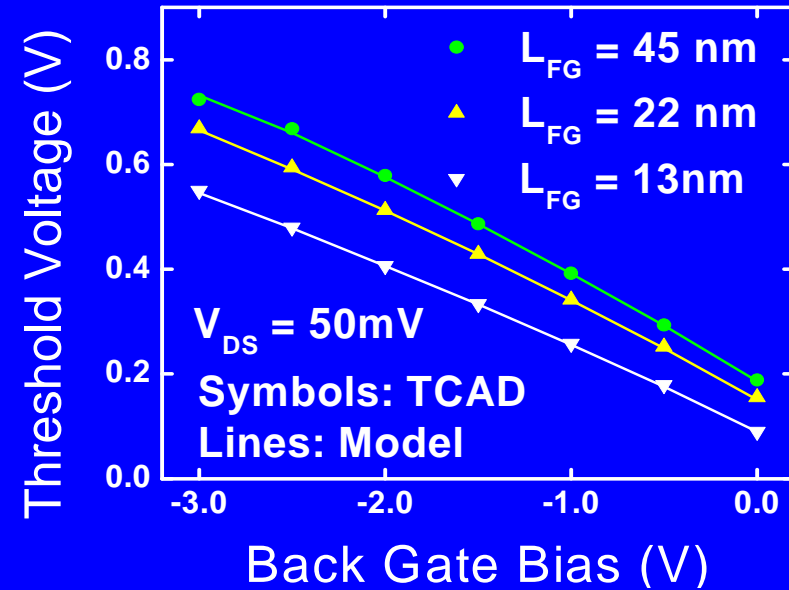
Gamma definition:

$$\gamma = -\frac{dV_{TH}}{dV_{bg}}$$

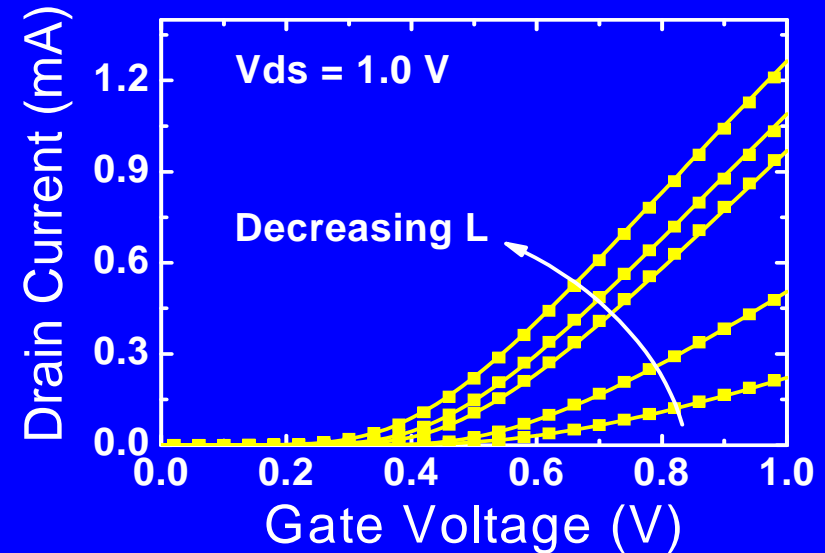
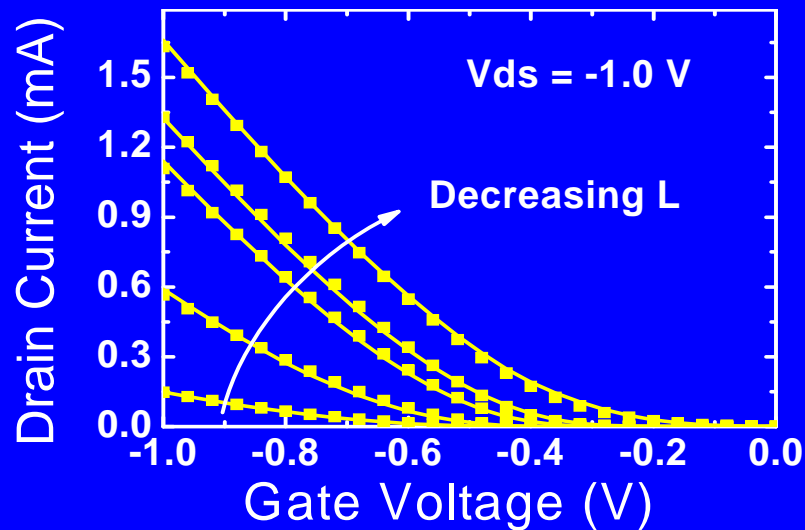
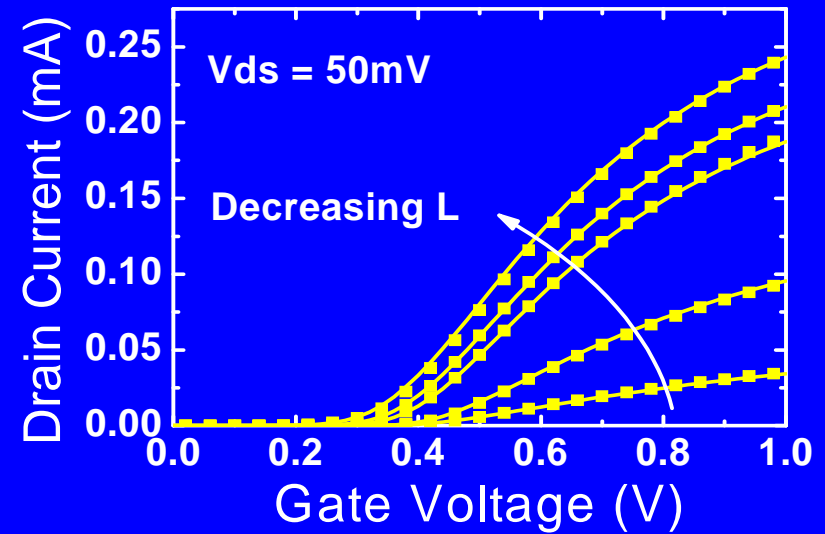
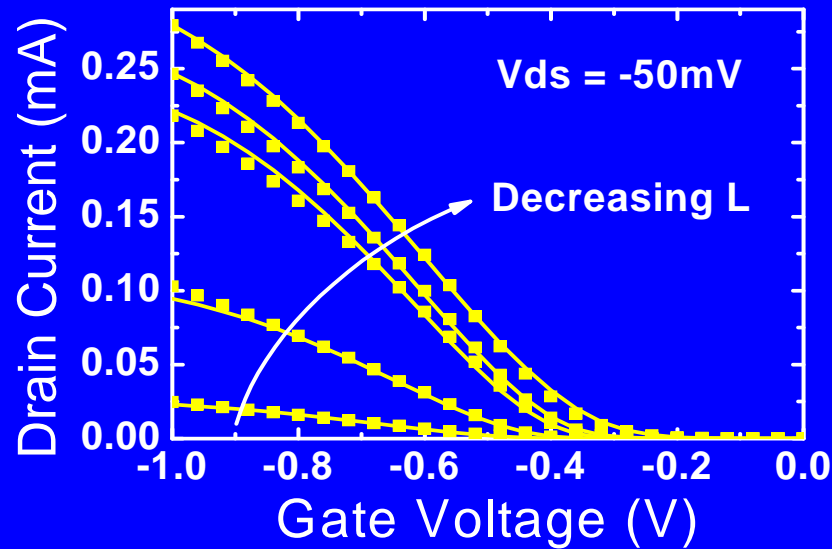
Capacitance network analysis:



$\gamma$  degradation for short channel:



# SOI FinFET Global Parameter Extraction

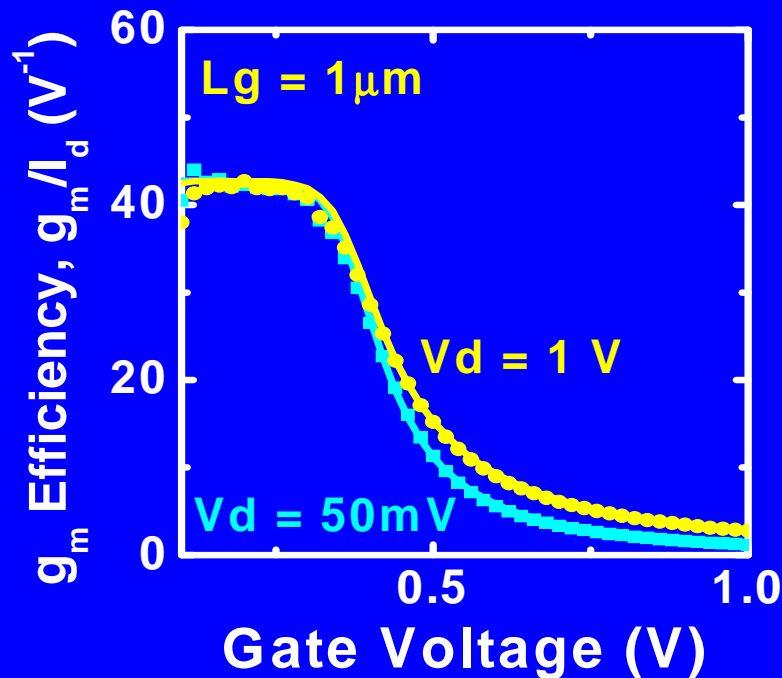


- **FinFET with  $L_G = 1\mu\text{m}, 235\text{nm}, 95\text{nm}, 85\text{nm}, 75\text{nm}$   $H_{\text{fin}}=60, T_{\text{fin}}=22,$   
20 lightly-doped fins**

# Analog metrics (SOI FinFETs)

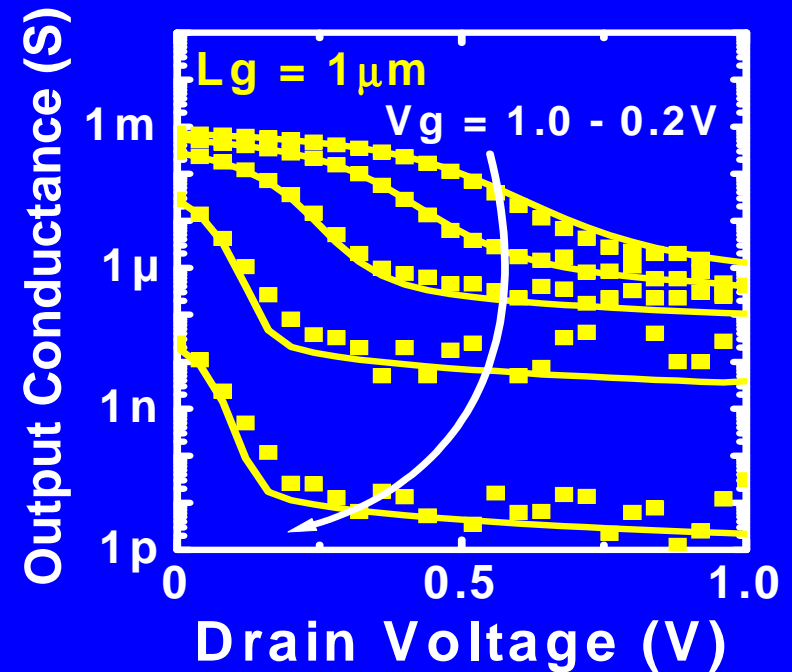
- Analog metrics ( $g_m/I_d$  and  $g_{ds}$ ) for the long channel are also captured well.

$g_m$  Efficiency ( $g_m/I_d$ )



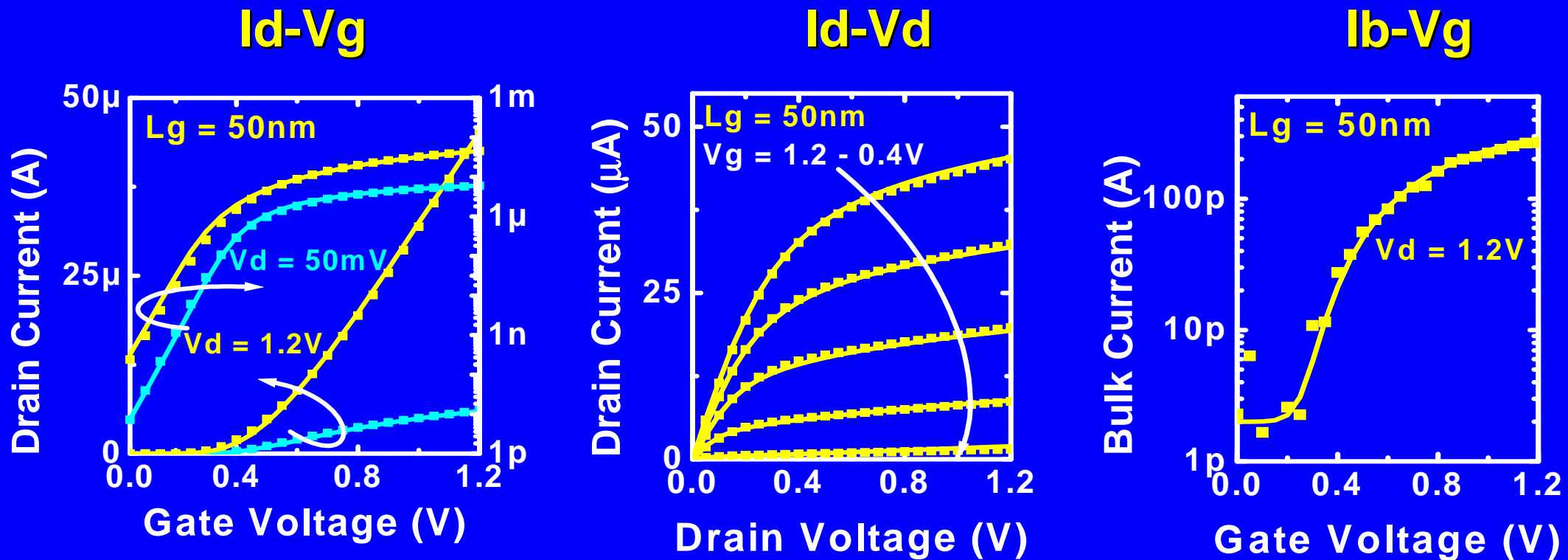
Dunga et al., VLSI 2007

Output Conductance



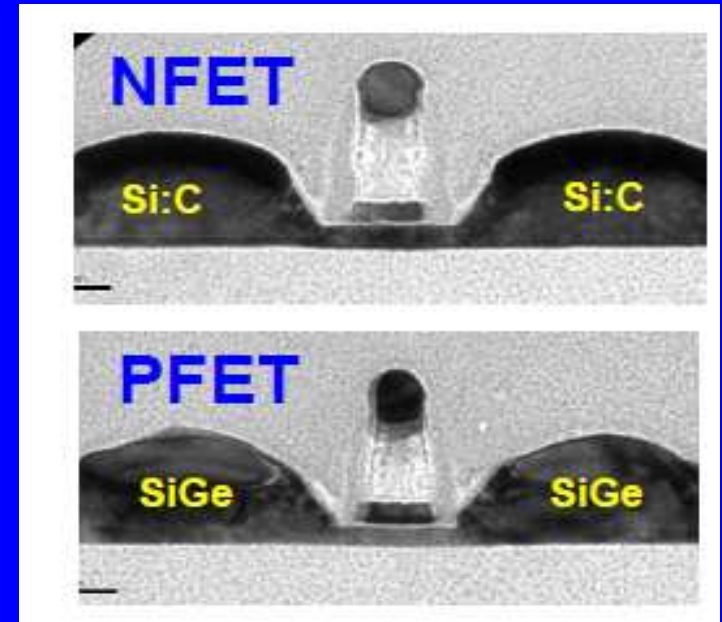
# Short Channel Bulk FinFETs

- Model is used to describe bulk FinFET technology also.
- Substrate Current: Impact Ionization



# Validation of BSIM-IMG Model

- ❑ Global parameter extraction
  - ❑ 22nm ETSOI technology (IBM)
  - ❑  $I_{ds}$  for NMOS and PMOS
  - ❑  $L_g = 24.5\text{nm} \dots 66\text{nm}$
  - ❑ Model extracted using ICCAP
  - ❑ Parasitic capacitances calibrated to mixed-mode TCAD

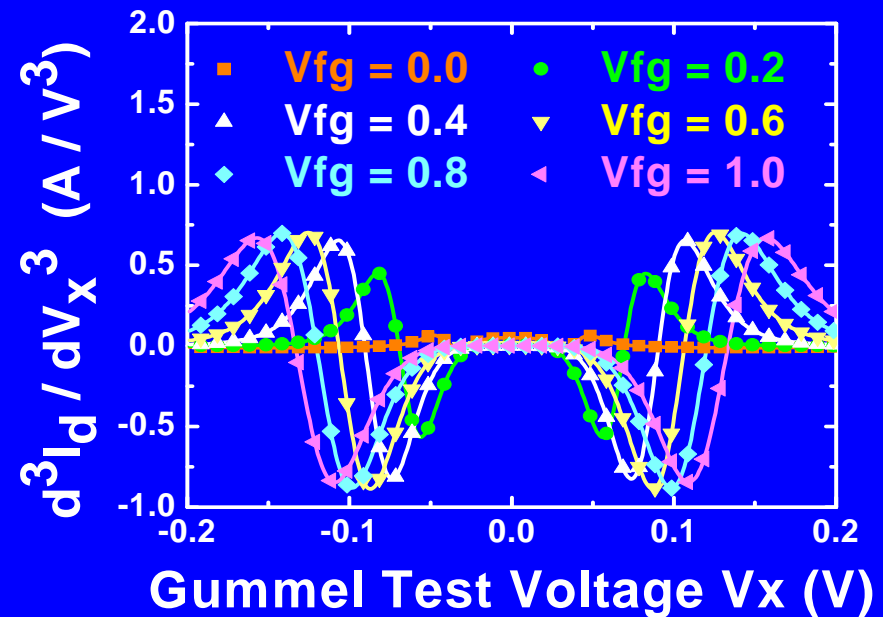
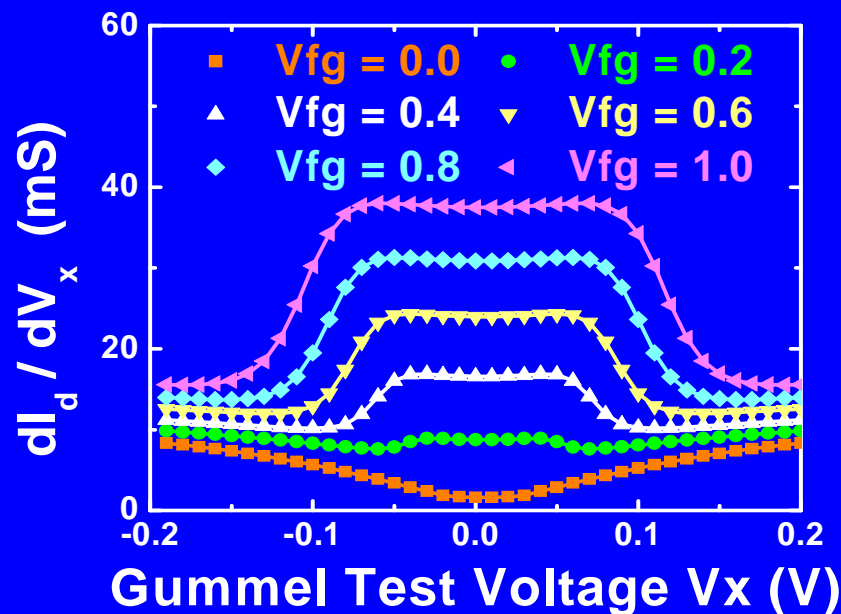


## ETSOI

K. Cheng et al. IEDM 2009  
(IBM / ST)

# Gummel Symmetry Test

- $I_{ds}$  continuity at  $V_{ds}=0$  is verified through the Gummel symmetry test.
- Both BSIM-CMG and BSIM-IMG passes this test



Results shown here are 1<sup>st</sup> & 3<sup>rd</sup> order derivatives of  $I_{ds}$  for BSIM-IMG

# Summary

- **Core I-V and C-V models for common and independent multi-gate FETs are developed and verified with TCAD without using fitting parameters**
- **Volume inversion and the effect of finite body doping are captured.**
- **BSIM-like real device effects are implemented.**
- **BSIM-CMG is calibrated to an SOI FinFET technology and a bulk FinFET technology. Short channel effects, temperature dependence, GIDL leakage, substrate current and analog metrics agree well with data.**
- **BSIM-IMG is also calibrated to an ETSOI technology with good agreements.**