The direct determination of MOSFET parameters from the $I_D$ versus $V_S$ curve at low $V_{DS}$

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Contents

1 - Threshold Voltage definitions

2 - Determination of MOSFET parameters from $I_D \times V_S$ curve, (channel_conductance)/$I_d$ method

3 - Comparison with $g_m/I_d$ method

4 - Applications of the threshold voltage determinations

5 - Conclusions
Near the threshold condition (moderate inversion), both the drift and diffusion transport mechanisms are important.

No critical point can be directly identified

*I from Yannis Tsividis, Operation and Modeling of The MOS transistor, McGraw-Hill*
Classical threshold voltage (VT) definition

Classical (surface potential based) definition of threshold:

\[ \phi_S = 2\phi_F + V_C \]

Where:
- \( \phi_S \) - surface potential for \( V_G = V_T \)
- \( \phi_F \) - Fermi potential in the substrate
- \( V_C \) - channel potential

In principle the direct determination of the threshold voltage is possible

1) calculate the saturation drain current \( I_{DTh} \) for \( \phi_S = 2\phi_F + V_C \)
2) inject \( I_{DTh} \) in the transistor and measure \( V_G = V_T \)

Drawbacks

- geometrical (W, L) and technological parameters (mobility, oxide thickness,..) are needed to calculate \( I_{DTh} \)
- the transistor operates in the saturation region where several secondary effects are relevant
Current based threshold definition

\[ V_T = V_G, \text{ when } I_{\text{drift}} = I_{\text{diff}} \]

For a MOSFET the current defined threshold corresponds to an inversion charge density equal to the thermal charge density (the effective channel capacitance per unit area times the thermal voltage).

For a bulk MOSFET

\[ Q'_I = -nC'_OX \phi_t \]

where \( n \) is the slope factor
## Relationship between threshold voltages

<table>
<thead>
<tr>
<th>Threshold Definition</th>
<th>Physical Meaning</th>
<th>Value of $\phi_S$ at threshold</th>
<th>Value of $Q'_i$ at threshold</th>
<th>Difference in $V_{T0}$ relative to classical definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\phi_S = 2\phi_F + V_C$</td>
<td>Surface concentration of electrons= bulk concentration of holes</td>
<td>$2\phi_F + V_C$</td>
<td>$-(n-1)C'_ox\phi_i$</td>
<td>0</td>
</tr>
<tr>
<td>$Q'_i = -nC'_ox\phi_i$</td>
<td>$50%$ drop (relative to the peak) in the $g_m/I_D$ curve</td>
<td>$2\phi_F + V_C + \phi_i \ln\left(\frac{n}{n-1}\right)$</td>
<td>$-nC'_ox\phi_i$</td>
<td>$\phi_i \left[1 + n \ln\left(\frac{n}{n-1}\right)\right]$</td>
</tr>
</tbody>
</table>
‘Ideal’ threshold voltage extraction procedure

• No parameters are needed to calculate the threshold current
• The transistor operates at low current levels and in the linear region to minimize series resistances and short channel effects

\[ \text{gm/Id curve in the linear region} \]
VT determination from $gm/Id$ curve in the linear region

- Transconductance-to-current ratio for $V_{DS} \equiv \phi_t/2$ and $V_S=0$.

\[ \text{Threshold } g_{m}/I_{D} \equiv 0.5\ (g_{m}/I_{D})_{\max} \]

Drawback $(g_{m}/I_{D})_{\max}$ has some dependence on $V_G$
The new (channel conductance $G_{no}/I_d$) methodology

Direct determination of MOSFET parameters from the ID versus VS curve at low VDS

$$\Delta V_S = \Delta V_D = \Delta V_X$$

$$\frac{\partial I_D}{\partial V_X} = -g_{ms} + g_{md} = G_{no}$$
The Gn0/Id methodology

Transistor operation:
- low $V_{DS}$
- weak and moderate inversion
- fixed $V_G$

Negligible effects of:
- series resistances
- field dependent mobility
- slope factor variation
- channel length modulation
The Gn0/Id methodology – extract $V_T$ and $I_S$

From transistor model

$$g_{ms(d)} = \frac{2I_s}{\phi_i} \left(\sqrt{1+i_{f(d)}} - 1\right)$$

$$I_D = I_s(i_f - i_r) \quad I_s = \mu C_{ox} n \frac{\phi_i^2}{2} \frac{W}{L}$$

$$G_{n0} = \frac{-2}{\phi_i \left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)} = \left(\frac{G_{n0}}{I_D}\right)_{\text{min}} \frac{2}{\sqrt{1+i_f} + \sqrt{1+i_r}}$$

From UICM

$$\frac{V_P - V_{S(D)}}{\phi_i} = \sqrt{1+i_f(r)} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)$$

When $i_f=3 \Rightarrow V_P=V_S=V_X$

When

for $i_f = 3$ and $V_{DS} = \phi_i / 2$

we have $i_r = 2.12$

$$\frac{G_{n0}}{I_D} = 0.53 \times \left(\frac{G_{n0}}{I_D}\right)_{\text{min}}$$

and

$V_P = V_X$

$V_{DS} = \phi_v / 2$

$V_X$

$V_G$
The Gn0/Id methodology – extract $V_T$ and $I_S$

When

$$\frac{G_{n0}}{I_D} = 0.53 \left( \frac{G_{n0}}{I_D} \right)_{\text{min}}$$

$$V_P = V_X$$

$$V_{T0} = -nV_P + V_G$$

and

$$I_S = I_D$$
The Gn0/Id methodology – extract pinch-off voltage $V_p$ and slope factor $n$

- **BSIM simulation**

$V_p$ vs $V_G$

$n = \frac{1}{dV_p/dV_G}$

- Measuring $I_D \times V_S$ for different $V_G$ values
Gn0/Id x gm/Id methods

\[ \frac{g_{mI}}{I_D} = \frac{2}{n\sigma_t \left( \sqrt{1 + i_f} + \sqrt{1 + i_r} \right)} \]

\[ \frac{|G_{n0}/I_D|}{I_D} = \frac{-2}{\phi_t \left( \sqrt{1 + i_f} + \sqrt{1 + i_r} \right)} \]
Gn0/Id x gm/Id methods

0.18 µm technology

$V_{T0}$

<table>
<thead>
<tr>
<th>$L_{mask}$ (W/L=100)</th>
<th>0.2 µm</th>
<th>0.3 µm</th>
<th>0.4 µm</th>
<th>0.5 µm</th>
<th>0.6 µm</th>
<th>0.8 µm</th>
<th>2.0 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_T$ (mV) gm/Id</td>
<td>514</td>
<td>499</td>
<td>494</td>
<td>488</td>
<td>484</td>
<td>478</td>
<td>456</td>
</tr>
<tr>
<td>$V_T$ (mV) Gn0/Id</td>
<td>515</td>
<td>495</td>
<td>490</td>
<td>486</td>
<td>481</td>
<td>475</td>
<td>455</td>
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$I_s$ when $V_{GS}=V_{T0}$

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<th>2.0 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_s$ (µA) gm/Id</td>
<td>23.82</td>
<td>18.21</td>
<td>16.19</td>
<td>15.67</td>
<td>15.54</td>
<td>15.94</td>
<td>16.62</td>
</tr>
<tr>
<td>$I_s$ (µA) Gn0/Id</td>
<td>21.47</td>
<td>15.21</td>
<td>13.27</td>
<td>13.53</td>
<td>13.41</td>
<td>13.72</td>
<td>14.65</td>
</tr>
</tbody>
</table>

$0.18 \mu m$ technology

V_T when $V_{GS}=V_{T0}$

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Applications

Applications using VT extraction

- Transistor aging (or electrical stress)
- Matching assessment
- Temperature drift characterization
- Radiations effects on MOS transistor
Applications

1- Extract IS and VT in a non-noisy environment using an accurate method (gm/Id or Gn0/Id)

2- Extract VT in a real environment considering Id=3*Is \( (i_f=3) \) in a saturated transistor

\[
VP = \frac{V_G - V_{T0}}{n}
\]

From UICM when \( i_f = 3 \), \( V_P = V_S \)
Example of HCI stress measurement using VT variation

\[ \Delta V_T \text{ [mV]} \]

\[ \text{Time [Seconds]} \]

- 55C
- 25C
- 125C
Conclusions

• New procedure for direct determination of the threshold voltage and some other important electrical parameters with minimum influence of second order effects.

• The threshold voltage is determined at a constant gate-to-substrate voltage, at a low drain-to-source voltage and with transistor operation in the weak and moderate inversion regions.

• Under these operating conditions the effects of series resistances, mobility and slope factor variations, and channel length modulation are practically negligible, allowing a direct determination of the threshold voltage and of the DIBL effect.