Compact Modeling Activities in the Cfaed

Dr.-Ing. Martin Claus

Leader of Device Modeling Group for Emerging Electronics
Center for advancing electronics Dresden (cfaed)
Technische Universität Dresden, Germany,
martin.claus@tu-dresden.de

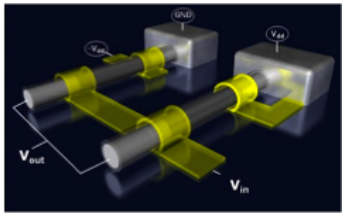
MOS-AK Workshop – 18.03.2016

German Cluster of Excellence
Center for Advancing Electronics Dresden

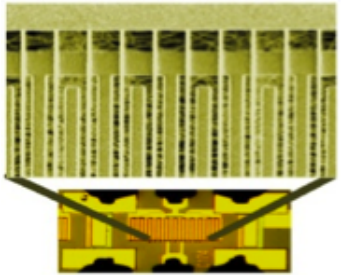
Center for Advancing Electronics Dresden

- 9 emergent technologies (Carbon, Nanowires, Organic, . . .)
- 60 principle investigators from EE, Computer Science, Chemistry, Physics, Biology, Mathematics
- Centered at Dresden, close connection to semicond. industry (Infineon, Global Foundries, Intel, . . .)
- Funding volume: 34 Mio. EUR
- First funding period: 01.11.2012 - 31.10.2017

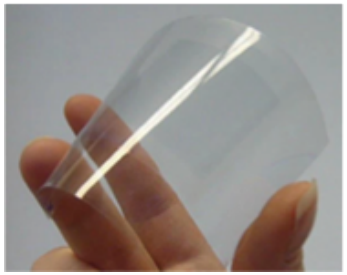
Selected Cfaed technologies



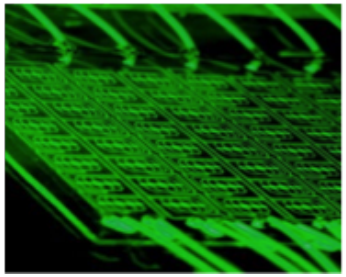
Nanowire Path
NW-based reconfigurable circuits and nanosensing



Carbon Path
CNT-based circuits for high-frequency applications

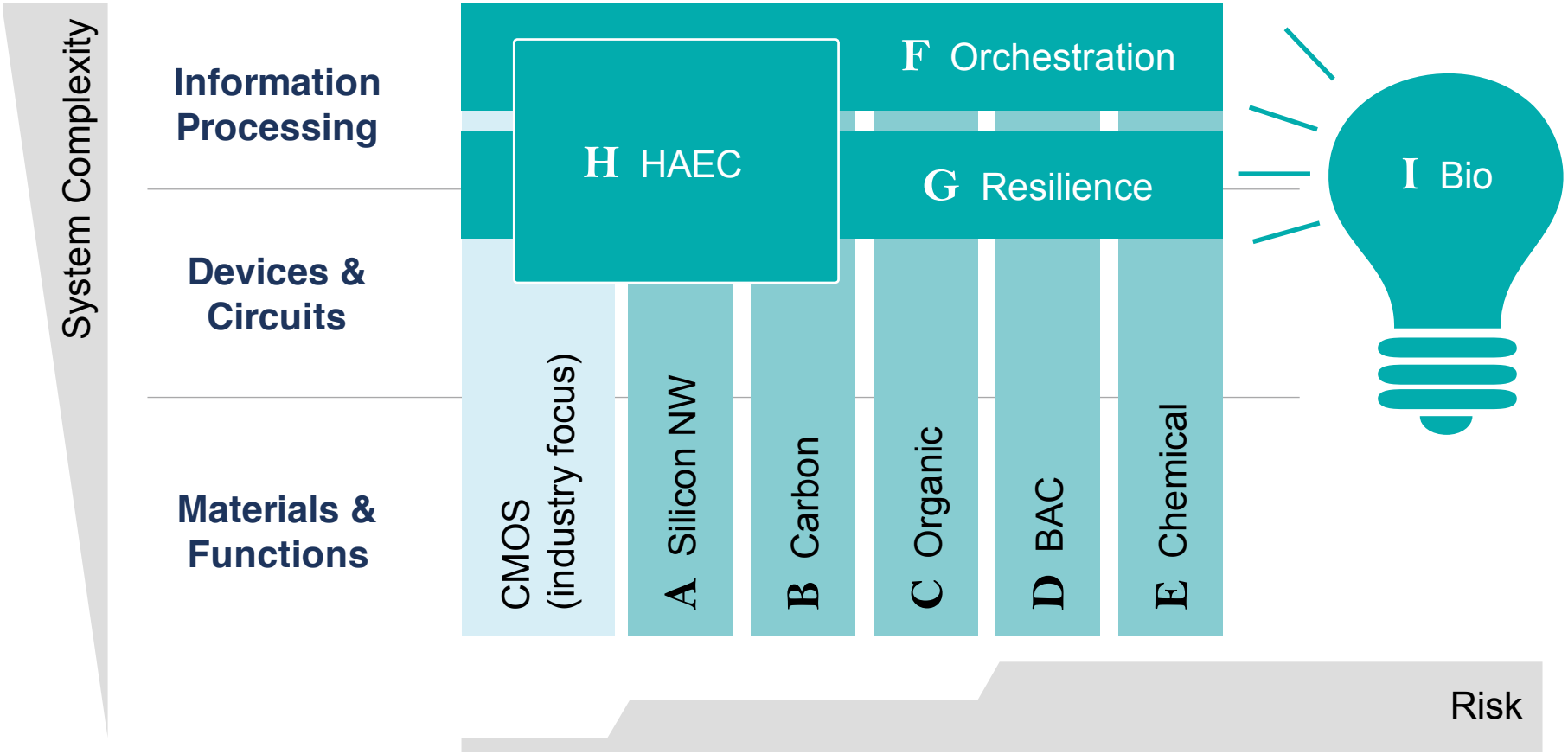


Organic Path
Organic electronics for information processing



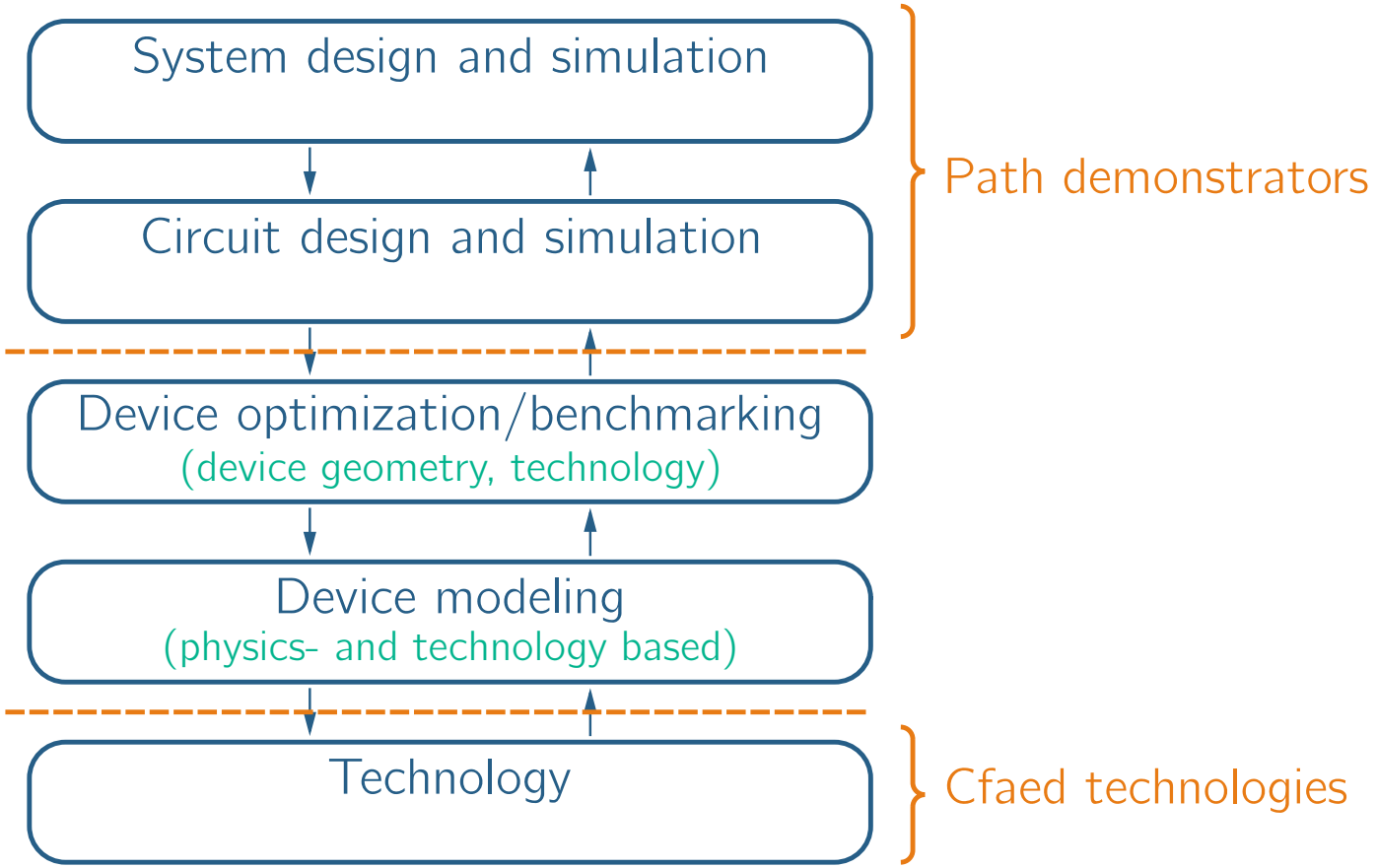
Chemical Information Processing Path
Building chemical processors

Cfaed vision



Cfaed vision: From material science to system design

Role of Device Modeling in the Cfaed



Device and circuit behavior predicted by the models must match the behavior after fabrication.

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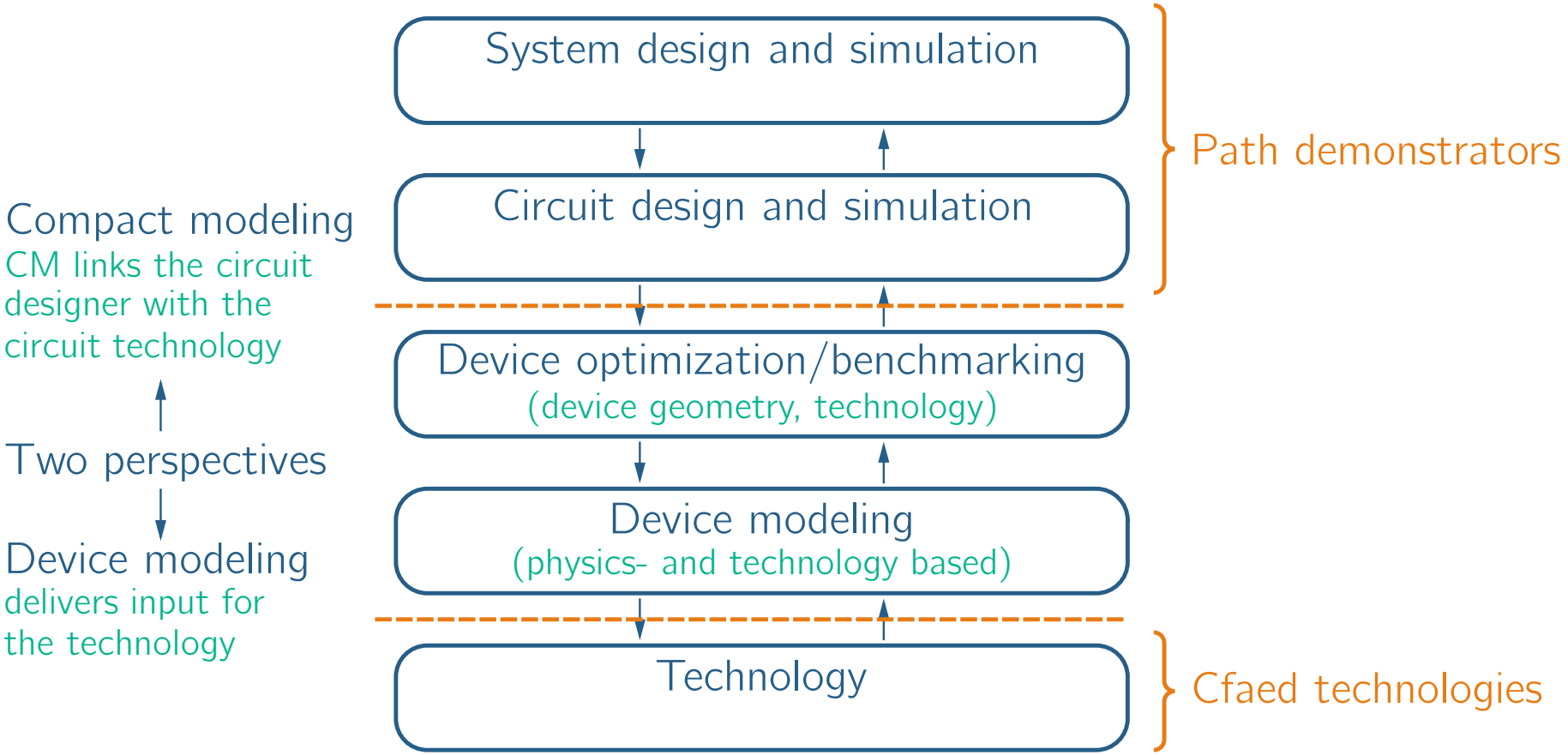

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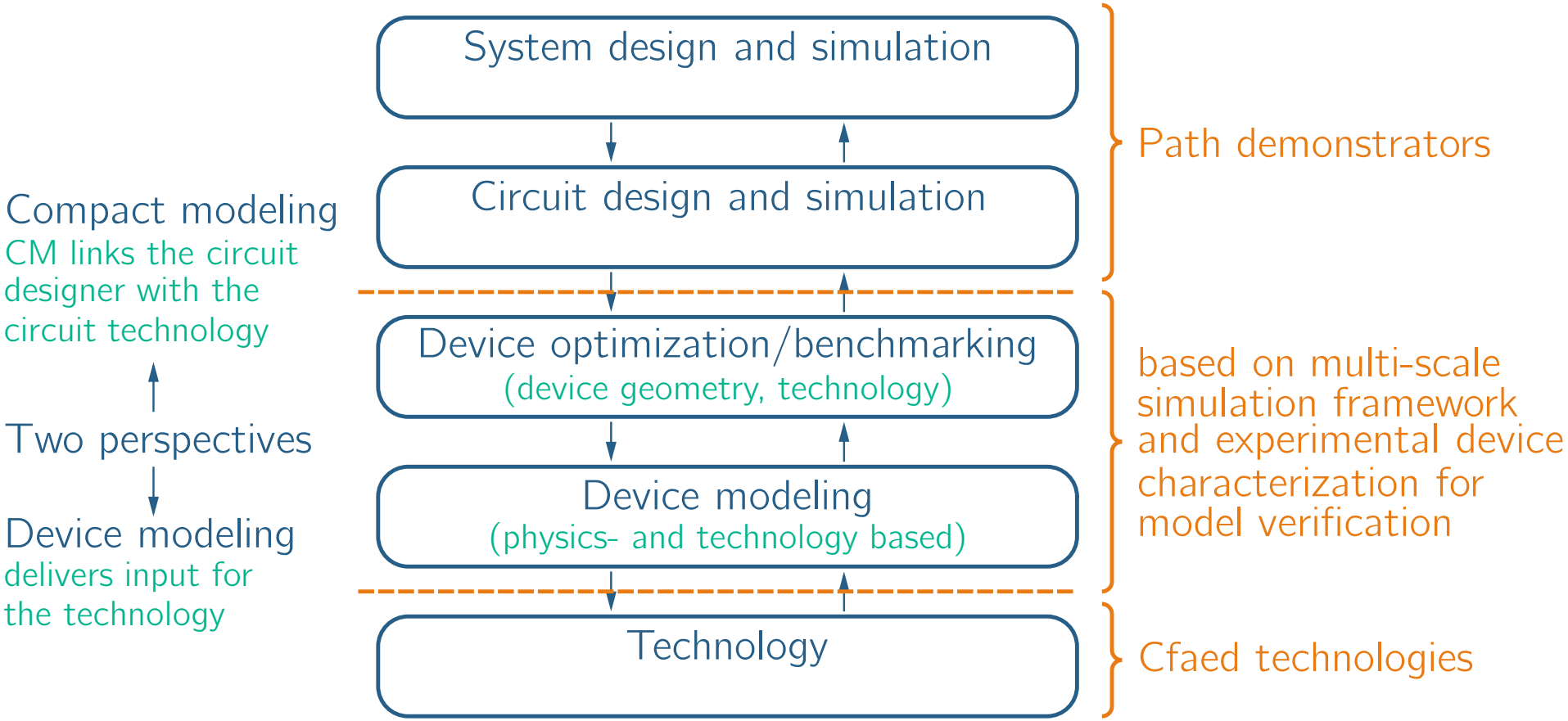

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Role of Device Modeling in the Cfaed

General tasks and goals:

1. Development of multi-scale simulation framework and application for device optimization
2. Development of compact models for circuit design
3. Development of suitable electrical device characterization techniques for device performance evaluation and model verification
4. Benchmark circuit design studies for evaluation of performance potential

→ Support technology and circuit design within Cfaed

Tight cooperation with technology groups essential for success!
Reasonable number of devices with reproducible behavior needed!

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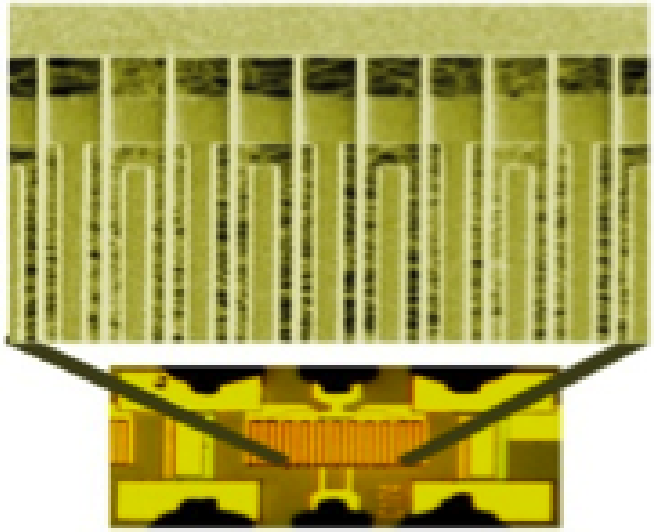
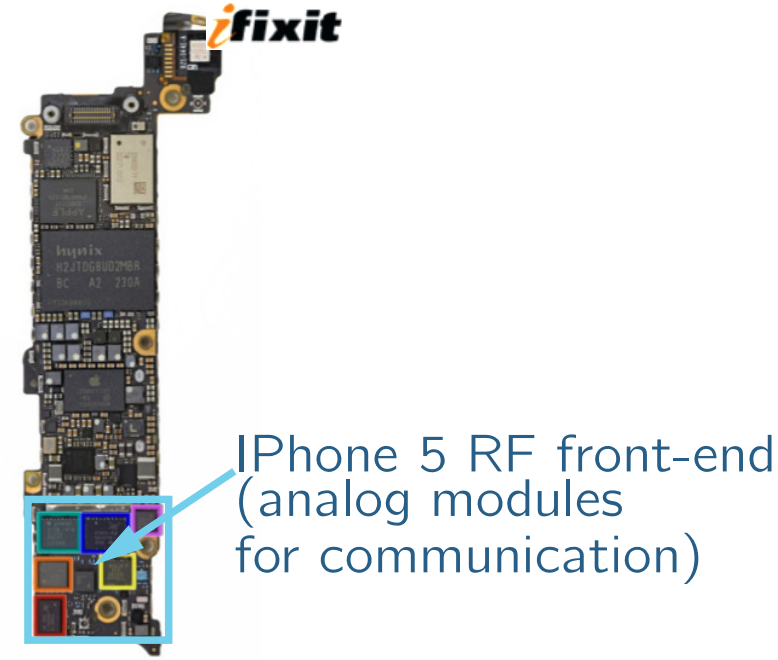
Modeling Activities in the Carbon Path

Modeling Group for Emerging Electronics



Motivation for Carbon Path

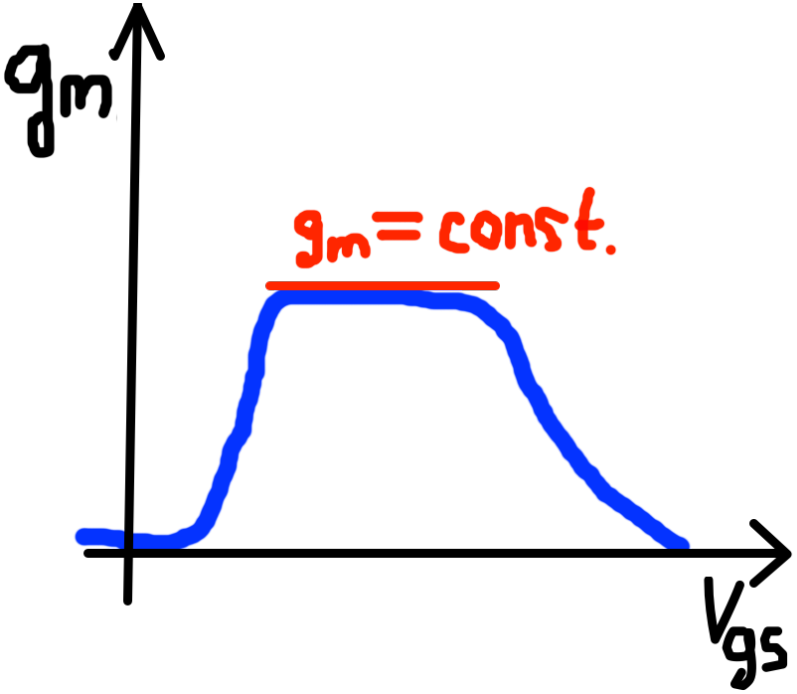


Requirements on RF front-end technology:

- High data volume and high-speed data transmission
- Technology option: provide transistors with high device linearity (i. e. constant g_{m}) working in GHz regime
- CNTFETs provide high linearity @ GHz under specific conditions!

Motivation for Carbon Path

IPhone 5 RF front-end (analog modules for communication)



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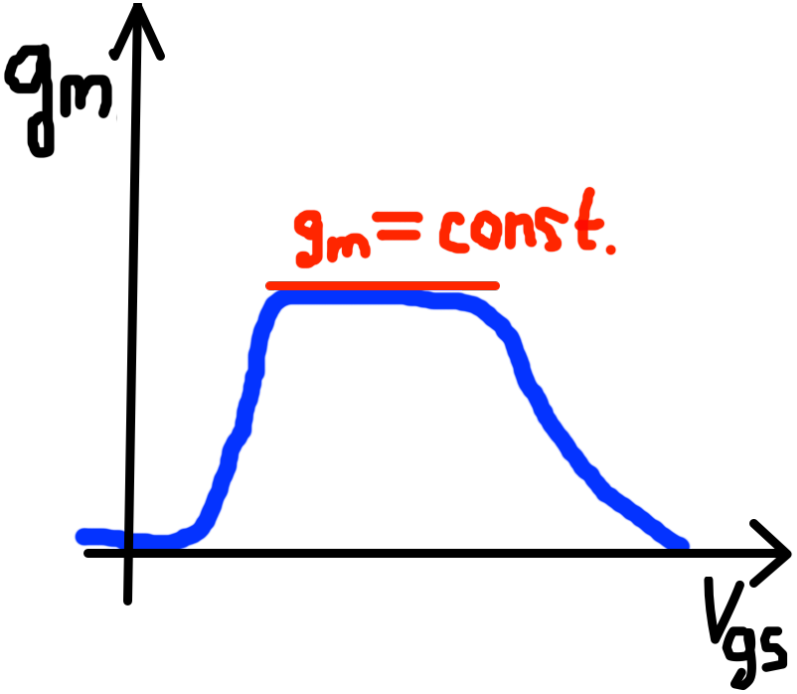

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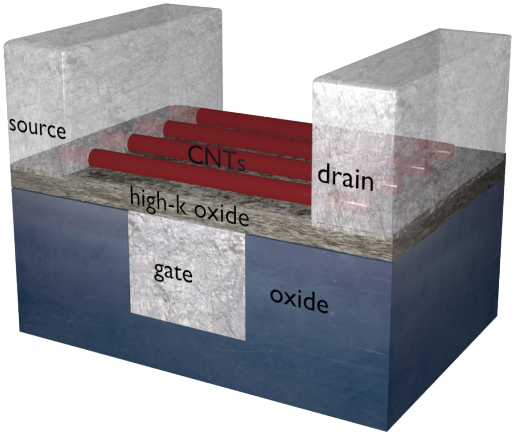
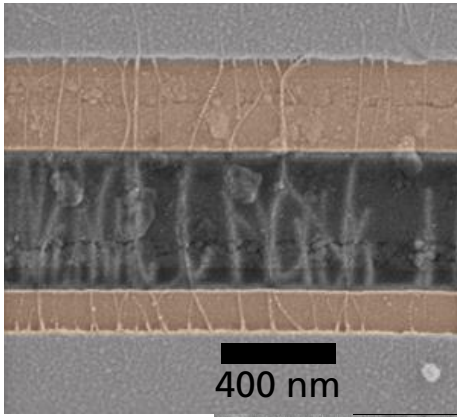
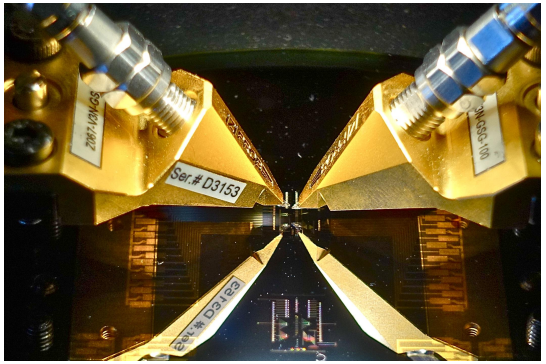
Device design for GHz operation



GHz operation demands specific device design - optimization by multi-scale simulation framework



Fabrication of HF layout according to suggestions of modeling group



Experimental data shows 3 GHz performance! (SoA is 5 GHz @ same channel length)

Still room for technology improvements!

However, early circuit design studies mandatory for reasonable evaluation of performance potential of CNTFET technology!

CNTFET compact model essential!

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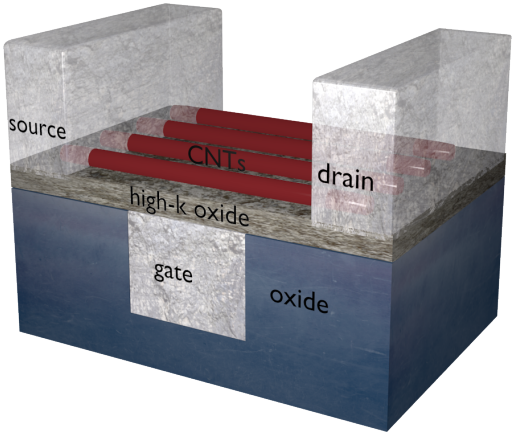

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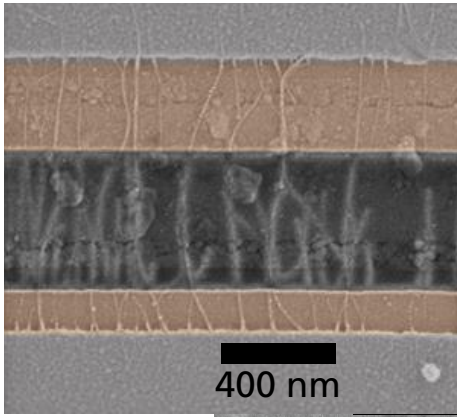

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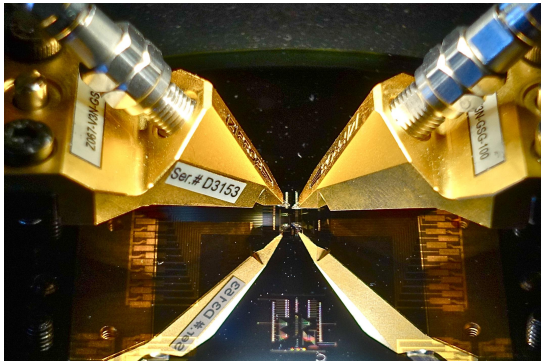

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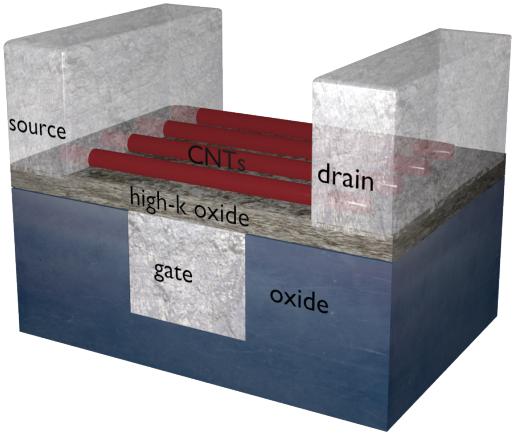

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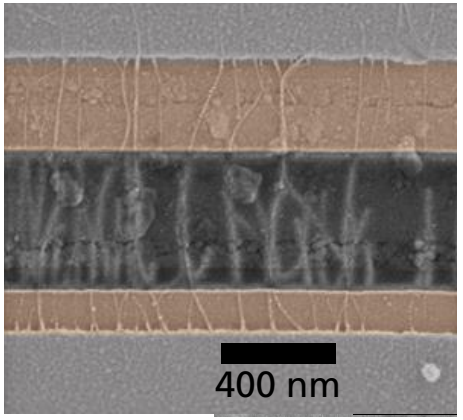

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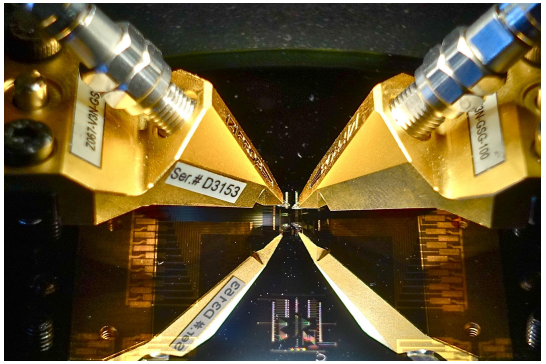

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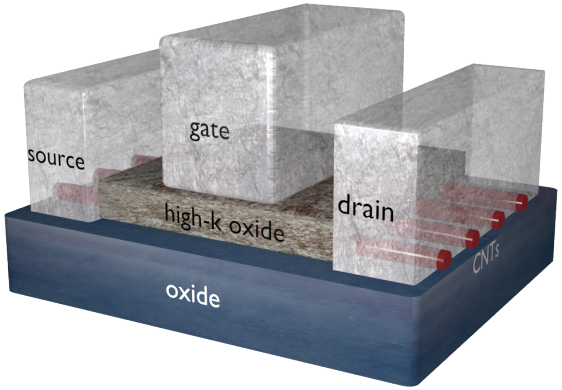
CNTFET compact model essential!

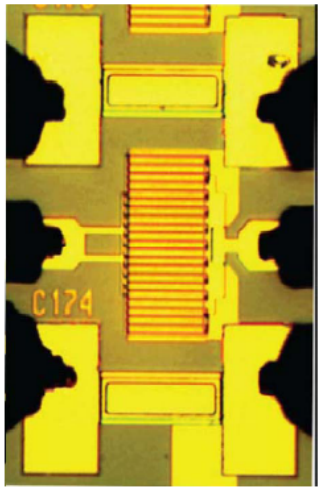
CNTFET compact model: CCAM

52 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 62, NO. 1, JANUARY 2015

A Semiphysical Large-Signal Compact Carbon Nanotube FET Model for Analog RF Applications

Michael Schröter, *Senior Member, IEEE*, Max Haferlach, Aníbal Pacheco-Sanchez, Sven Mothes, Paulius Sakalas, *Member, IEEE*, and Martin Claus

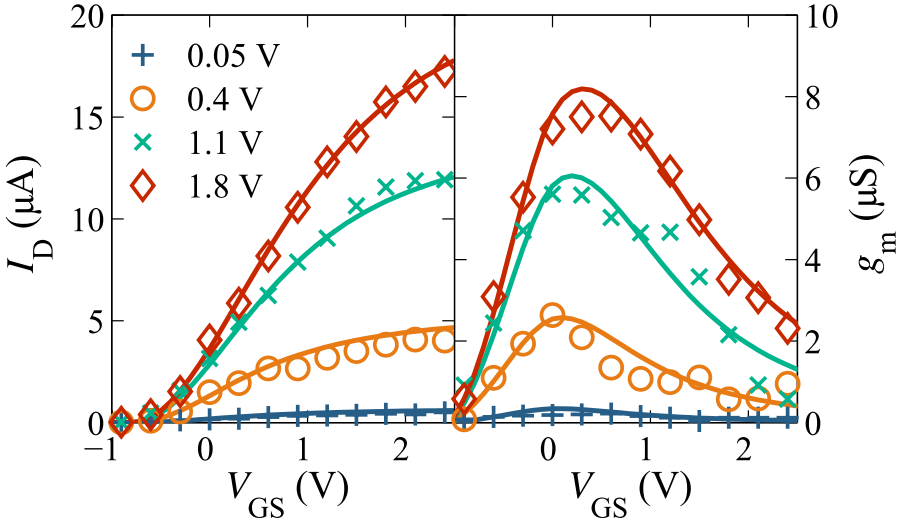




CNTFET compact model: CCAM

CCAM – compact model (CM) for CNTFETs

- Semi-physical compact model
- Includes all layout parasitics
- Worldwide unique CM which allows analog HF circuit design
- Enables circuit design and optimization



Comparison between experimental data and compact model

Availability

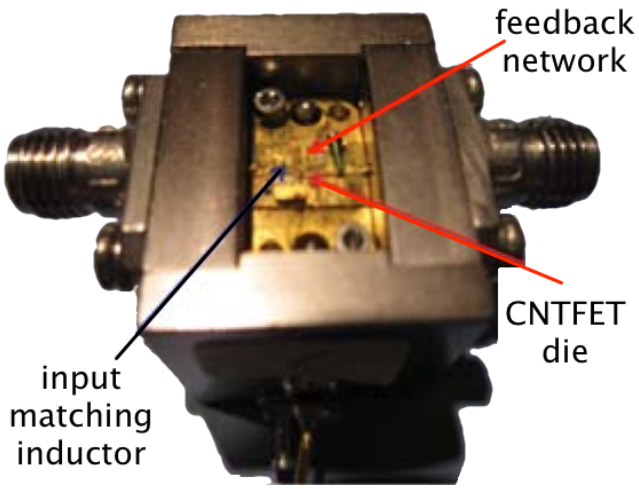
- Various PDKs for circuit design ready for use
- Release of CCAM at nanohub.org

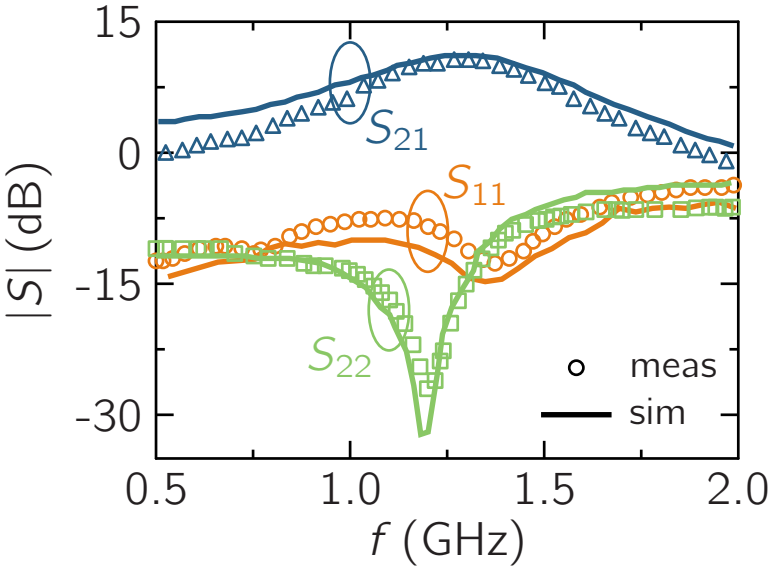
nanoHUB.org an NCN project ONLINE SIMULATION AND MORE FOR NANOTECHNOLOGY

NEEDS NANO-ENGINEERED ELECTRONIC DEVICE SIMULATION NODE

Circuit results - L-band RF amplifier[2]

- First CNT-based single-stage L-band RF amplifier
- 11 dB linear gain with 10 dB input/output return loss at 1.3 GHz



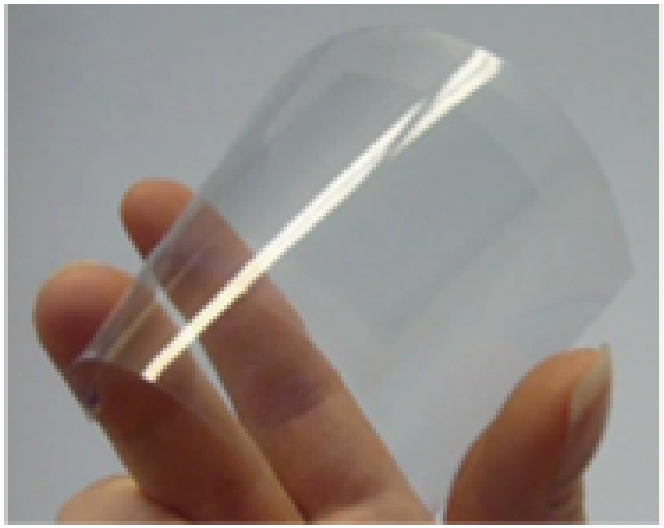


- Good matching between experimental results and model

[2] M. Eron, ..., M. Schröter, "An L-band carbon nanotube transistor amplifier", Electronics Letters, Vol. 47(4), 2012.

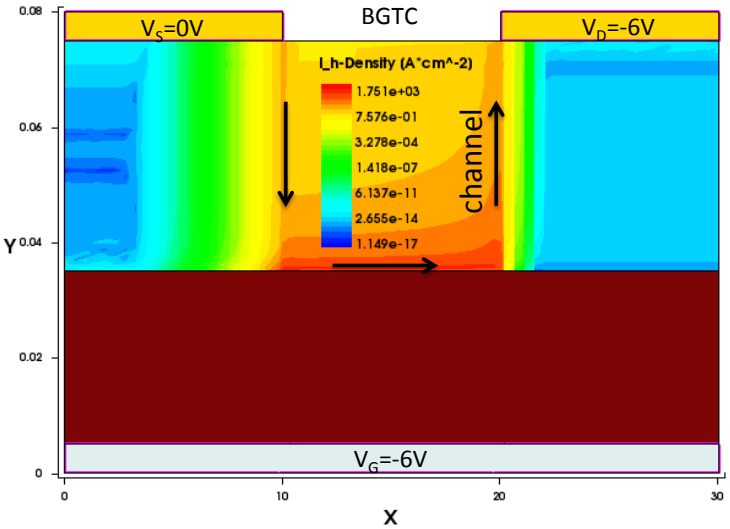
Modeling Activities in the Organic Path

Modeling Group for Emerging Electronics

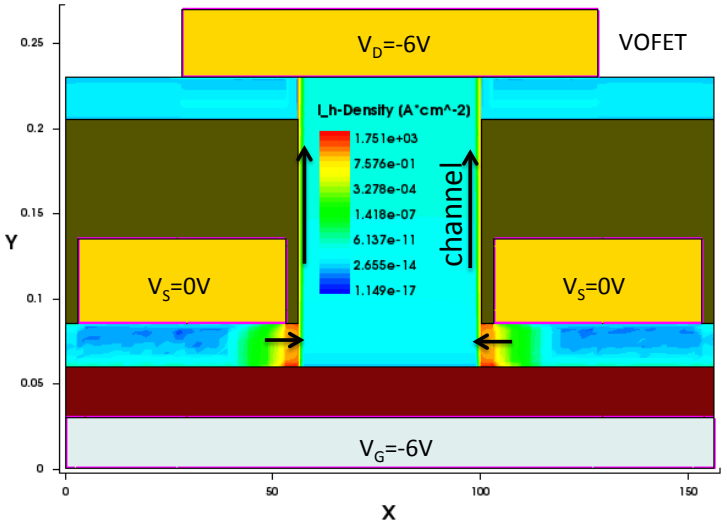


Structural optimization of organic FETs

- Experimentally verified modeling and simulation platform
- Guiding technology development by providing optimized device architectures
- Close collaboration with technology groups within Cfaed



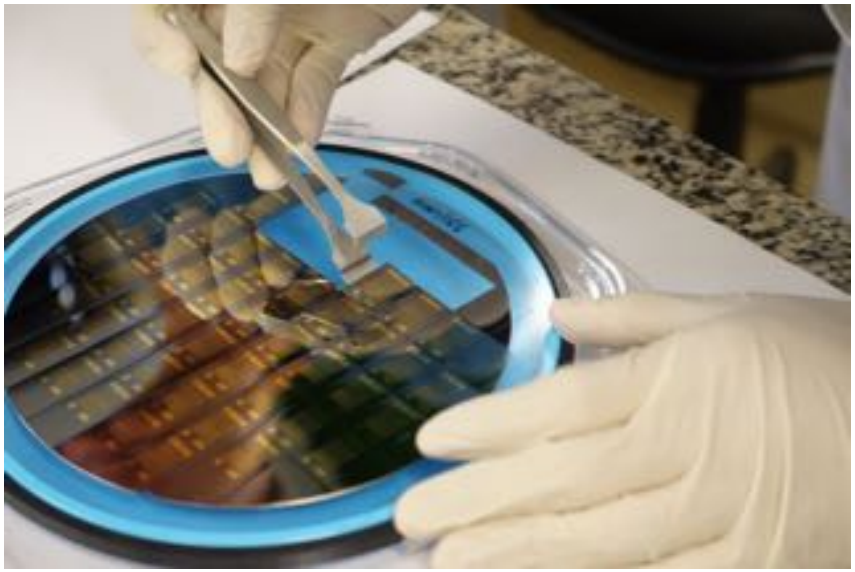
Current flow in a bottom-gate top-contact architecture.

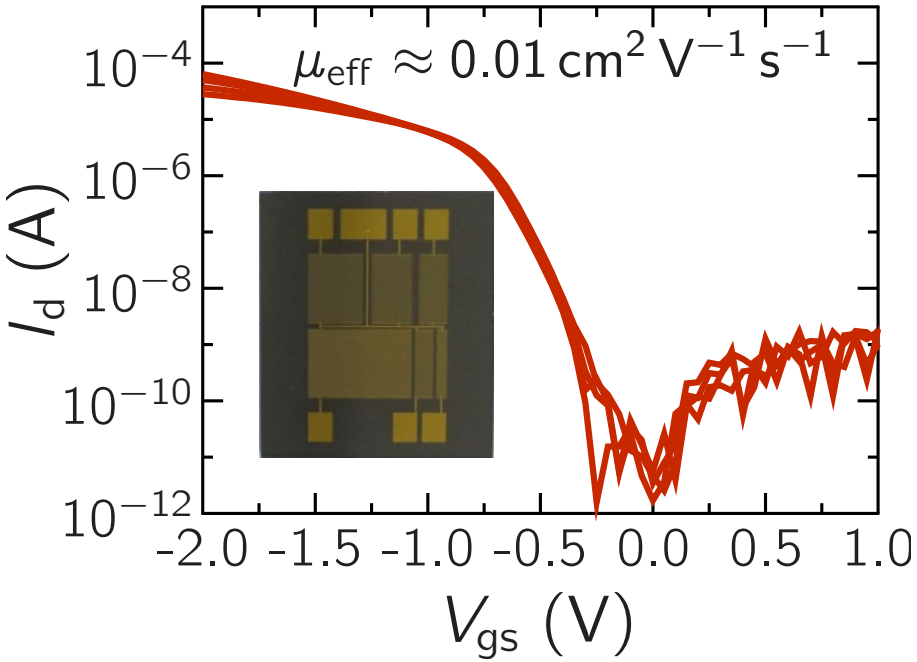


Current flow in a vertical architecture.

Design of test structures for material screening

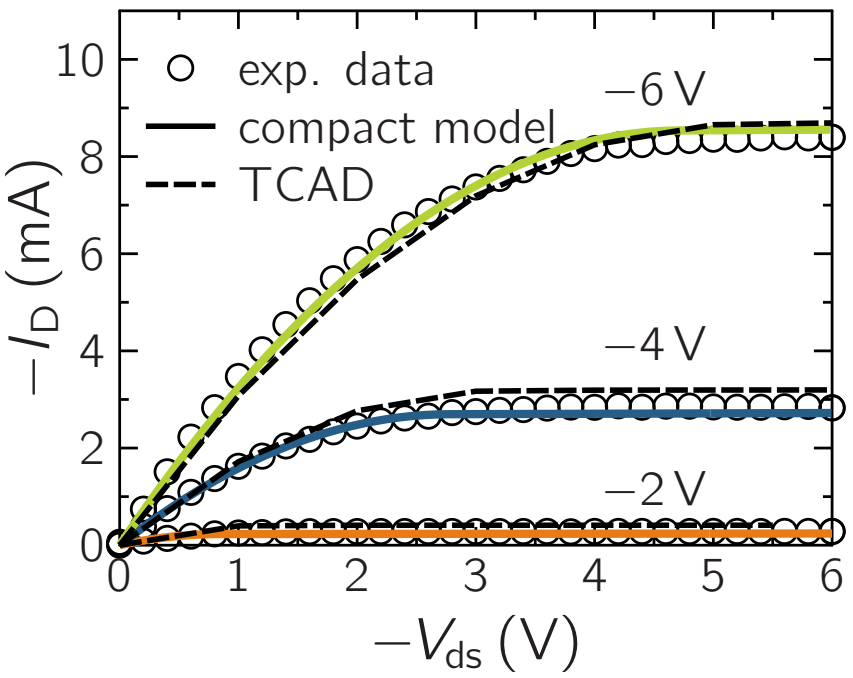
- Fabrication TCAD optimized test structures for screening of organic materials
- Large number of identical test structures allows excellent model verification





Compact modeling for circuit design

- Compact model development based on experimental data and TCAD
- Good agreement between experimental data, calibrated TCAD and compact model
- However, large variation in organic materials makes unified physics-based approach difficult



Cfaed focussed poster session

A. Pacheco	Contact resistance extraction method and mobility definitions for carbon nanotube field-effect transistors
S. Mothes	Toward RF-linearity in Schottky barrier CNTFETs
M. Claus	Multi-scale Simulation Framework for CNTFETs
G. Darbandy	Compact Model and Device Design of OFETs and VOFETs
G. Darbandy	Simulation and Modeling of reconfigurable NW FETs
T. Nardmann	Compact Modeling and Experimental Characterization for Ultra-High Data Transmission
A. Pawlak	Device Modeling for CoolBaseStation ICs