Analysis and modelling of wafer level process variability in advanced FD-SOI devices, using split C-V and gate current data

Krishna Pradeep¹, ², Theano A. Karatsori², Thierry Poiroux³, André Juge¹, Patrick Scheer¹, Gilles Gouget¹, and Gérard Ghibaudo²

krishna.pradeep@st.com

¹STMicroelectronics, Crolles Site, 850 rue Jean Monnet, 38926 Crolles, France
²IMEP-LAHC, MINATEC Campus, 3 Parvis Louis Néel, 38016 Grenoble, Cedex 1, France
³CEA-Leti, MINATEC Campus, 38054 Grenoble Cedex 9, France
Outline

• Introduction.
• Split C-V based process parameter extraction.
• Gate current.
• Statistical modelling.
• Conclusion.
Outline

• Introduction.
  • Split C-V based process parameter extraction.
  • Gate current.
  • Statistical modelling.
• Conclusion.
The concern

- **Variability:** growing concern with scaling.
  - How to effectively account for it in design?
The concern

- **Variability: growing concern with scaling.**
  - How to effectively account for it in design?

- **Global**
  - Lot to lot variation.
  - Wafer to wafer variation.
  - Die to die variation.

- **Local**
  - Intra die variation.
The concern

• **Variability: growing concern with scaling.**
  – How to effectively account for it in design?

  • **Global**
    • Lot to lot variation.
    • Wafer to wafer variation.
    • Die to die variation.

  • **Local**
    • Intra die variation.
FD-SOI

- Key contender for sub-32 nm nodes.
  - Low power, IOT applications, ...

Outline

• Introduction.
• Split C-V based process parameter extraction.
• Gate current.
• Statistical modelling.
• Conclusion.
Vertical thicknesses
Automated extraction from slope of $Q_i/C$ vs $Q_i$ plot

Vertical thicknesses

On-wafer trends

Similar trends for PFET and NFET.

Ground plane vertical doping profile

\[ \frac{1}{C_{bg}^2} = \frac{1}{C_{stack}^2} + \frac{2}{q\varepsilon_{Si}N_a} \left( V_{bg} - V_{fbb} \right) \]

[Ghibaudo et al., T-SM 2000].

- \( C_{bg} \ (V_{bg}) \) gives the depletion depth, \( x_{dep}(V_{bg}) \).
- The vertical doping profile obtained by combining these.

Ground plane vertical doping profile

Highly perturbed by measurement noise, close to accumulation.

Lateral dimensions

- $\Delta C_{gc} = C_{gc}(V_g = V_T + offset) - C_{gc}(V_g = V_T - offset)$.
  - $V_T$ is the threshold voltage.
- $\Delta C_{gc} = \frac{\varepsilon_{ox}}{T_{ox}} (L - \Delta L)(W - \Delta W)$.
- Linear regression with $W$ (for constant $L$) and $L$ (for constant $W$).
- $L_{ov}$ from overlap component of parasitic capacitance.

$L_{eff} = L_{design} \times shrink - \Delta L$
$W_{eff} = W_{design} \times shrink - \Delta W$
$L_{poly} = L_{eff} + 2L_{ov}$

Lateral dimensions

On-wafer trends

Similar trends and values observed for PFET and NFET (except for $L_{\text{overlap}}$).

Outline

• Introduction.
• Split C-V based process parameter extraction.
• Gate current.
• Statistical modelling.
• Conclusion.
Equivalent single trapezoidal barrier model

- \( I_g = f \times Q_i' \times T_r \times W \times L \).
- Gate transparency modelled using an equivalent single trapezoidal barrier.
  - Thickness: \( t_{ox} \times HK \).
  - Barrier height: \( A \times \phi_{ox} \).
  - \( T_r = \exp \left( - \frac{t_{ox}HK\sqrt{A}}{\lambda_{ox}} + \frac{Q_i' t_{ox}^2 HK^2}{4\varepsilon_S \lambda_{ox} \phi_{ox} \sqrt{A}} \right) \).
  - \( \lambda_{ox} = \frac{1}{1.5 \times K_{ox} \sqrt{\phi_{ox}}} \).

$t_{IL}, t_{HK}$ variance segregation using C-V & $I_{g}$

- Using $\ln \left( \frac{I_{g}}{Q_i} \right) = \ln f + \ln T_r$:
  - Intercept of linear fit of $\ln T_r$ with $Q_i$:
    \[
    \left( -\frac{t_{IL}}{\lambda_{IL}} - \frac{t_{HK}}{\lambda_{HK}} \right).
    \]

- $\lambda_{IL}^2 \sigma_{\text{Intercept}}^2 = \sigma_{t_{IL}}^2 + \left( \frac{\lambda_{IL}}{\lambda_{HK}} \right)^2 \sigma_{t_{HK}}^2$.

- From split C-V:
  - $\sigma_{t_{ox}}^2 = \sigma_{t_{IL}}^2 + \left( \frac{\varepsilon_{IL}}{\varepsilon_{HK}} \right)^2 \sigma_{t_{HK}}^2$.

- Can extract $\sigma_{t_{IL}}$ & $\sigma_{t_{HK}}$ from these.

- **28 nm FD-SOI**:
  - $W/L = 2 \mu m/10 \mu m$.
  - $\sigma_{t_{IL}} = 0.004 \text{ nm}$.
  - $\sigma_{t_{HK}} = 0.014 \text{ nm}$.

- **14 nm FD-SOI**:
  - $W/L = 5 \mu m/5 \mu m$.
  - $\sigma_{t_{IL}} = 0.005 \text{ nm}$.
  - $\sigma_{t_{HK}} = 0.092 \text{ nm}$.

Outline

• Introduction.
• Split C-V based process parameter extraction.
• Gate current.
• Statistical modelling.
• Conclusion.
Statistical modelling of global variability

• For any property $X$ of the device whose variability is being studied.
  – $\Delta X/X \equiv \ln \frac{X}{X_0}$ where $X_0$ is the property of the device at the center of the wafer.
  – Standard deviation, $\sigma(\Delta X/X)$.
  – $\sigma \left( \frac{\Delta X}{X} \right)^2 = \sum_{P_j} \left( \frac{\partial \ln X}{\partial P_j} \right)^2 \sigma(P_j)^2$.

• Sensitivity to each parameter: $\text{abs} \left( \frac{\partial \ln X}{\partial P_i} \right)$.

• Percentage contributions:
  – $\%_{P_i} = \frac{(\partial \ln X / \partial P_i)^2 \sigma^2(P_i)}{\sum_j (\partial \ln X / \partial P_j)^2 \sigma^2(P_j)} \times 100$.

• This can be applied to capacitance.
  – Using Leti-UTSOI compact model.

• This can be applied to gate current.
  – Using equivalent single trapezoidal barrier model.

Capacitance statistical model

Long-wide NFET

- Good fit obtained with the model.
- Fitted values close to initial guesses.

Parameters used:
\( V_{fb}, V_{fbb}, T_{Si}, T_{BOX}, T_{OX}, \ln N_{well} \)

Capacitance percentage contributions

Long-wide NFET

- $T_{ox}$ dominant in strong inversion.

- RBB, moderate inversion: $V_{fb}$ dominant.
  - Even stronger at $V_b = 0$ V.

- Very strong FBB, moderate inversion: $T_{Si}$ dominant.

The proposed model can reproduce the measured variance quite well.

Parameters used:
- $V_T$
- $t_{ox}$

Ig percentage contributions

14 nm FD-SOI

- Above threshold, the Ig variation is controlled almost completely by the barrier thickness.
- Below threshold, both $V_T$ and barrier thickness have similar contributions.
  - $V_T$ slightly dominating barrier thickness.

Outline

• Introduction.
• Split C-V based process parameter extraction.
• Gate current.
• Statistical modelling.
• Conclusion.
Conclusions

• Robust, efficient split C-V parameter extraction methods.
  – Automated extraction on large amount of measurement data.

• Gate leakage current model proposed.
  – Shown to work in different technology nodes and different geometries.
  – Can extract variance of IL and HK layers.

• Statistical model.
  – Works for both capacitance and Ig wafer level global variability.
  – Can analyse the dominant source of variability at each bias condition.
  – Can be further extended to Id or any other property, using Leti-UTSOI compact model.
THANK YOU
Appendix
Calibrated Leti-UTSOI

Long-wide NFET

- Good fit of the measurements obtained with Leti-UTSOI at different $V_b$ values.
- Used to calculate the sensitivities.

Percentage contribution of $T_{Si}$

Leti-UTSOI results

- The change in the sign of sensitivity around the threshold voltage.
  - Responsible to make the contribution go to zero at this bias.