Advanced PDK and Technologies accessible through ASCENT

MOS-AK
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The Challenge

Increasingly (in)accessible nodes as scaling progresses...

Cost of Mature Designs

IBS, July 2018

GF Puts 7nm On Hold

Foundry forms ASIC subsidiary as it focuses on 14nm/12nm and above.

AUGUST 27TH, 2018 - BY: MARK LAPIEDUS

GlobalFoundries is putting its 7nm FinFET program on hold indefinitely and has dropped plans to pursue technology nodes beyond 7nm.

The moves, which mark a major shift in direction for the foundry, involve a headcount reduction of about 5% of its worldwide workforce. At the same time, the company is also moving its ASIC business into a new subsidiary.

As a result of GlobalFoundries’ announcement, there are only three foundries that will provide 10nm/7nm technologies in the near term—Intel, Samsung and TSMC. There are also fewer foundry customers that can afford advanced nodes. This, in turn, has some ramifications throughout the equipment industry and supply chain.

GlobalFoundries, which originally announced its 7nm plans in 2016, said...
The Challenge

Nanowire Transistors,
Colinge & Greer,
Cambridge University Press 2016
A part of the solution ... an infrastructure for the global nanoelectronics modeling, characterization, and design communities.

J. Greer, ESSDERC 2017
The Access Providers

State-of-the-art 14 nm FDSOI CMOS & nanowire
Advanced transistor and interconnect test structures
Electrical & nano-characterization platforms

Fabrication facilities for nanowires & 2D materials
Advanced nanowire and nano-electrode test structures
Electrical & nano-characterization platforms

State-of-the-art 14 nm FinFET CMOS
Advanced transistor and interconnect test structures
Electrical & nano-characterisation platforms

www.ascent.network
Items for Device Analysis

300mm wafers with planar FDSOI and Nanowire devices

SPICE models and model cards for digital: target and preliminary

- 14nm FDSOI
- 10nm FDSOI
- 10nm FFSOI
- 7 nm Stacked-nanowire

TCAD decks

- FDSOI MOSFET
- Trigate SOI Nanowire
- GAA Nanowire MOSFET (mainly electrostatics)
Items for Circuit Performance Analysis

- Preliminary PDK for Full custom IC design
  - 14nm planar FDSOI technology
  - 10nm planar FDSOI technology (preliminary)
- DK for IC demonstrators
  - 28nm FDSOI technology (ST Microelectronics)
- Near future:
  - PDK 10nm including libraries
Electrical Characterisation Capabilities

- Parametric testers with 300mm full auto probers
- General purpose I(V)-C(V) 200/300mm testers
- Temperature range for test on wafers: 2K ⇒ 600°C
- Test systems for memories
- HF tests up to 40 MHz, Noise measurements
- Reliability tests: hot carriers, TDDB, charge pumping, ...
- Internal Photo Emission
- Electrical test under calibrated strain
- High power tests (10kV, >100A) on 300mm prober
- Deep Level Transient Spectroscopy
- Electrostatic discharges, Electromigration

450m²
Access to LETI 300mm wafers with Nanowire devices for characterization and study of advanced nanodevices in the characterization facilities of the Nanoelectronics Lab of Univ. Granada.
Range of cleanrooms designed for flexible process & product development

- Silicon MOS Fabrication
- MEMS Fabrication
- Compound Semiconductor Fabrication
- Photonics Fab Training Facility
- e-Beam Lithography
- Non-standard nano-processing
Fab Access
Access to Tyndall FlexiFab for non-standard processing

Test Chips
Si nano-wire test chips with range of devices

Electrical Characterisation Access
Access to Tyndall electrical test labs

Physical Characterisation Access
Access to Tyndall device characterisation facilities
Imec’s offer

Access to state of the art process technology

Main features: Bulk finFET, Replacement Metal Gate, S/D epi with Local Interconnect and silicide-last integration using single metal BEOL
Imec’s offer

Material for Device Analysis

- 300mm wafers with Bulk FinFET devices
- Silicon EPI nFET/pFET CMOS fully integrated vehicle
- Embedded Si:P / SiGe S/D CMOS fully integrated vehicle
- Replacement Metal Gate [RMG] with Local Interconnect
- Single level BEOL metal
- Digital and Analog/RF existing test chips
- Complete suite of test structures for Reliability/ESD/Matching/Local Layout effects/…
- Standard devices up to circuit level [Ring-Oscillators, …]
- State-of-the-art bulk FinFET device baseline

![FET arrays, Matching, LDE](image1)

![STD Test-chip Content](image2)

![Testchip Documentation and Simulation](image3)

![State-of-the-Art Device](image4)

FinFET test chip documentation

- Documentation of process assumptions for the test chips
- Inventory of test structure types available on the test chips
- Access to test structures data

Electrical Characterization Capabilities

Available systems and methods:

- >500 m² of test labs, ~25 semi-auto/manual 300mm probers
- Statistical data treatment in JMP
- Fully automatic 300mm parametric testers
- Semi-automatic 300mm parametric testers
- Temperature range for test on wafers 77/10K → high T
- Fast Pulse testing, Self-Heating characterization
- HF tests up to 50 GHz
- Noise measurements
- Reliability tests: hot carriers, TDDB, charge pumping,…
- High power tests (13kA), >100A on 300mm prober
- Electrostatic discharge LAB

![Semi auto tester 300mm chuck with T capability](image5)

![Full Auto tester 300mm chuck with T capability](image6)

![RF semi auto 300mm tester](image7)

Scientific & technical support

Whenever necessary and upon request of the User, imec can offer scientific support for in-depth data interpretation.
How to Access

Step 1 Sign Up
Step 2 Enquire
Step 3 Apply
Step 4 Selection
Step 5 Access
Step 6 Report
Step 1- Sign-Up

Sign-up Form

Please fill your details below. By signing up, you become a member of the ASCENT network. Members will receive specific information by e-mail on ASCENT technologies, details about upcoming events and news.

For a more detailed technical enquiry regarding access, please fill the ASCENT Enquiry form.

Your name *

Your e-mail address *

Comments

How did you hear about ASCENT?

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347 members of ASCENT Network
Recent on-line survey to all members - 68 replies

- 85% : Yes, programme is relevant to their research
- 75% : Have not applied for access yet
- 44% : plan to apply
- 88% : Rated application process at highest option
- 100% : Would recommend this programme to colleagues
What’s new for MOS-AK 2018 in Dresden?

Leti presents an advanced SPICE model for 3D mosfets: the Nanowire Surface Potential Model (Leti-NSP)
• **State-of-the-art today for advanced design (<7 nm): BSIM-CMG, limited to FinFET and 1 squared NW**

• **Our solution is Leti-NSP model dedicated to advanced GAA MOSFET. Leti-NSP model can simulate:**
  - Vertically stacked GAA MOSFET (nanosheet and/or nanowire)
  - Vertical channel GAA MOSFET (nanosheet and/or nanowire)
  - FinFET / Trigate MOSFET (SOI & bulk)
• Advances offered by Leti-NSP: stacked nanosheet with variable W & Tch GAA MOSFET architecture and its asymptotic cases

NSP model only supports all nanosheet GAA CMOS technologies
Overview of Model features (1/3)

• For all device sizes

Model features: Leti-NSP model v1.0.0

Interface states

Quantum mechanical effect (GAA, finfet)

Channel doping effect

Management of SiGe channel for pfet

Mobility model including sidewall effects

Temperature scaling and self-heating effect

Validation of quantum confinement modeling

Mobility model including sidewall effects

Introduction to Leti-NSP model for 3D MOSFETs – June 1st, 2018
• **Short channel effects**

Model features: Leti-NSP model v1.0.0

Threshold voltage roll-off
L-scaling of mobility model
Drain Induced Barrier Lowering
Velocity saturation
Channel length modulation in saturation
Series resistances with bias dependence
Overview of Model features (3/3)

- Other parasitic effects

Model features: Leti-NSP model v1.0.0

- Inner and Outer fringe capacitances
- All external parasitic capacitances including device to substrate capacitances
- External access resistances
- Gate resistance with scaling effects
- Gate tunneling currents
- GIDL/GISL currents
- Junction currents and charges

Dedicated instance parameters for all GAA geometries
Leti-NSP model: Verilog-A code and manual are available

NSP model is ready for standardization (presented to the CMC)
Highlights to Ascent & Advanced models:

- Ascent provides a unique platform for access to advanced technologies, electrical & physico-chemical characterization, models thanks to Leti, Tyndall and IMEC as leading European RTO & European subsidy

- 347 members have already joined. Go ahead, join, to meet your own targets!

As an example of offered platform within ASCENT advanced models → Leti NSP

- Unique SPICE model for 3D Mosfets: from Symmetrical DG to Circular GAA, passing through different aspect ratio of nanosheet MOS

- Stacking possibility is enabled

- Fundamental effects included with brand-new emphasis triggered by customised device features (corner effect, quantum confinement, mobility degradation including sidewall effects...)

- Validated on several technologies.
Join our community:
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Please join us in this exciting opportunity for nanoelectronics research