ANALYSIS AND MODELING OF 1/f NOISE IN IGZO TFTs

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Outline

- Introduction about the origin of Flicker noise
- Results of 1/f noise analysis and modeling in IGZO TFTs
  - Bias and channel length dependence
  - Noise mechanism
- Conclusions

OBJETIVE

- Determine the cause and origin of the noise in
  - IGZO TFTs

- Determine the behavior of noise with
  - V_G
  - L

1/f NOISE

Study of the scalability of noise

Dependence on :

- V_G
- Channel length

Study of the origin of 1/f noise

2 theories

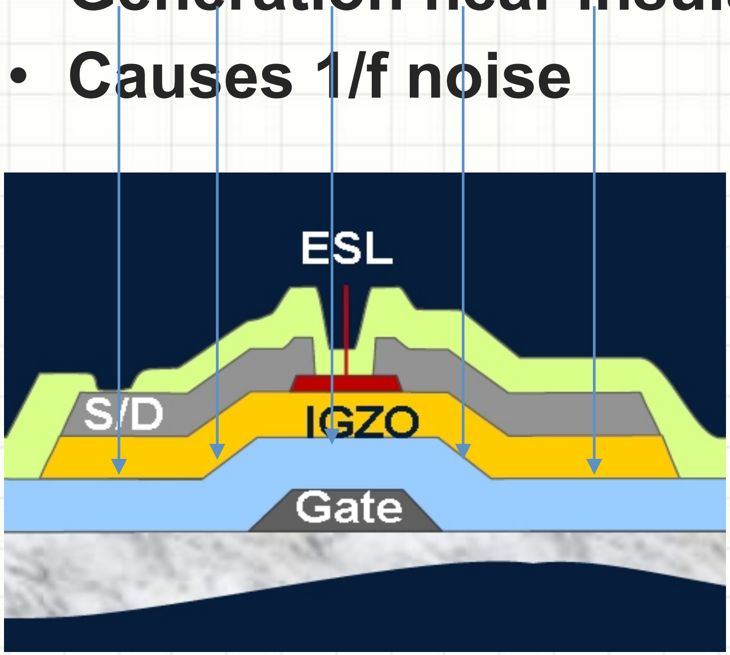
- Mobility fluctuations, $\Delta\mu$
- Carrier number fluctuation, ΔN

Origin of the 1/f noise

Carrier number fluctuation, ΔN

McWhorter Model, 1957

- **Charge trapping and release**
- **Generation near insulating interface**
- **Causes 1/f noise**



IGZO TFT, source www.semind.com

Origin of 1/f noise

Carrier number fluctuation, ΔN

$$S_{ID} = \frac{k^*}{f} \frac{\mu}{C_{ox} L^2} \frac{I_D V_{DS}}{(V_{GS} - V_{th})} \qquad (1)$$

Dimitradis *et al* proposed, for poly-Si TFTs:

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2} V_{DS}^2\right] \qquad (2)$$

Therefore :

$$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f} \frac{1}{C_{ox}^2 WL} \frac{1}{(V_{GS}-V_{th})} \frac{1}{\left[(V_{GS}-V_{th})-\frac{1}{2}V_{DS}\right]} \qquad (3)$$

Origin of 1/f noise

Mobility fluctuations, Δμ

Hooge model, 1969

- **Fluctuations of carriers mobility in the conduction channel.**

Origin of 1/f noise

Mobility fluctuations, Δμ

Hooge proposed

$$\frac{S_i(f)}{I^2} = \frac{S_v(f)}{V^2} = \frac{S_R(f)}{R^2} = \frac{S_\mu(f)}{\mu^2} = \frac{\alpha_H}{fN} \quad (4)$$

$$S_I = \frac{\alpha I^2}{N} \cdot \frac{1}{f} \quad (5)$$

N el number of carriers:

$$N = \frac{C_{ox}WL}{q}(V_{GS} - V_{th}). \quad (6)$$

Therefore:

$$\frac{S_{ID}}{I_D^2} = \frac{q}{C_{ox}WL}\frac{\alpha_H}{f}\frac{1}{(V_{GS}-V_{th})} \quad (7)$$

Devices Analized

- **IGZO TFT**

TNO, HOLST CENTER, The Netherlands

A total of five IGZO TFT were analyzed, all of them with a 100µm channel width and 15, 20, 30 and 50µm channel length, for a better scalability comparison. All the devices have a bottom gate, an insulation thickness of 200nm and an ESL thickness of 100nm, with 5µm design rules.

Origin of 1/f noise

Model by Ghibaudo 1991, Δμ-ΔN

Combination of both theories

- **Proposed:** $$\frac{S_{ID}(f)}{I_D^2} = \left[1 \pm \alpha_s \mu_{eff} C_i \frac{I_D}{g_m}\right]^2 \left[\frac{g_m}{I_D}\right]^2 S_{V_{FB}}(f)$$

- **For a pure ΔN model, the term with α_s is absent**

- **As a result, if $S_{ID}(f)/I_D^2$ and** $[g_m/I_D]^2$ as a function of I_D are parallel, it is because the fluctuation of the number of carriers.

Origin of 1/f noise

Summary:

Mc Whorter Model Δμ	Hooge Model ΔN	Ghibaudo Model Δμ-ΔN
$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f}\frac{1}{C_{ox}^2 WL}\frac{1}{(V_{GS}-V_{th})^2}$	$\frac{S_{ID}}{I_D^2} = \frac{q}{C_{ox}WL}\frac{\alpha_H}{f}\frac{1}{V_{GS}-V_{th}}$	$\frac{S_{ID}(f)}{I_D^2} = \left[1 \pm \alpha_s \mu_{eff} C_i \frac{I_D}{g_m}\right]^2 \left[\frac{g_m}{I_D}\right]^2 S_{V_{FB}}(f)$

Slopes

m = -2

Proportionality

$f\uparrow -1$

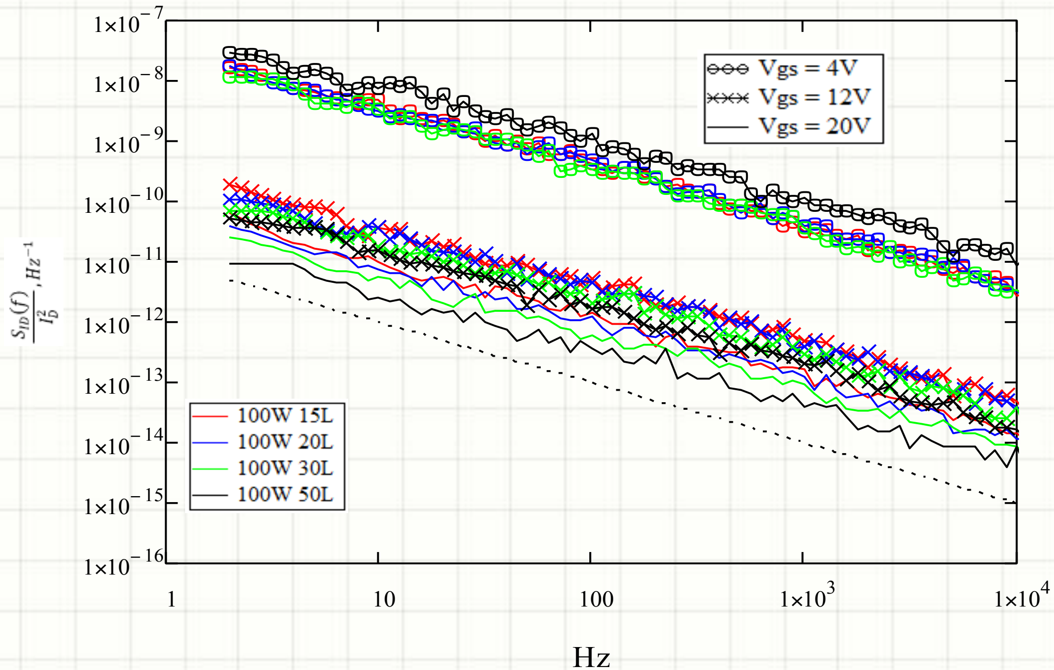
m = -1 m = -1

Scalability

- ↑ L ↓ S_{ID}
- ↑ V_G ↓ S_{ID}

Results, **Bias dependence**

IGZO TFTs follow, $1/f^{\gamma}$, with $\gamma = 1$.

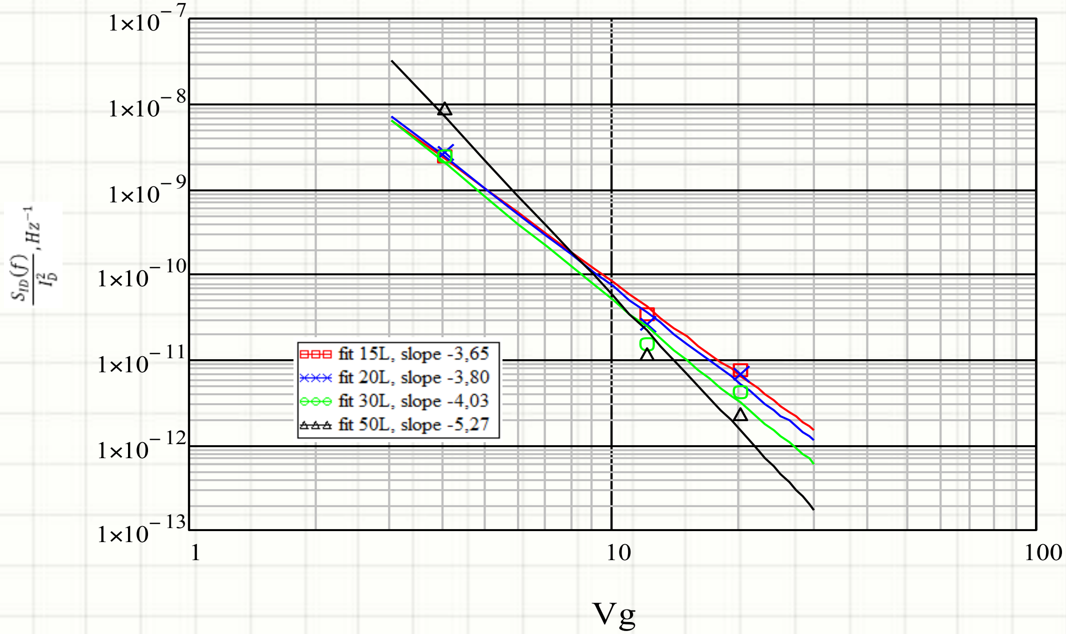


Normalized noise drain current spectral density (S_{ID} / I_D^2) for all targeted devices, measured at the 4, 12 and 20V gate voltage (V_{GS} − Vth) in the linear region of device operation (V_{DS} = 1.0 V). W and L in μm.

Results **Bias dependence**

Dependence on V_G.

TFT IGZO



$S_{ID}(f)/I_D^2$ versus V_{GS} (symbols), their linear approximations (solid lines) and extracted slope values (inset) at 12 Hz for different $(V_{GS} - V_{th})$ values, with V_{DS} = 1 V. W and L in µm.

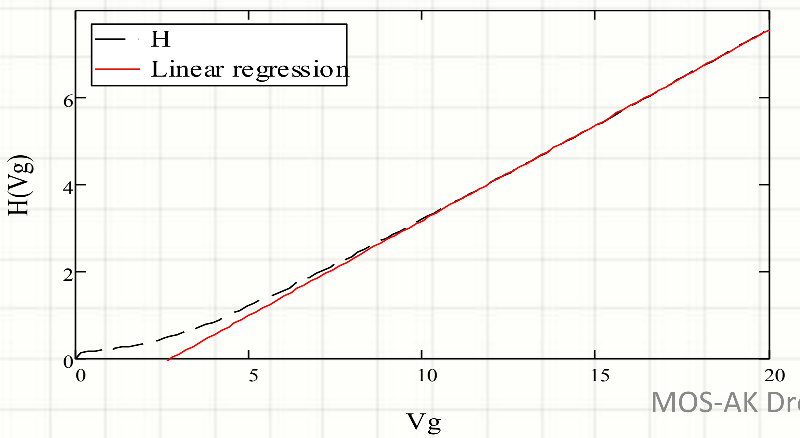
Results, Bias dependence

$$I_{DS} = \frac{W}{L} \cdot C_i \cdot \mu_{FET} \cdot \frac{(V_{GS} - V_T) \cdot V_{DS} \cdot (1 + \lambda \cdot V_{DS})}{\left[1 + R \cdot \frac{W}{L} \cdot C_i \cdot \mu_{FET} \cdot (V_{GS} - V_T)\right] \cdot \left[1 + \left[\frac{V_{DS}}{\alpha_S \cdot (V_{GS} - V_T)}\right]^m\right]^{\frac{1}{m}}}$$

$$\mu_{FET} = \frac{\mu_O}{V_{AA}^{\gamma}} \cdot (V_{GS} - V_T)^{\gamma}$$

Results

- Mobility is a power law of $(V_{GS} - V_{th})$ in IGZO TFTs, as well as I_{DS} at low V_{DS}
- Extraction of threshold voltaje in IGZO TFTs
- $H(V_{GS}) = \int_0^{V_{GS}} I_D(x)\,\mathrm{dx} \,/\, I_{DS}(V_{GS}) = 1/2 + \gamma (V_{GS} - V_{th})$

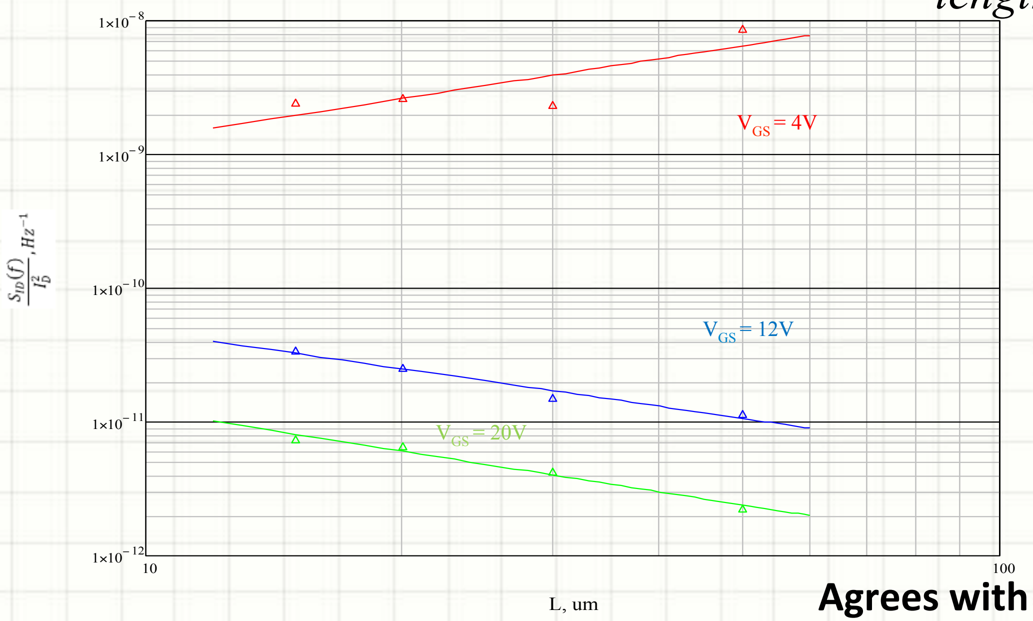


Results, Channel length dependence

Dependence on L.

TFT IGZO

S_{ID}/I_D^2 versus gate length at different $(V_{GS} - V_{th})$, with V_{DS} = 1 V, and f =12 Hz, for IGZO TFTs in 15-µm, 20-µm, 30-µm, and 50-µm gate-length devices.



Agrees with theory, Vg ↑ L ↑ noise ↓

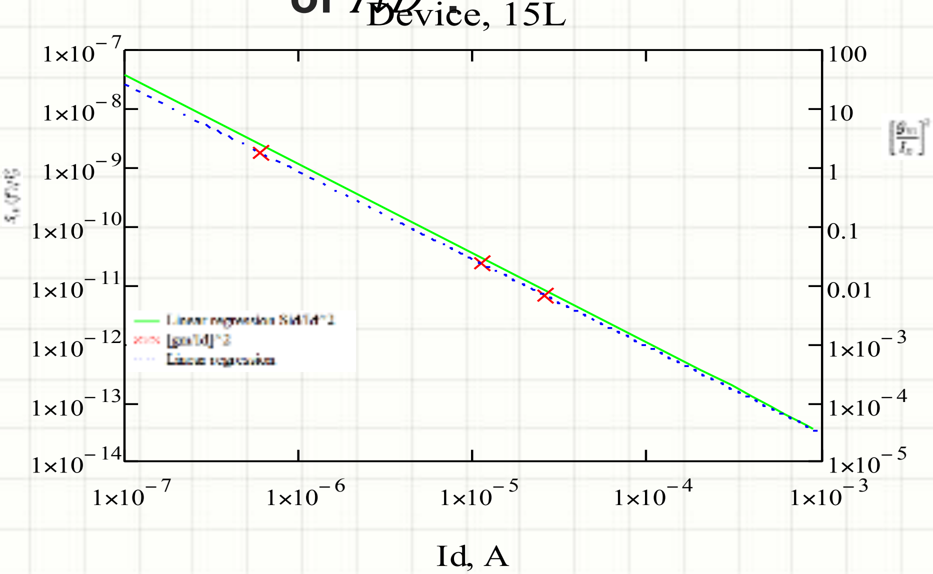
$$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f}\frac{1}{C_{ox}^2 W L}\frac{1}{(V_{GS}-V_{th})^2}$$

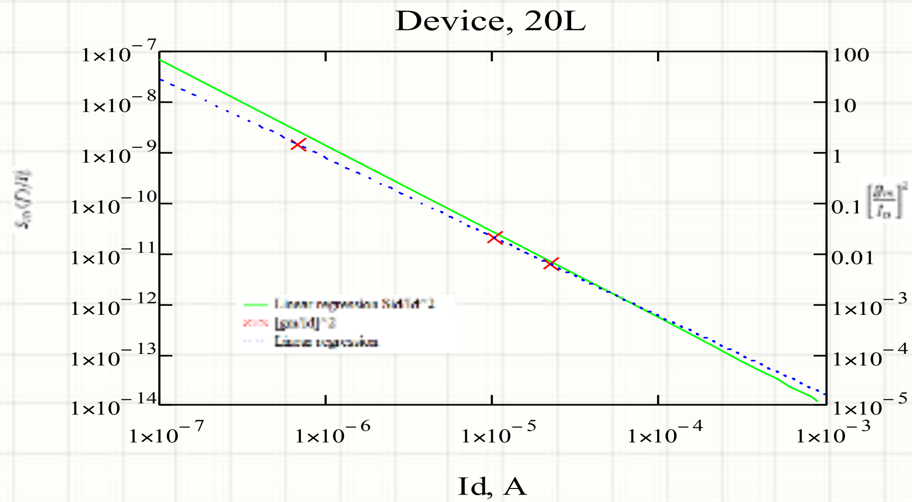
Noise produced in channel region.

$$\frac{S_{ID}}{I_D^2} = \frac{q}{C_{ox} W L}\frac{\alpha_H}{f}\frac{1}{(V_{GS}-V_{th})}$$

RESULTS, Origin of noise

$S_{ID}(f)/I_D^2$ and $[gm/I_D]^2$ are parallel as a function of I_D .

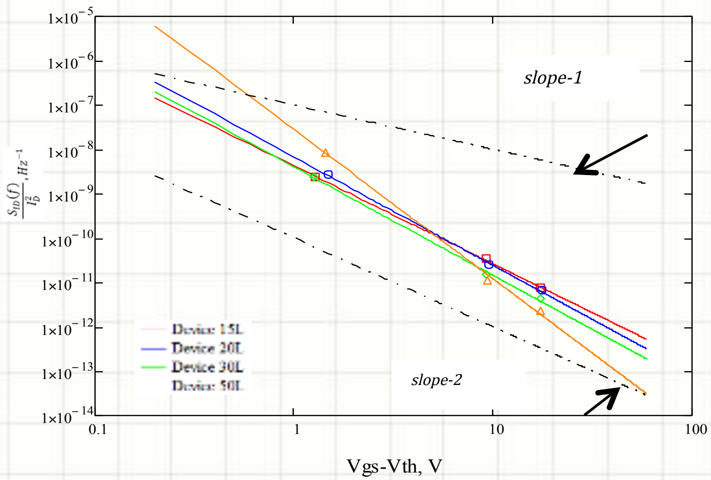




This means that the main origin of noise is the fluctuation of the number of carriers

RESULTS, Origin of Noise

Log–log plot of the normalized noise drain current spectral density ($S_{ID}(f)/I_D^2$) versus gate voltage overdrive ($V_{GS} - V_{th}$)



Slope closer to -2.

This means that the main origin of noise is the fluctuation of the number of carriers

$$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f}\frac{1}{C_{ox}^2 WL}\frac{1}{(V_{GS}-V_{th})^2}$$

CONCLUSIONS

Channel length and bias dependences:

- **L increases, $S_{ID}(f)/I_D^2$ decreases**
- **VG increases, $S_{ID}(f)/I_D^2$ decreases**
- **~ $(1/f^{\gamma})$, γ = 1**

1/f Noise:

- **TFT IGZO,**

  Fluctuation of the number of carriers, ΔN.

  Log ($S_{ID}(f)/I_D^2$)-log($V_{GS} - V_{th}$)

  Slope ≈ -2.

  Caused by the mechanism of trapping and reléase at the interface of the insulating layer.

8th SINANO Modeling Summer School

- Tarragona (Spain), September 25-28 2018
- 23 lectures targeting different techniques of device modeling, characterization and application to circuits.
- Among the technologies targeted: SOI CMOS, Multi-Gate MOSFETs, GaN HEMTs, Organic TFTs, IGZO TFTs, Organic Photovoltaics, Quantum Computing devices, Synaptic devices,…
- Reduced registration fee until September 12. Cheap fee especially for students.

- **fundacio.urv.cat/congresos/sinano-modelling-summer-school**

- Looking forward to seeing you in Tarragona!

DOMINO RISE PROJECT

- Goal: compact models for Amorphous Oxide Semiconductor and Organic TFTs integrated in design tools
- 4 universities, 2 research centers (foundries), 3 EDA companies
- Coordinator: URV
- Dec 1 2014-Nov 30 2018

THANKS FOR YOUR ATTENTION

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