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Leading Innovation

Compact Model Challenges of 65nm RF-CMOS technology

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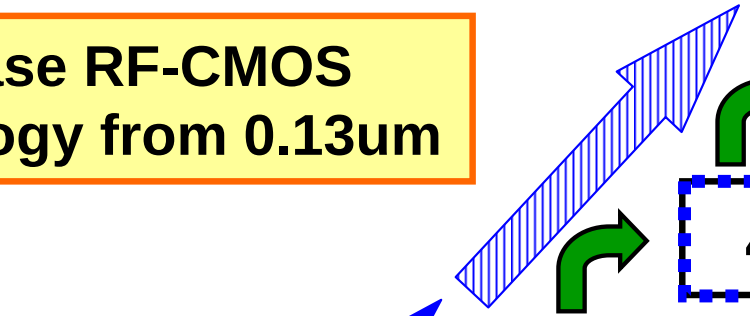
CMOS Technology Innovation

Release RF-CMOS Technology from 0.13um

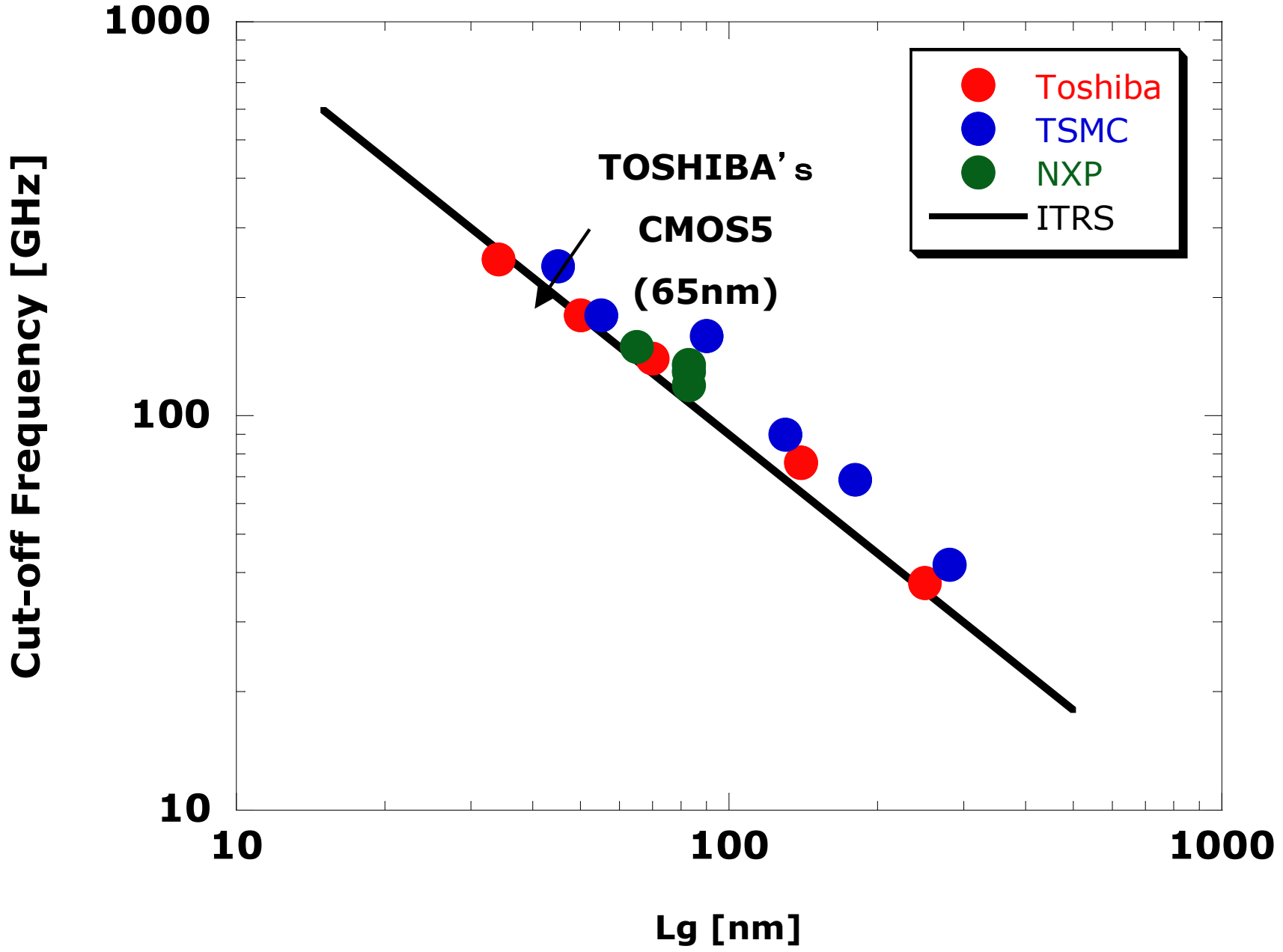


32nm	CMOS7 ?	*Metal Gate High-k*	
40nm	CMOS6 ?	*Strained-Si, High-k Low-k III*	
65nm	CMOS5 BSIM4・PSP・EKV*	*Stress control Low-k II*	CMOS5 08/Q2
90nm	CMOS4 BSIM4・EKV*	*Low k*	CMOS4 07/Q2
0.13um	CMOS3 BSIM3・EKV*	*Cu Interconnect*	CMOS3 06/Q2
0.18um	CMOS2 BSIM3・EKV	*Logic Based eDRAM*	
0.25um	CMOS1 BSIM3	*STI Dual Gate / Ti Salicide*	
0.35um	1995		

EKV available for internal use only

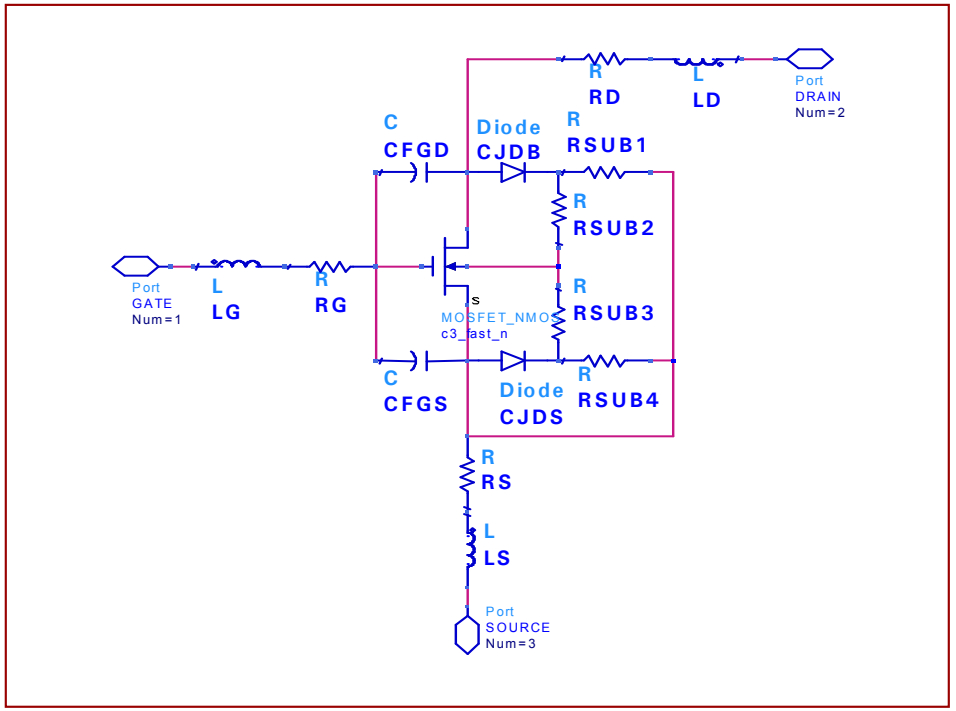
Toshiba's been a leader for many process generations

f_T Trend and Benchmarking



Agenda

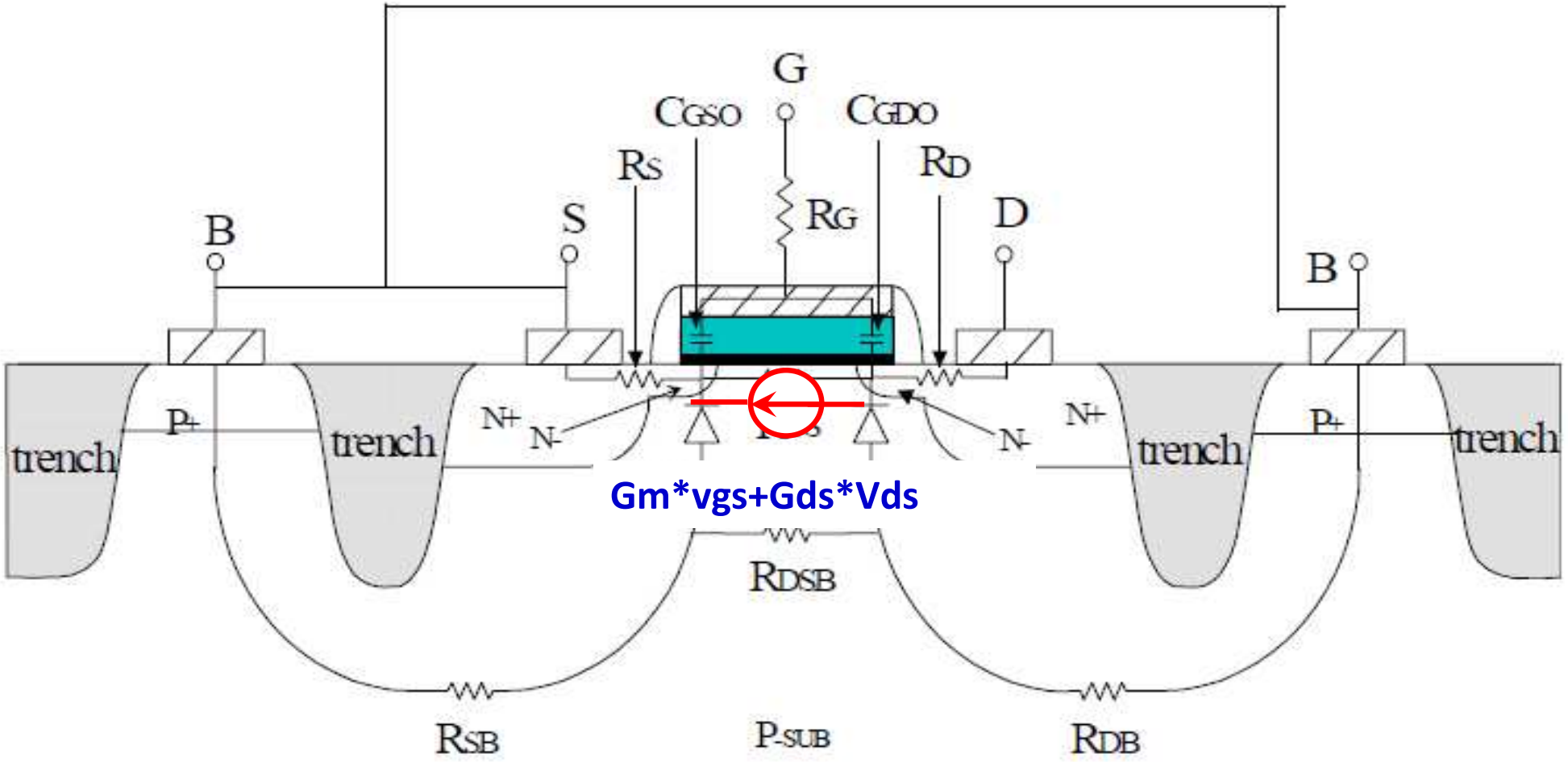
- **Challenges of RF scalable model creation of 65nm RF-CMOS technology**
  - Methodology of creation of RF-CMOS scalable model
  - Observation of “RF-scaling law”
  - Extensional validation issues.
    - RF Switch
    - High-linear circuits



What is needed for RF-CMOS compact model ?

- **Scalable and compact**
  - For portability, parasitic elements should be scalable function of
    - Lg (Gate Length)
    - Wf (Finger Length)
    - NF (Finger Numbers)
    - (SA,SB,SD)
- **Accurate for all design purpose**
  - LNA (NQS effect, Thermal noise)
    - Linear: S-parameters > 100GHz
      - De-embedding: SOLT ? TRL ?
  - VCO and Mixer (Harmonic distortion, Flicker noise)
    - Flicker noise close to the carrier.
    - ACPR, EVM
  - Power amplifier
    - Self Heating
    - Load-pull

MOSFET : Extrinsic Parasitic elements

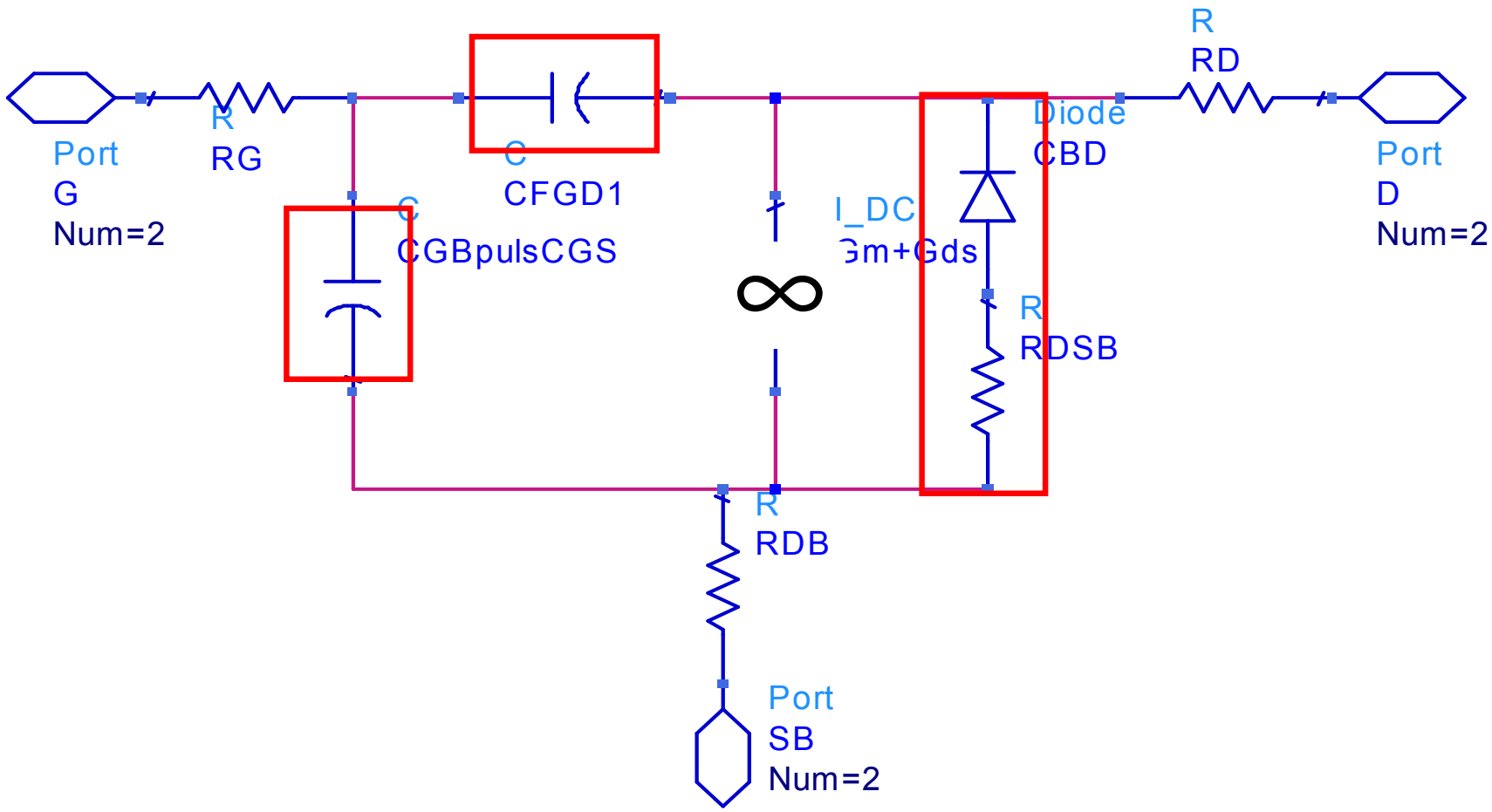


Yuhua Cheng et al.(2000b) MOSFET modeling for RF circuit design, Proceeding of the 2000 Third IEEE International Caracas Conference on Devices, Circuits and Systems, D23/1-D23/8

Simplified Equivalent Circuit when MOSFET=OFF

Source and Back-gate grounded

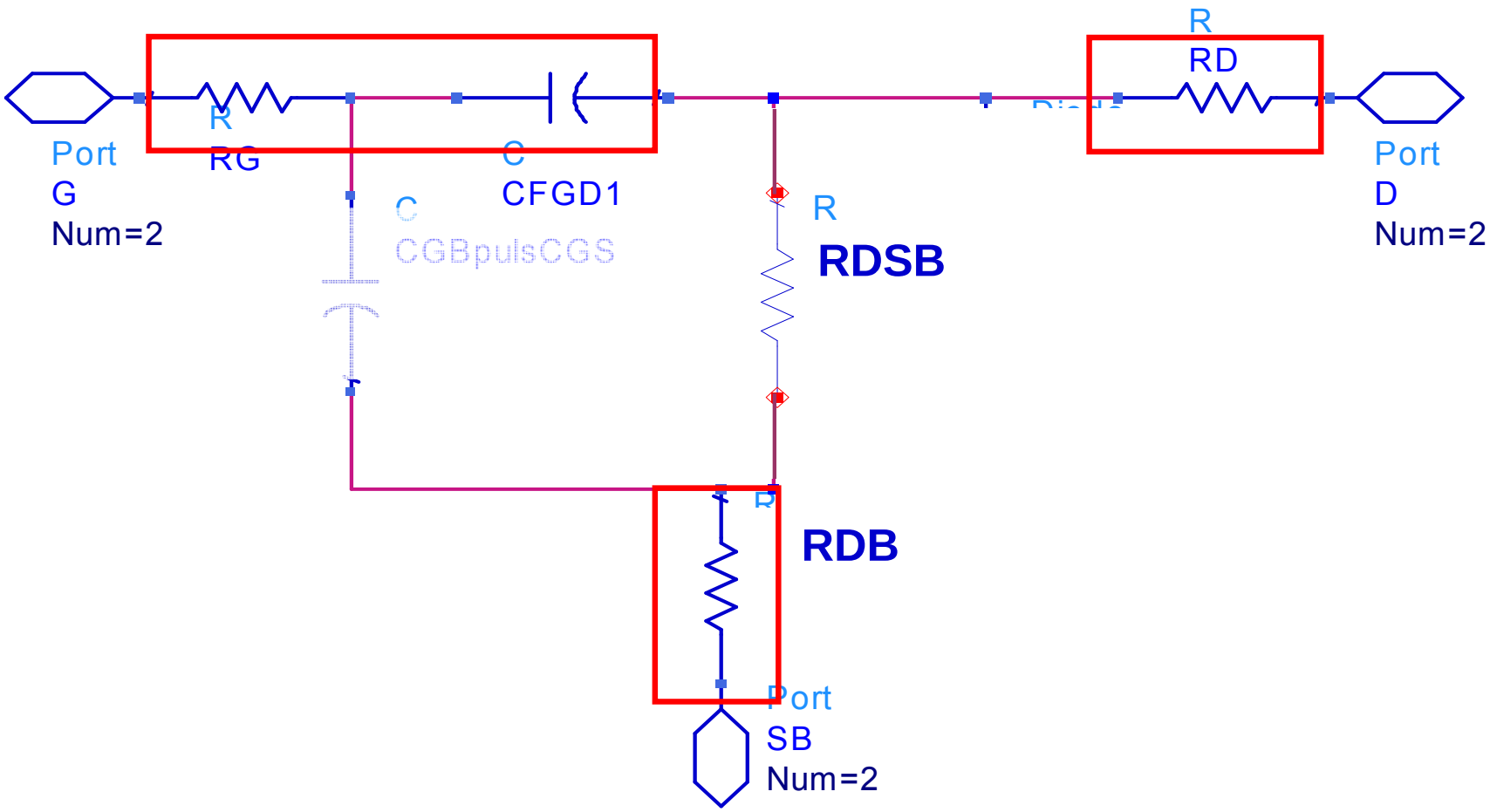
VG=VD=VS=VB=0



Equivalent Circuit when MOSFET=SI & Linear

Source and Back-gate grounded

VG=VDD, VD=low, VS=VB=0



Measure of components from y-parameters

Starting point the formula (12.7a~12.7d) : Christian C.Enz, Eric A. Vittoz , "Charge-based MOS Transistor Modeling" Wiley 2006.

$$Y_{11} \approx \omega^2 C_G^2 R_G + j\omega \mathrm{C_G}$$
$$Y_{12} \approx -\omega^2 R_G C_{GD} C_G - j\omega \mathrm{C_{GD}}$$
$$Y_{21} \approx G_m - \omega^2 R_G C_G (C_{GD} + C_m) - j\omega (C_{GD} + C_m)$$
$$Y_{22} \approx G_{DS} + \omega^2 R_G (C_G C_{BD} + C_G C_{GD} + C_{GD} C_m) + j\omega (C_{BD} + C_{GD})$$
$$C_G = G_{CS} + G_{CD} + G_{CB}$$

SI and linear region

$$R_G = \frac{\mathrm{Re}(Y_{11})}{\mathrm{Im}(Y_{11})^2}$$
$$R_D(R_S) = \mathrm{Re}(\mathrm{Z}_{22})$$
$$R_{DSB} = \mathrm{Re}\left(\frac{1}{Y_{22}}\right)$$

OFF region

$$C_{GD} = \mathrm{Im}(Y_{12})$$
$$C_{DB} = \mathrm{Im}(Y_{22} + Y_{12})$$
$$C_{GB} + C_{GS} \rightarrow \mathrm{Im}(Y_{11} + Y_{12})$$
$$R_{DB} \rightarrow \mathrm{Re}(Z_{12})$$

Q1

- **Does RG scaling follows classical ohmic-law ?**

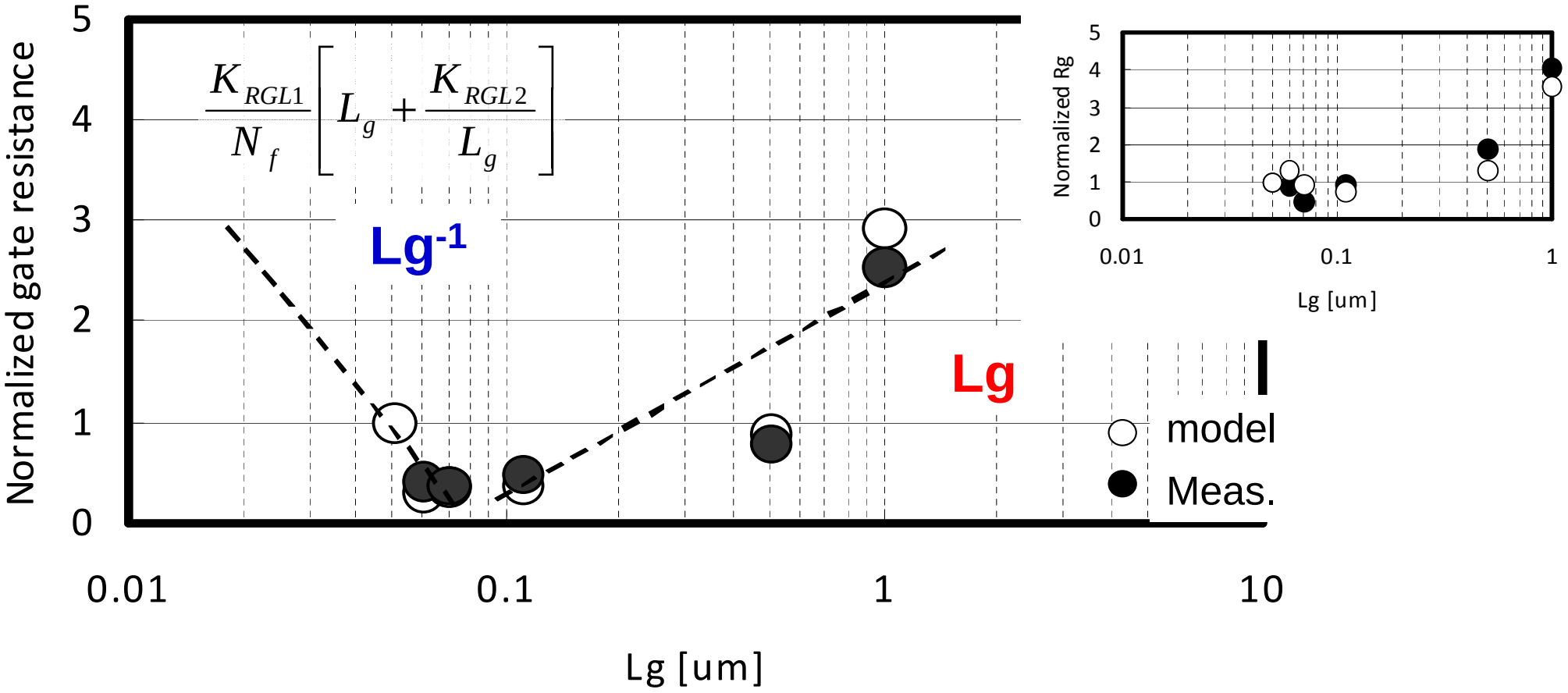
$$R_G = \rho_{rg} k \cdot \frac{Wf}{Lg \cdot Nf}$$

K : constant depending on the configuration of gate contact

NO : Gate resistance behaves complex behavior

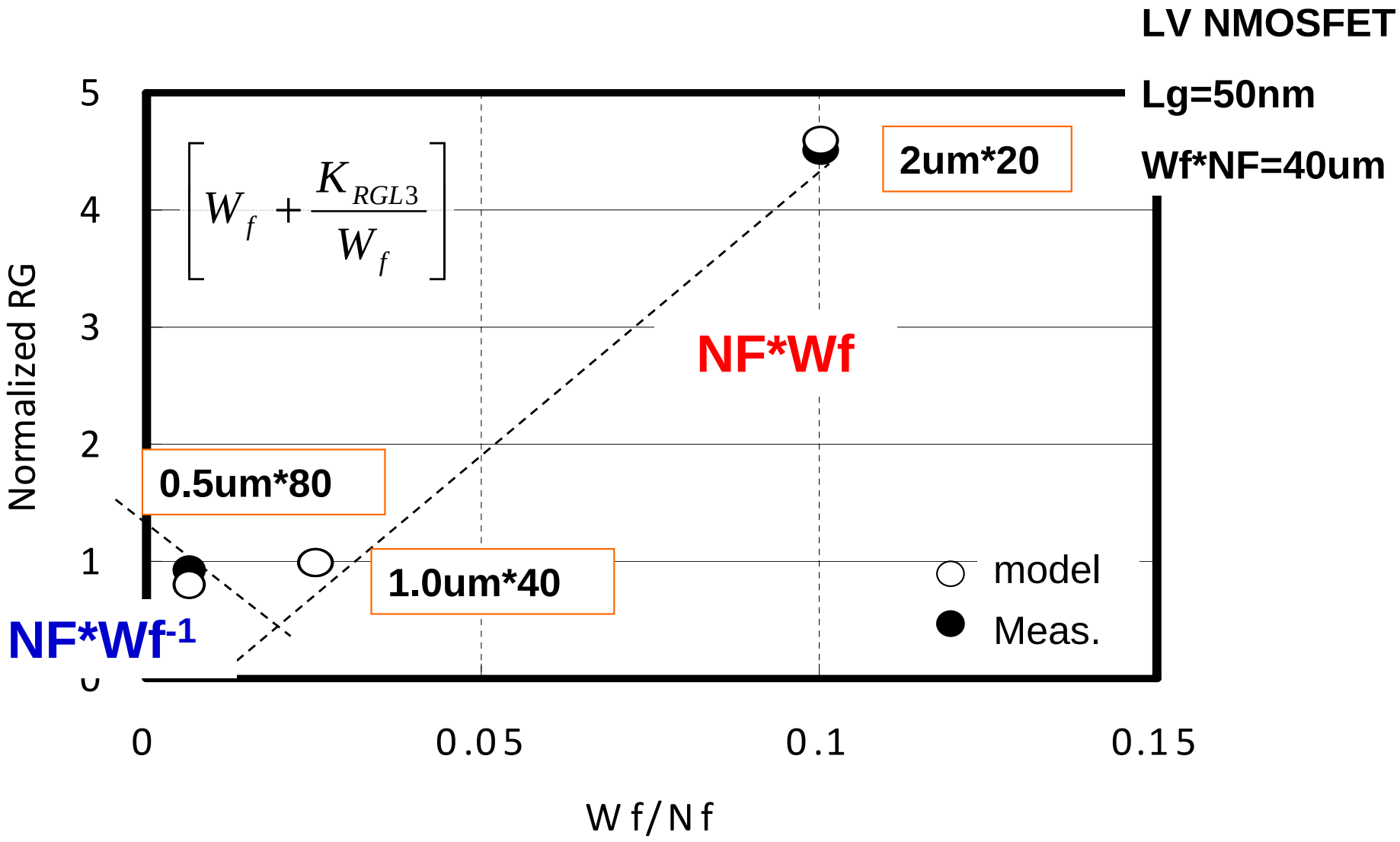
LV NMOSFET

Wf=1um, NF=40



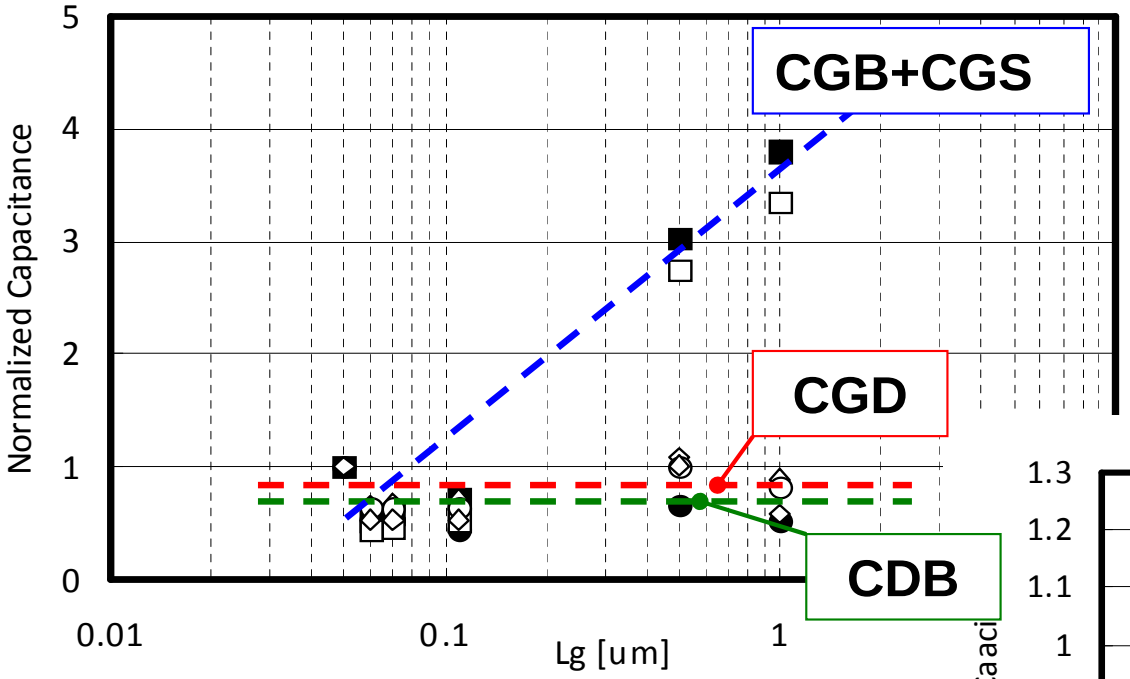
Scaling dependence of Rg on gate-length (Lg)

Scaling dependence of Rg on Wf/Nf

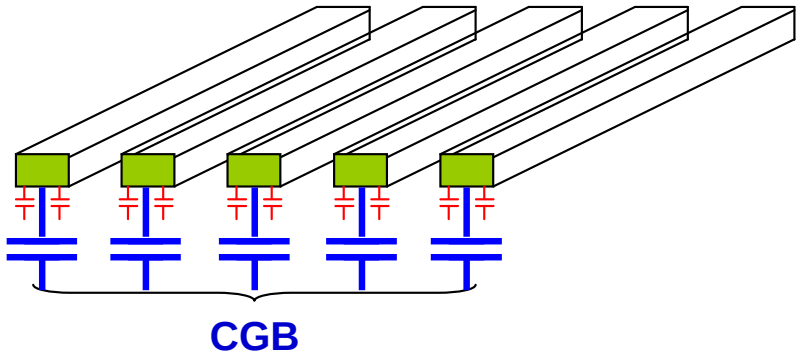


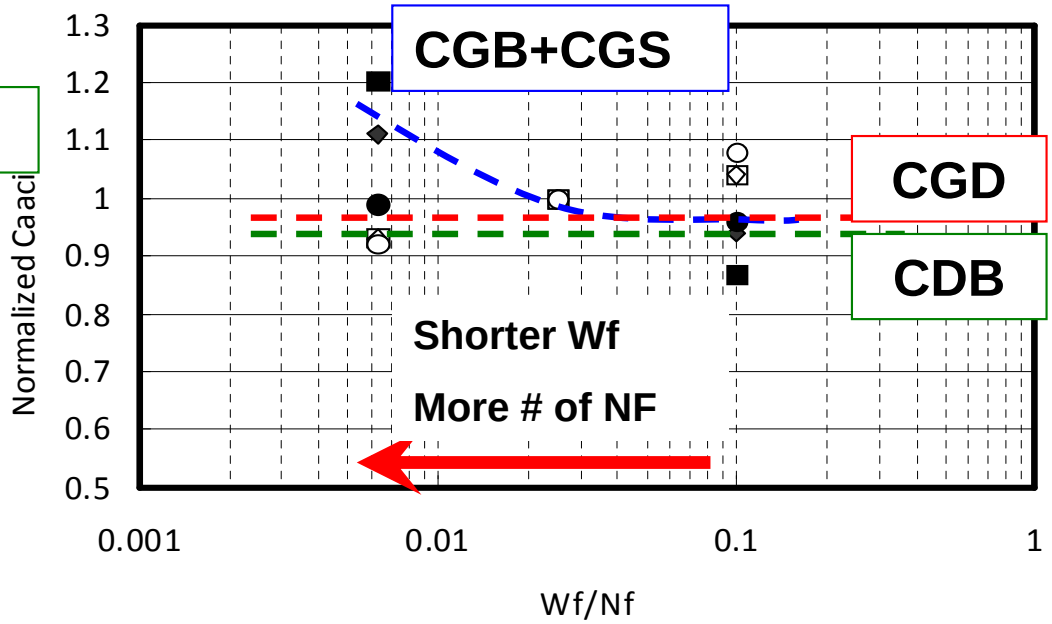
Q2 Does capacitance scaling has unique behaviour ?

- **NO : It is typical behavior**



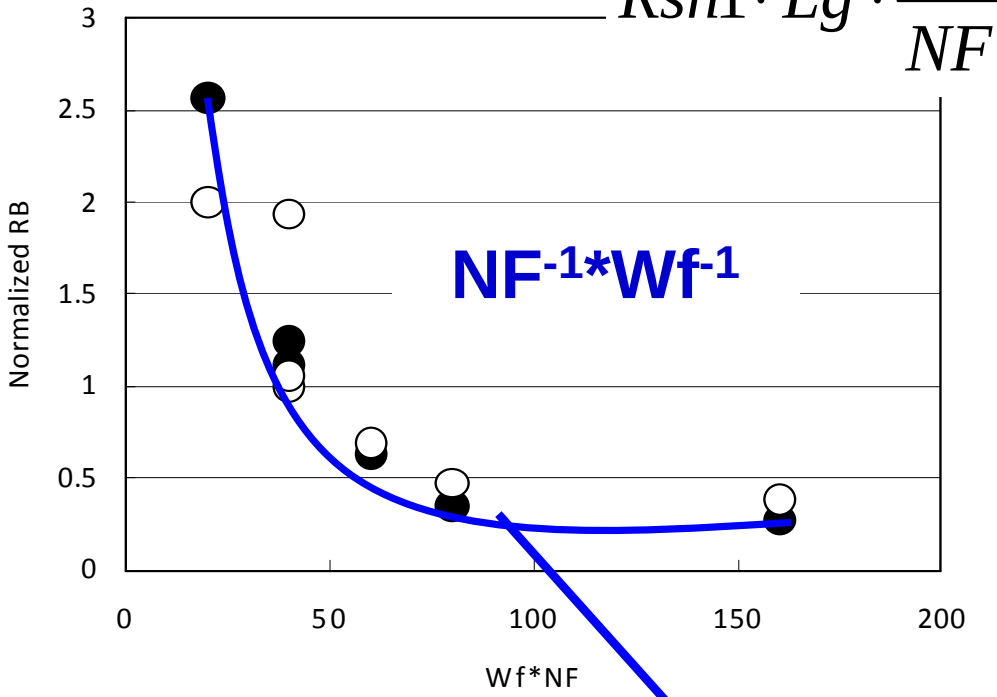
$$C_{GD} \rightarrow \mathrm{Im}(Y_{12})$$
$$C_{DB} \rightarrow \mathrm{Im}(Y_{22} + Y_{12})$$
$$C_{GB} + C_{GS} \rightarrow \mathrm{Im}(Y_{11} + Y_{12})$$

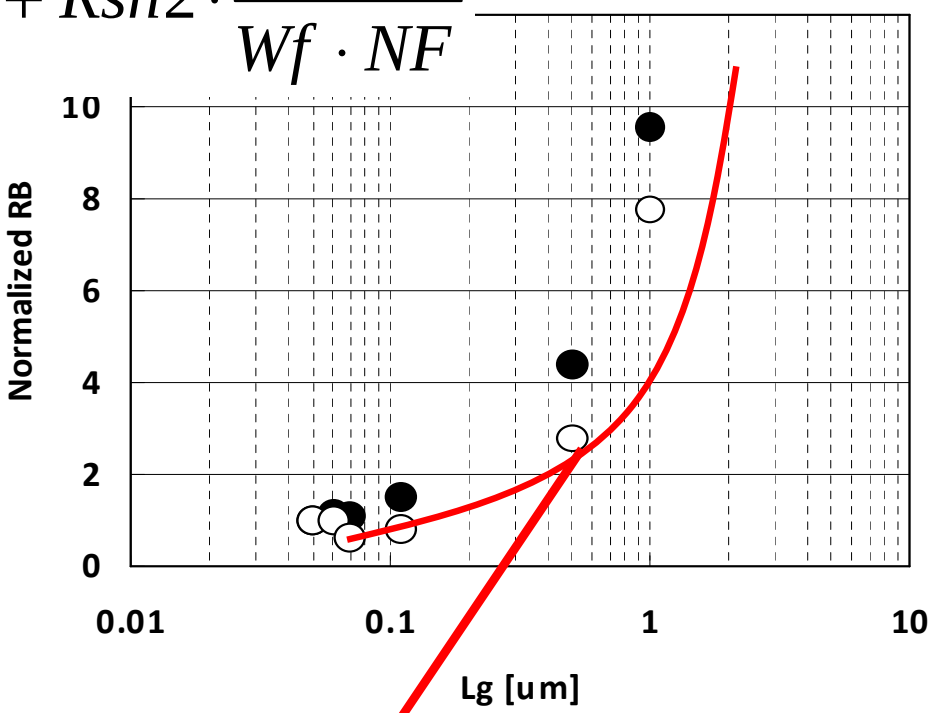


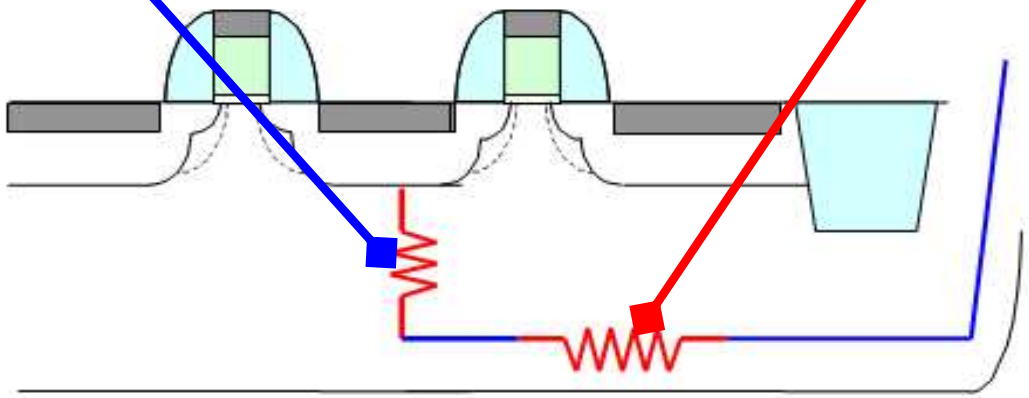


Observation of the RB scaling

$$Rsh1 \cdot Lg \cdot \frac{Wf}{NF} + Rsh2 \cdot \frac{1}{Wf \cdot NF}$$





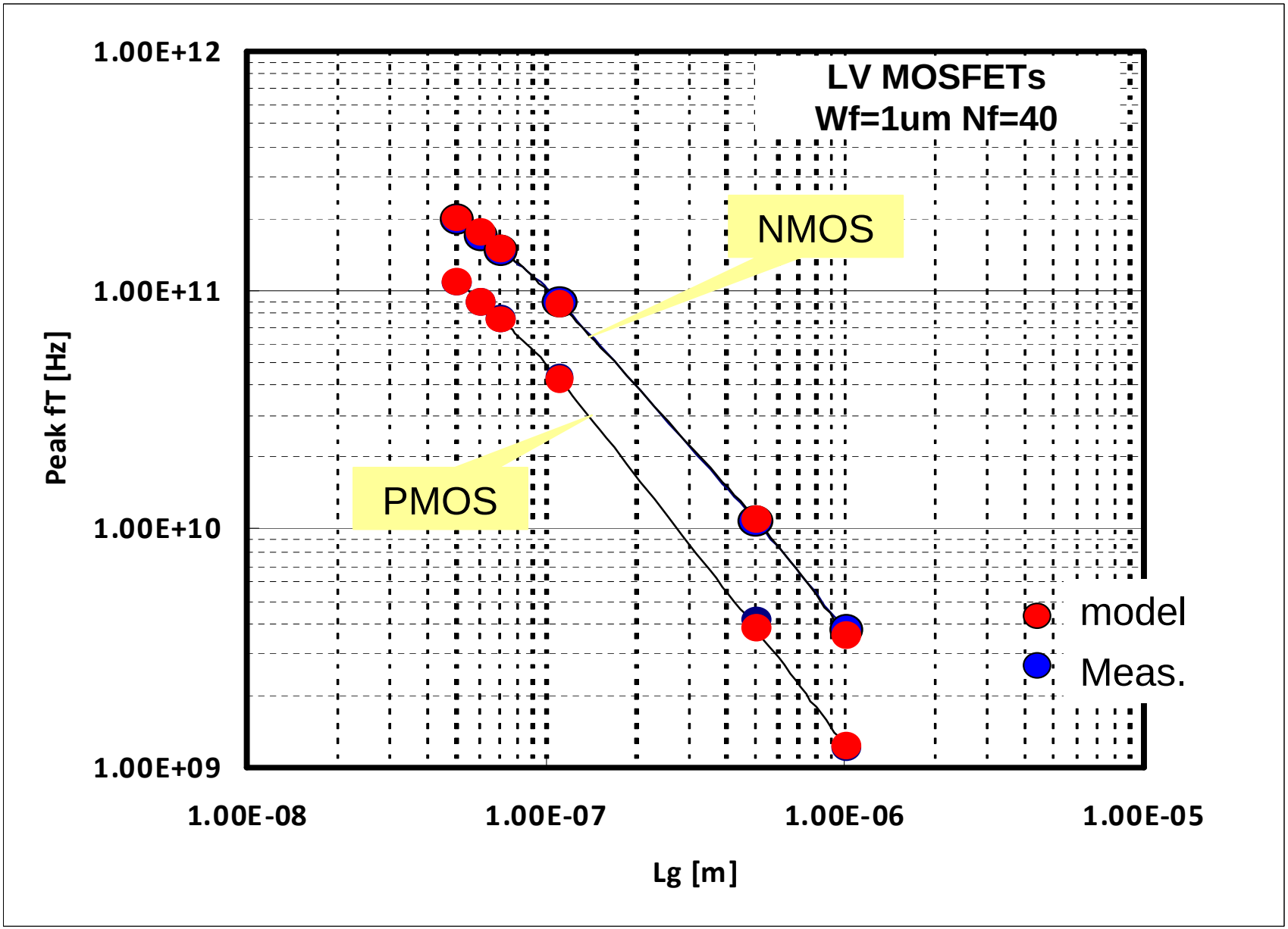


RF-CMOS modeling summary

Component name	Item name	Geometric dependency
NQS Gate resistance	RG	$\frac{K_{RGL\ 1}}{N_f}\left[L_g + \frac{K_{RGL\ 2}}{L_g}\right]\left[W_f + \frac{K_{RGL\ 3}}{W_f}\right]$
G-B capacitance	CGB	$CGB = K_{CGB} \cdot Lg \cdot Nf$
G-D,G-S overlap capacitance	CFGD CFGS	$K_{RCL} W_f N_f$
Substrate resistance	RSUB1 RSUB2 RSUB3 RSUB4	$Rsh1 \cdot Lg \cdot \frac{Wf}{NF} + Rsh2 \cdot \frac{1}{Wf \cdot NF}$

K_{CGB},K_{RGL1}, K_{RGL2}, K_{RGL3},K_{RCL},$K_{Rsh1,}$ K_{Rsh2} : Constants

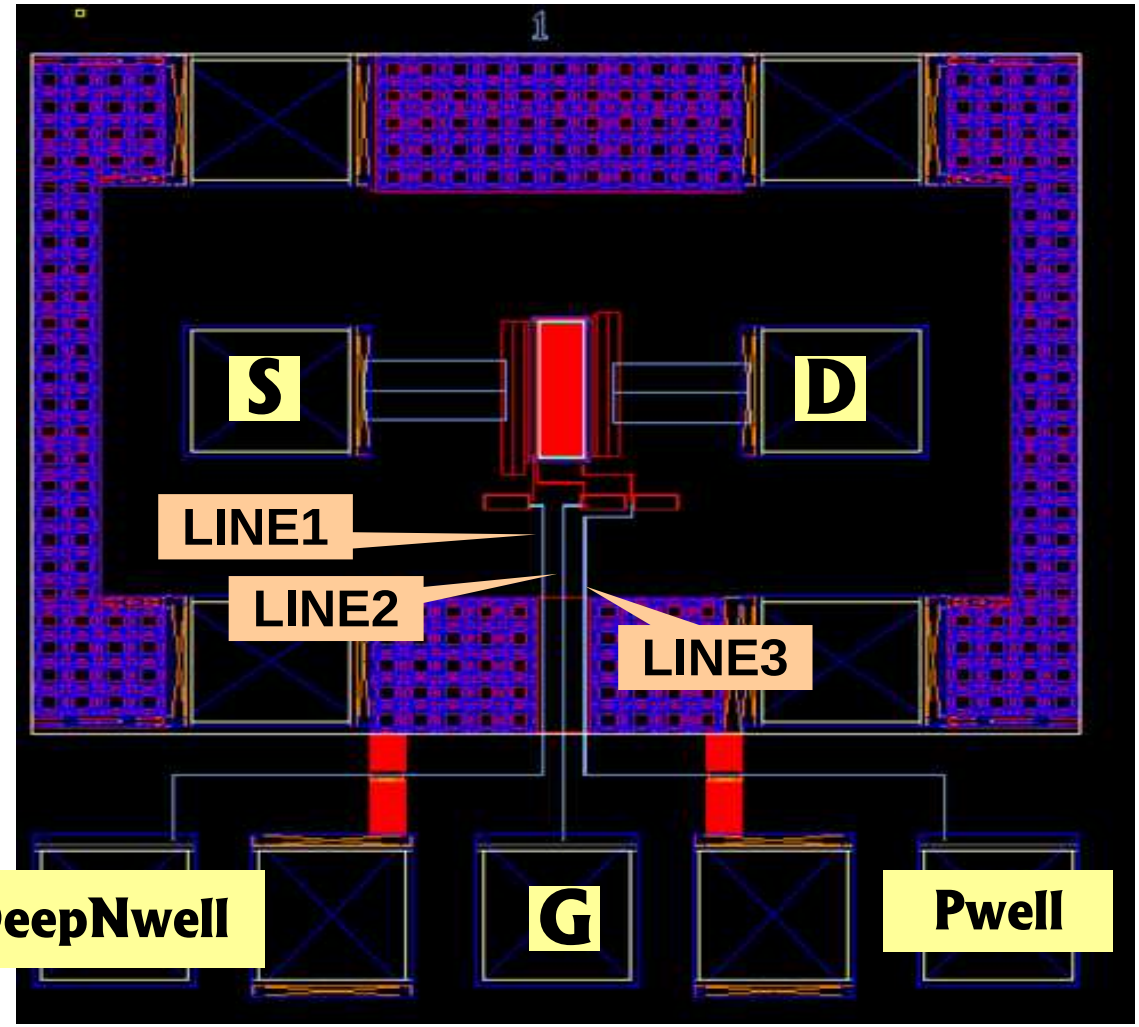
Verification of 65nm RF-CMOS via peak-fT



Improve

Model Verification

NMOSFET Lg=0.3um Wf=20um NF=100

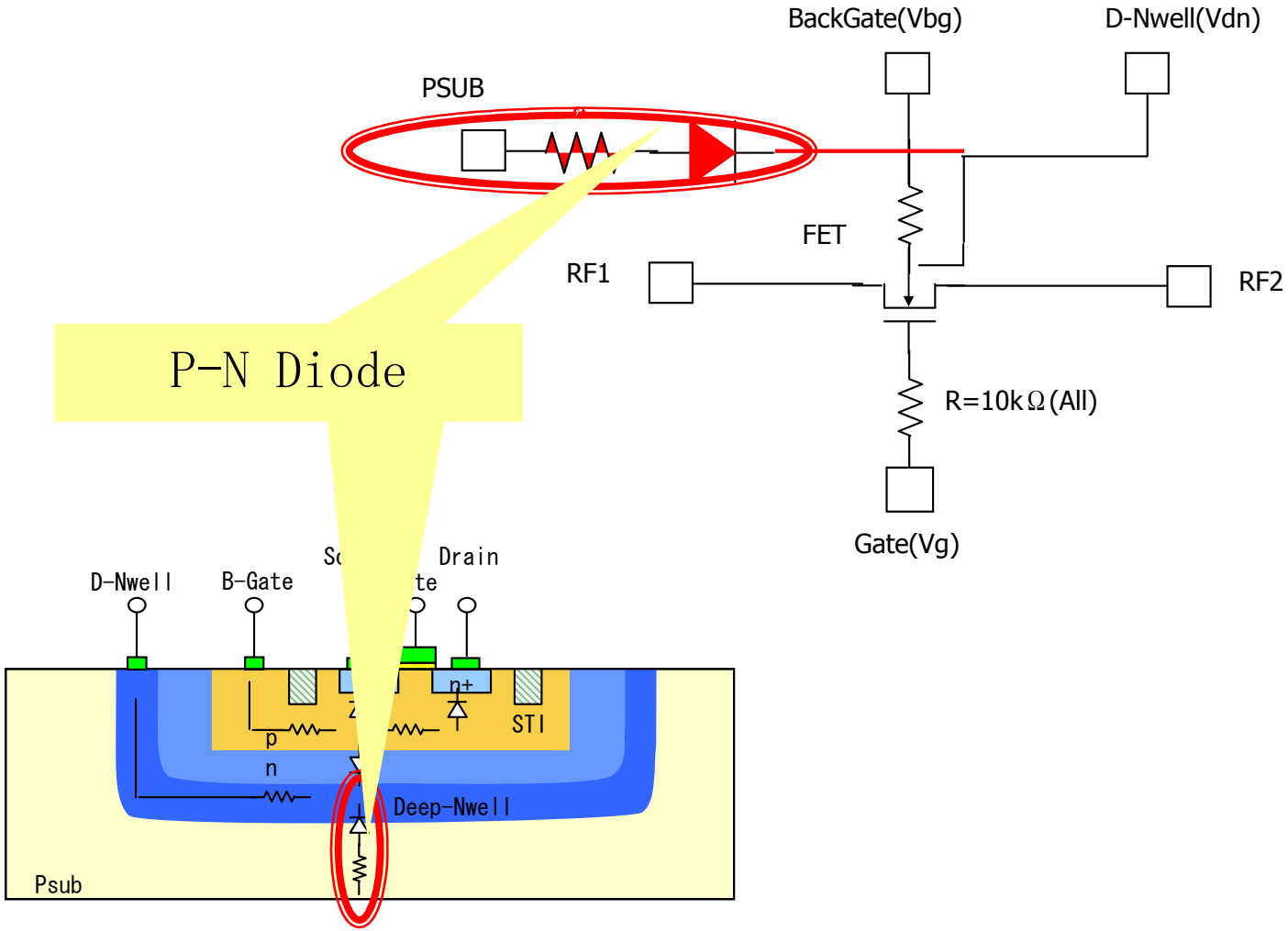


Line width all 0.3um

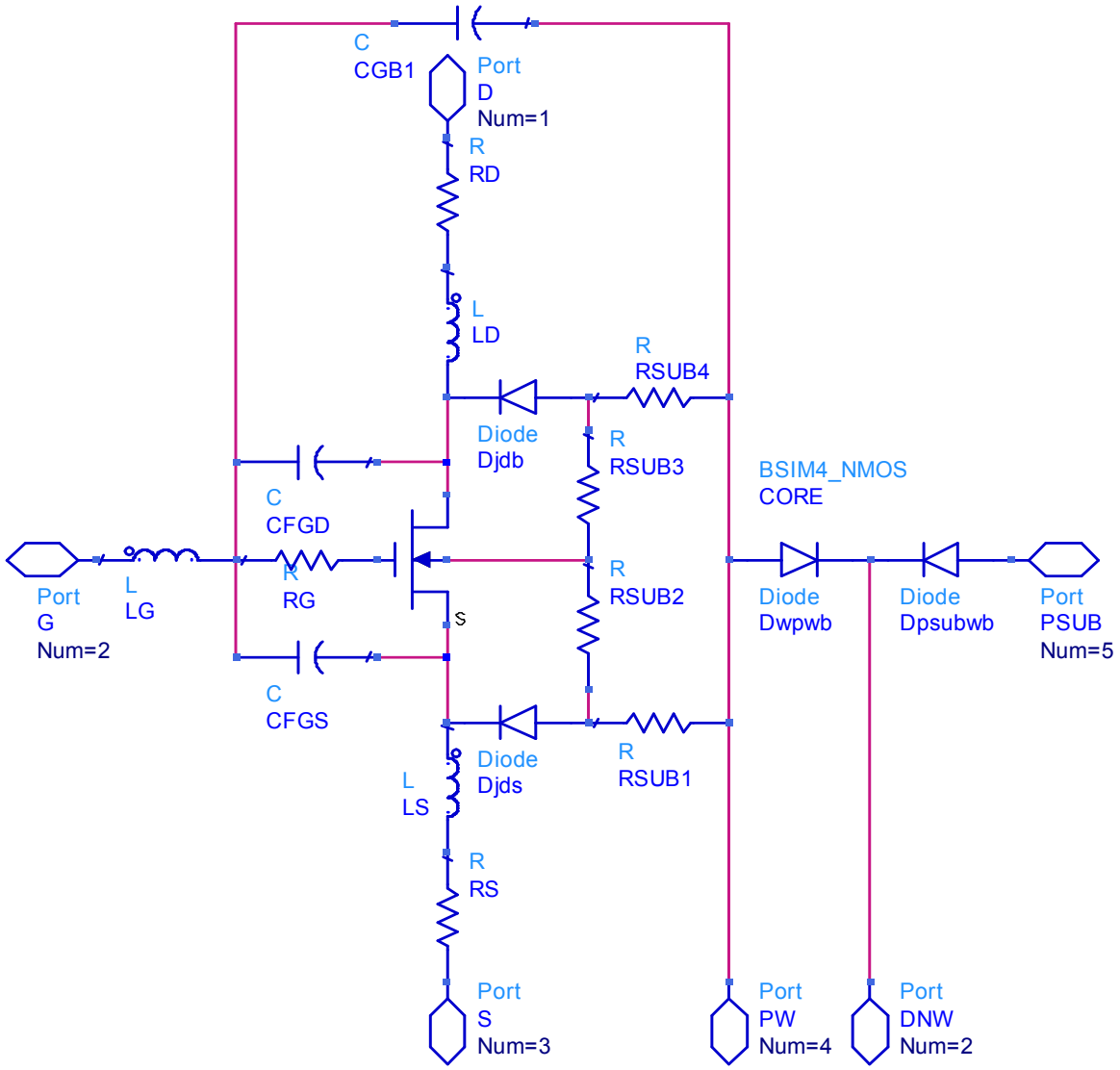
	PATH	Length of M1 [um]	Lngth of M6S [um]
LINE1	DeepNwell-RPOLY-PAD	25.04	355
LINE2	GATE-RPOLY-PAD	44.39	192.48
LINE3	Pwell-RPOLY-PAD	45.93	449.61

Define

MOSFET-Switch



5 Term MOS



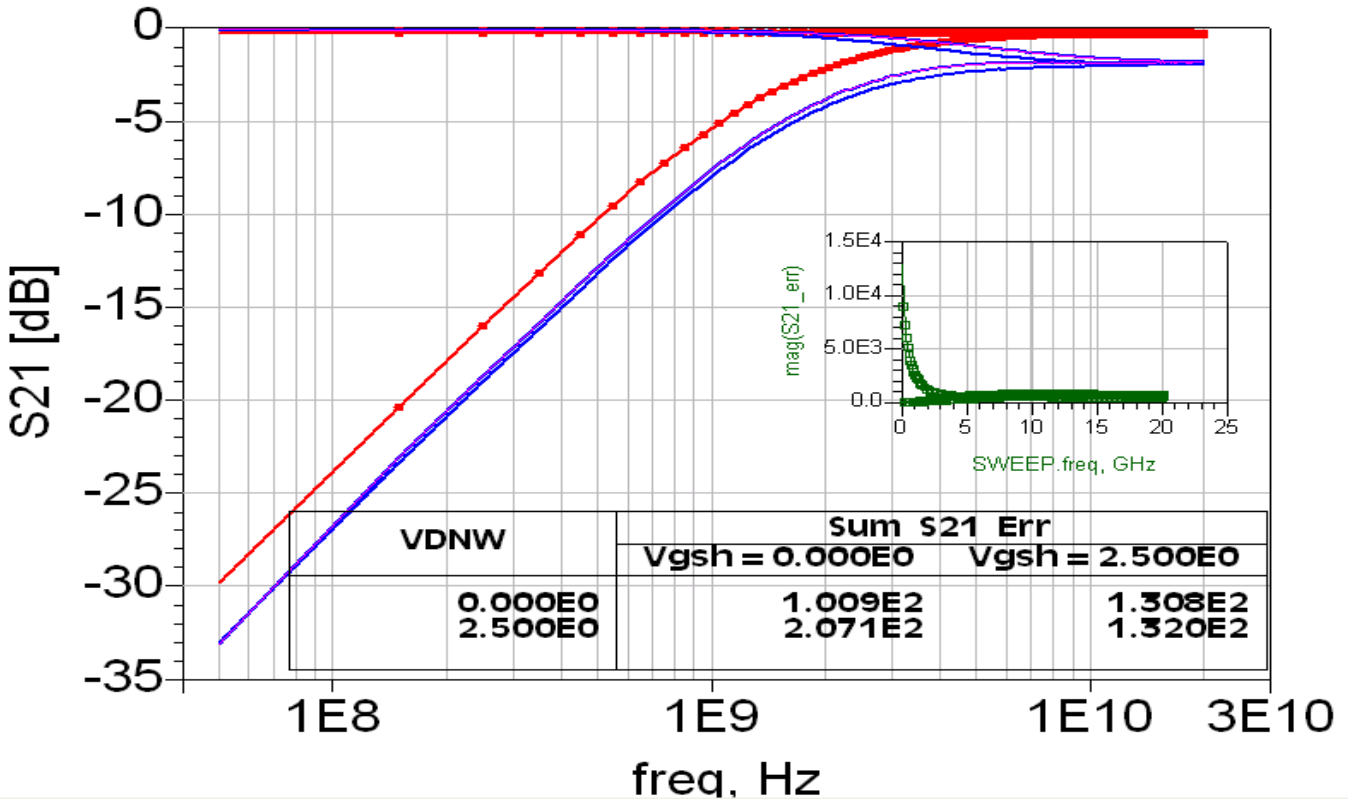
Simulation does not match

– NMOSFET Lg=0.3um Wf=20um NF=100

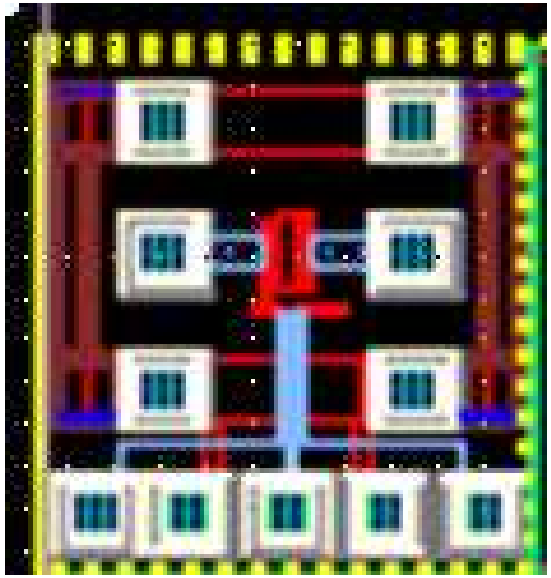
- **50MHz~20.05GHz (201 PTS)**
- **VG, V_DNW:0V,2.5V**
- **VD=VS=0V**

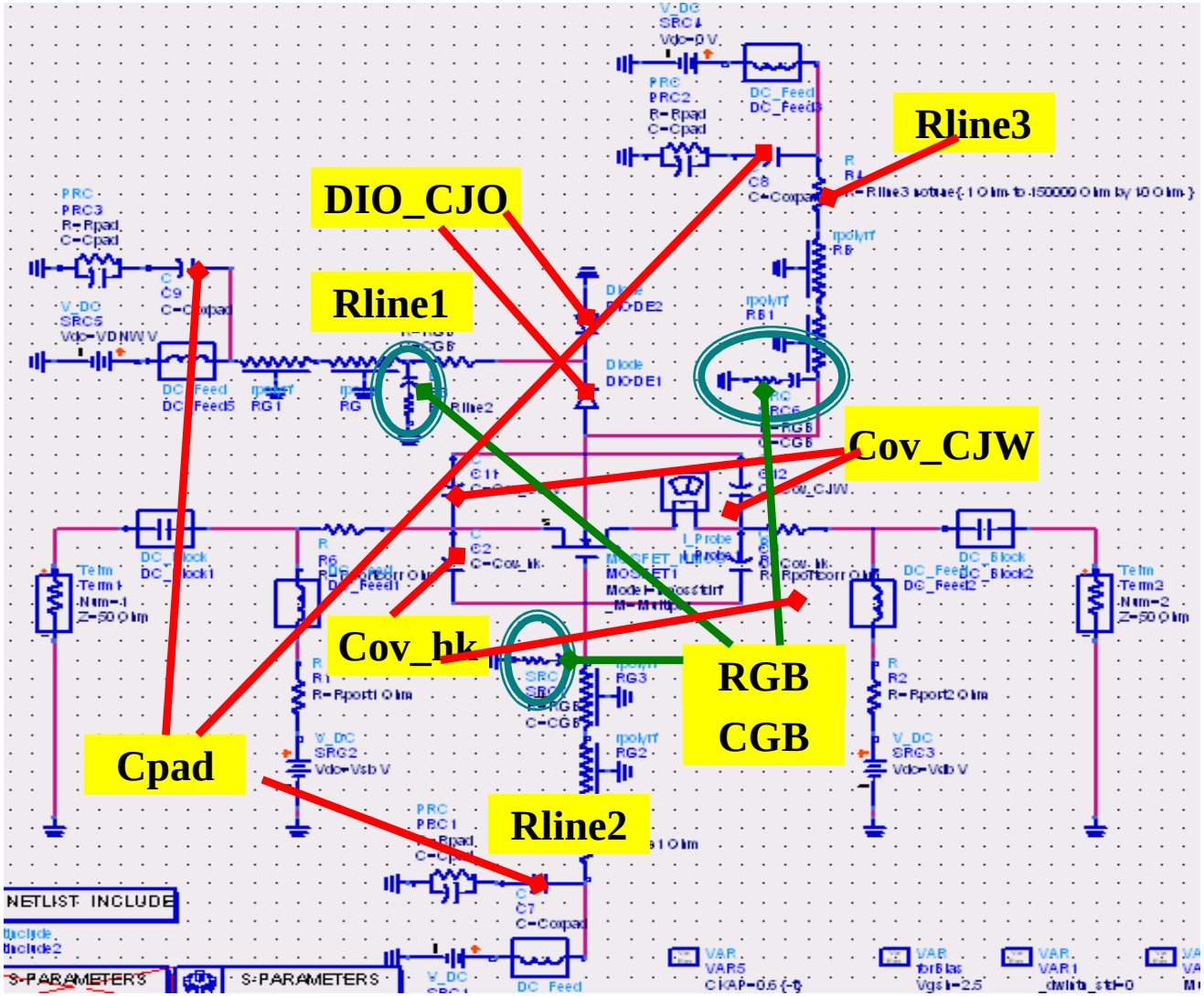
Blue:Meas

Red:Model



Hard Implemantation

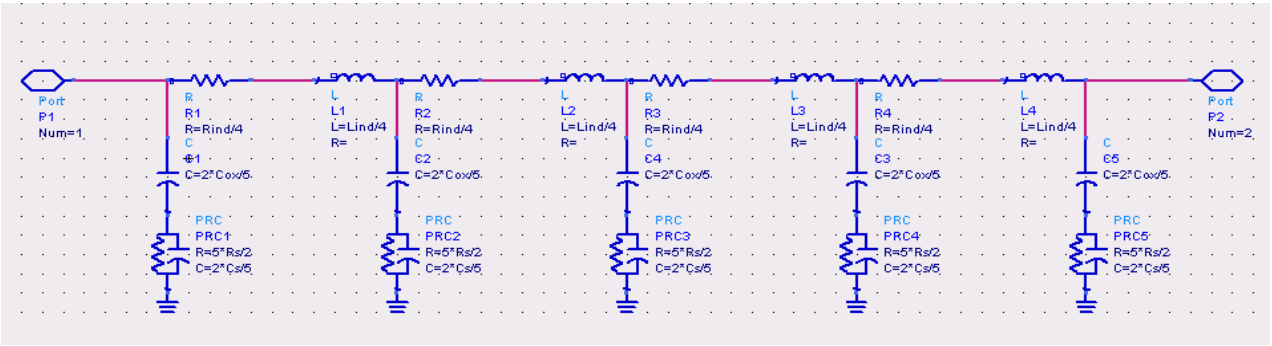




Improve

Transmission Line

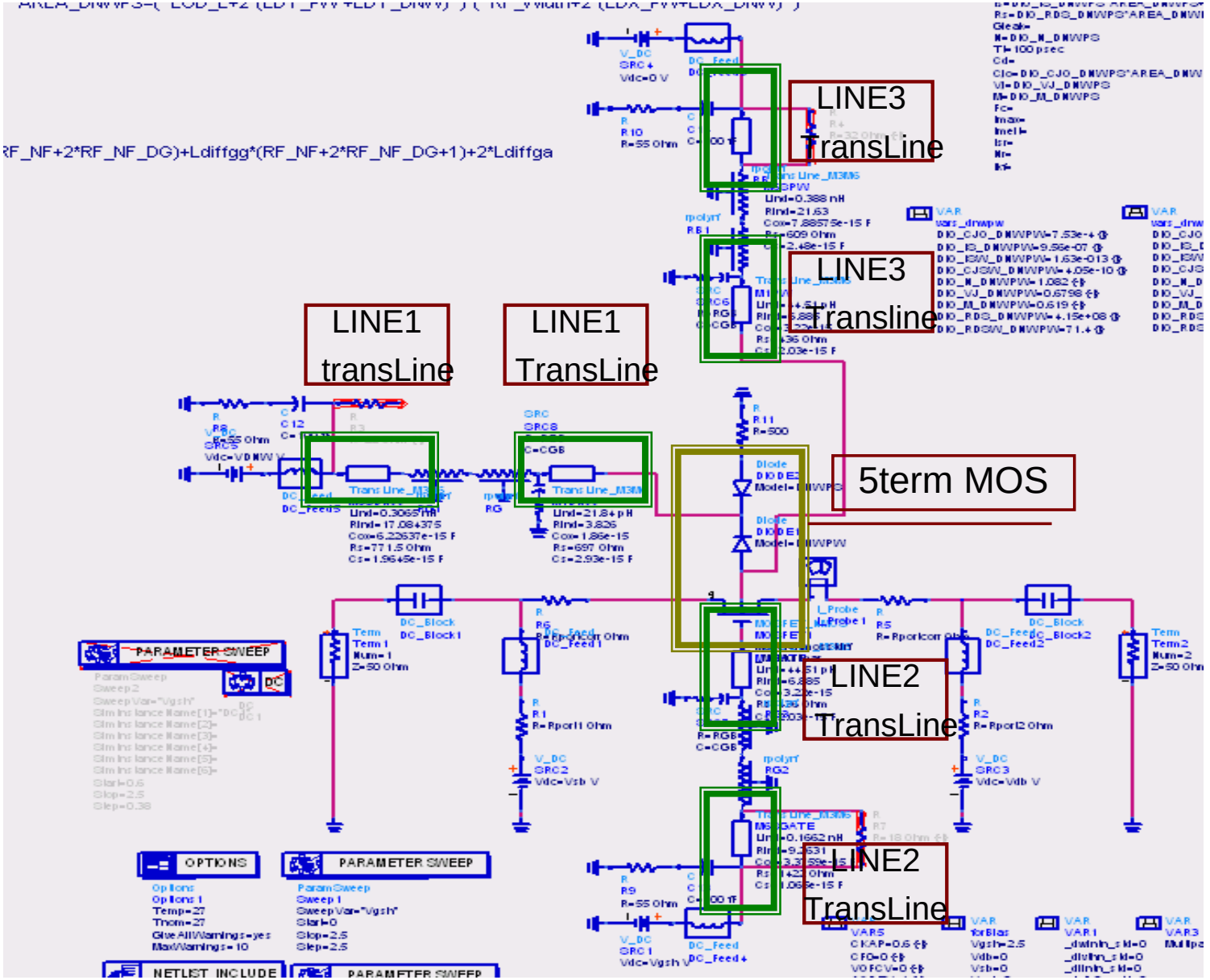
- Lind : Self inductaoce
- Rind:Series Resistance
- Cox : Cap between Metal and Si
- Rs : Loss of Si substrate
- Cs : Loss of Si substrate



	LINE1		LINE2		LINE3	
	M1	M6S	M1	M6S	M1	M6S
Lind [nH]	0.02	0.31	0.05	0.17	0.04	0.39
Rind [Ohm]	3.82	17.1	6.89	9.26	6.89	21.6
Cox [fF]	1.86	6.22	3.22	3.37	3.22	7.89
Rs [Ohm]	697	771.5	436	1422	436	609
Cs [fF]	2.93	1.97	2.03	1.07	2.03	2.48

Improve

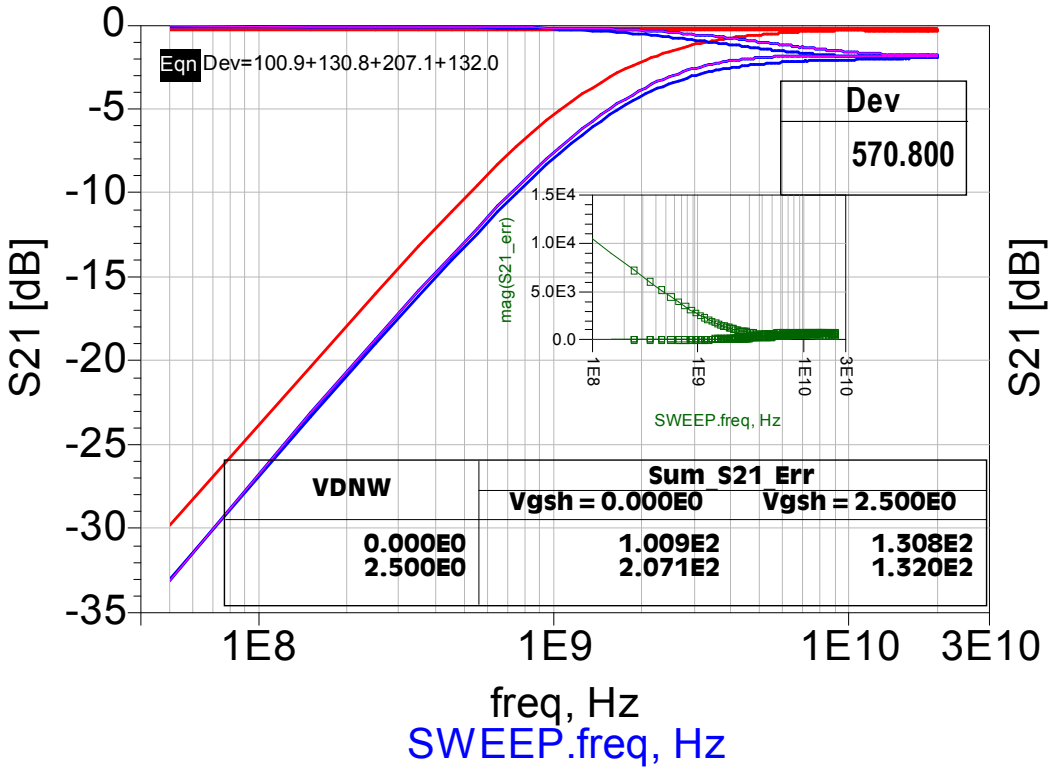
Completed schematic



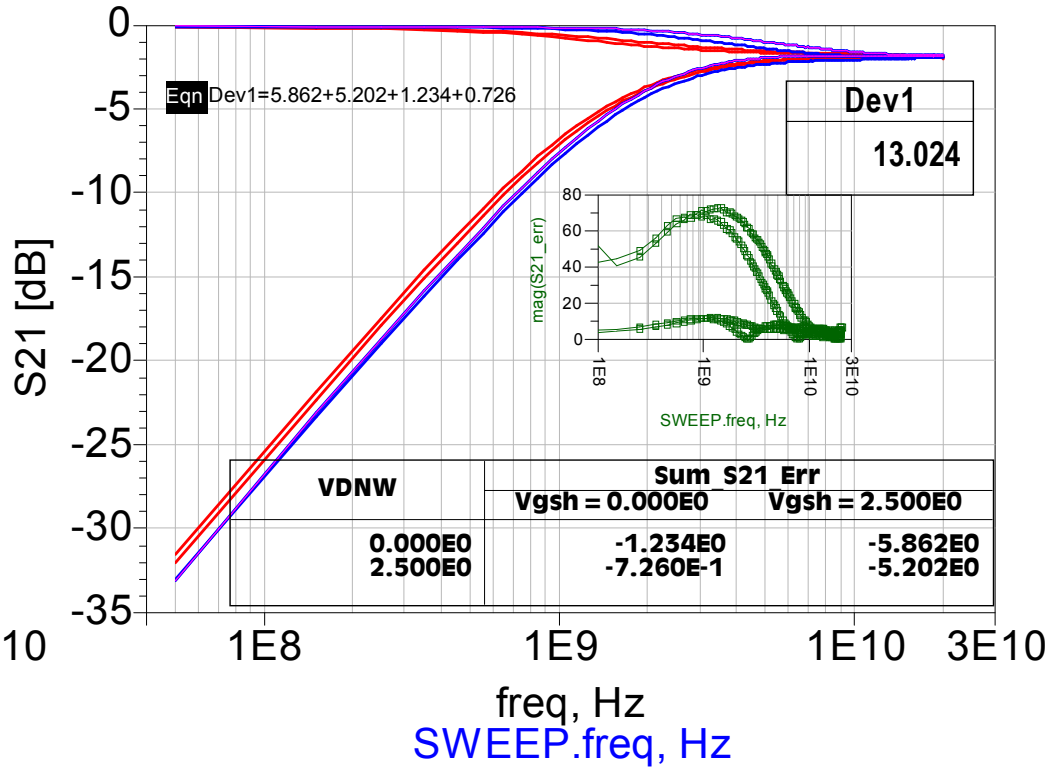
Improve

Comparison before and after

Before



after

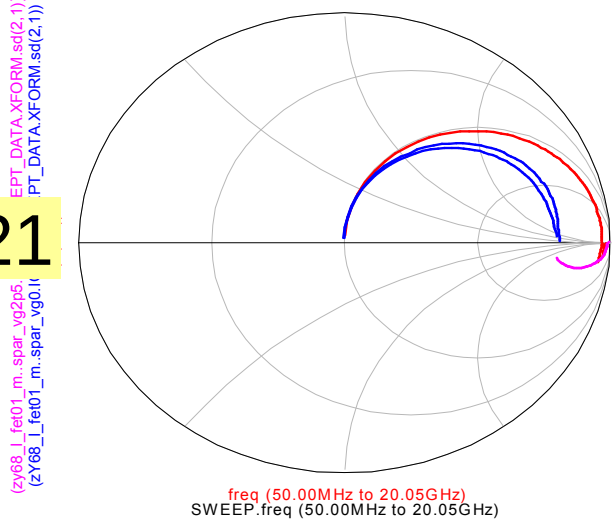


Improve

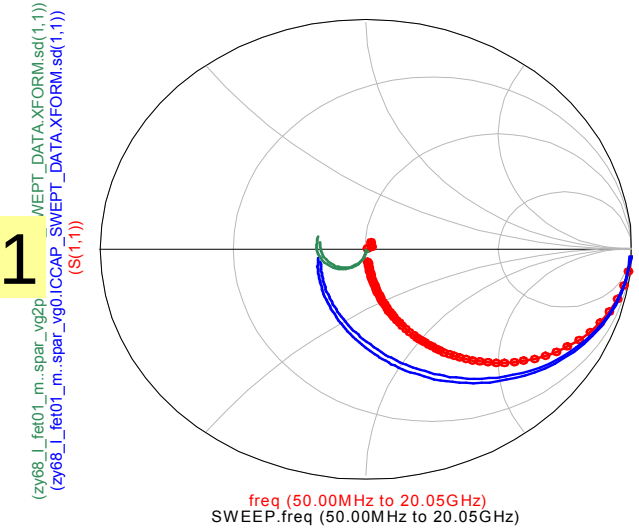
S-Parameter before and after

Before

S21

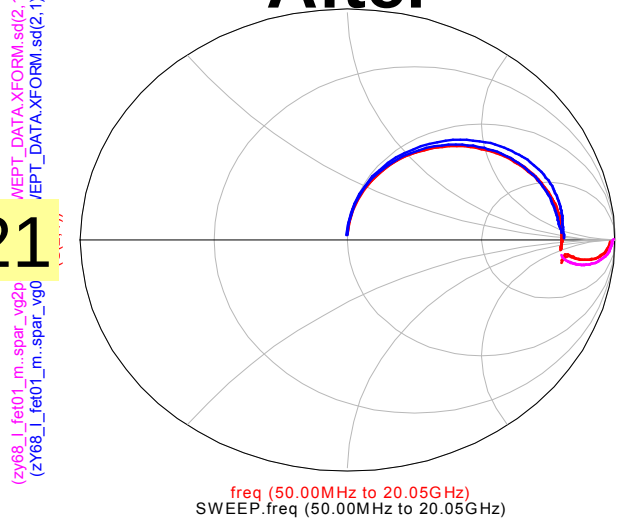


S11



After

S21



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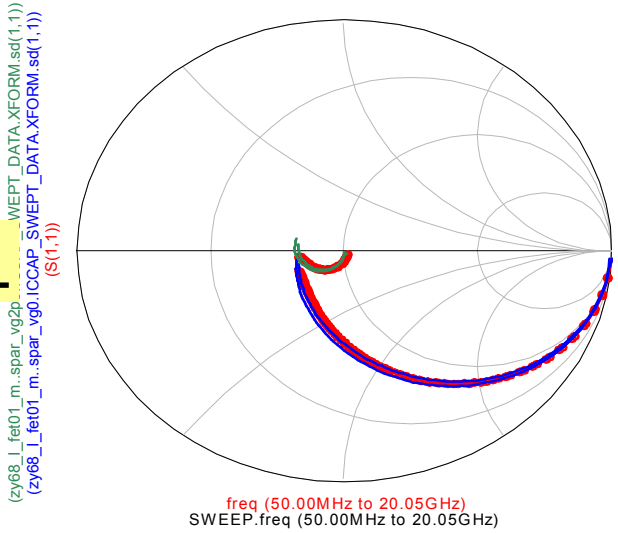

Summary

- **65nm-RFCMOS compact models' development**
  - Scaling approach based on COLD-measurement and SI & Linear measurement still works.
  - It is possible to get a simple guess by taking look at Y and Z parameters.
  - Substrate modeling is needed in case of RF switch which controls back-gate bias.
  - All possible modeling efforts by the aid of EM simulation is sure needed.

Thank you !