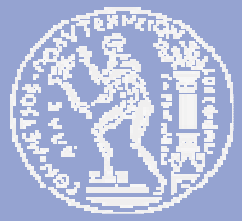


ESSCIRC/ESSDERC Workshops, MOS-AK Meeting
Edinburgh, September 15-19, 2008

Aspects of High-Frequency Modelling with EKV3

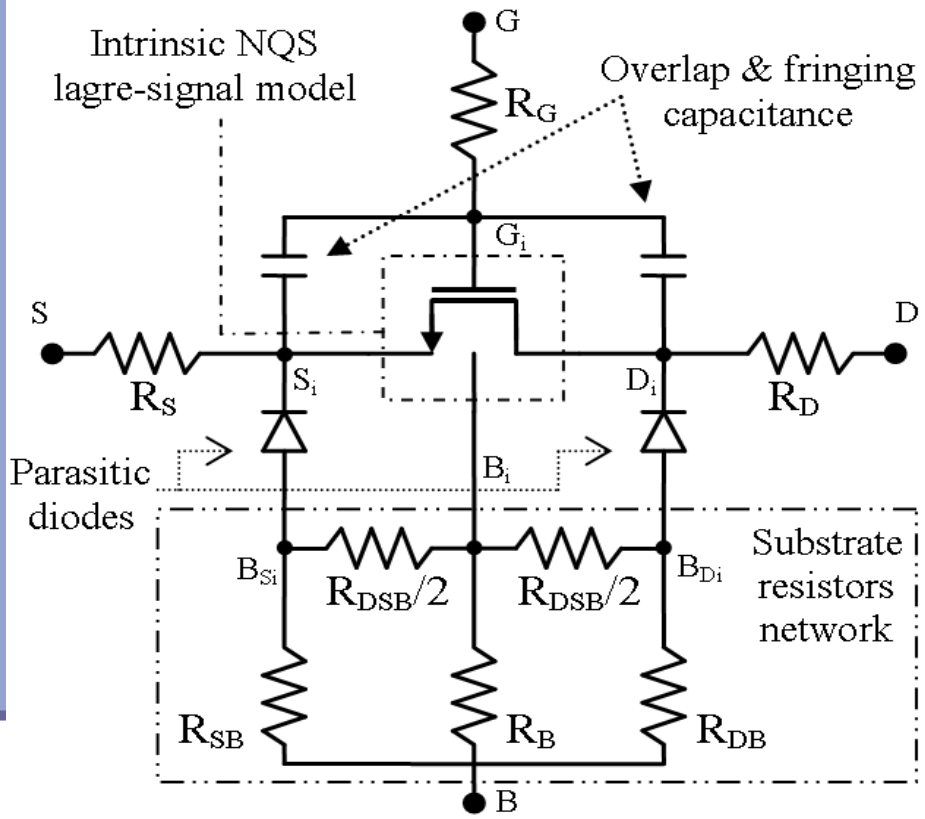
Matthias Bucher, Maria-Anna Chalkiadaki
Technical University of Crete (TUC), Chania, Greece

Antonios Bazigos
National Technical University of Athens (NTUA), Athens, Greece

Outline

- Introduction
- Case I: 180 nm CMOS
- Case II: 110 nm CMOS
- Case III: 90 nm CMOS
- Conclusions

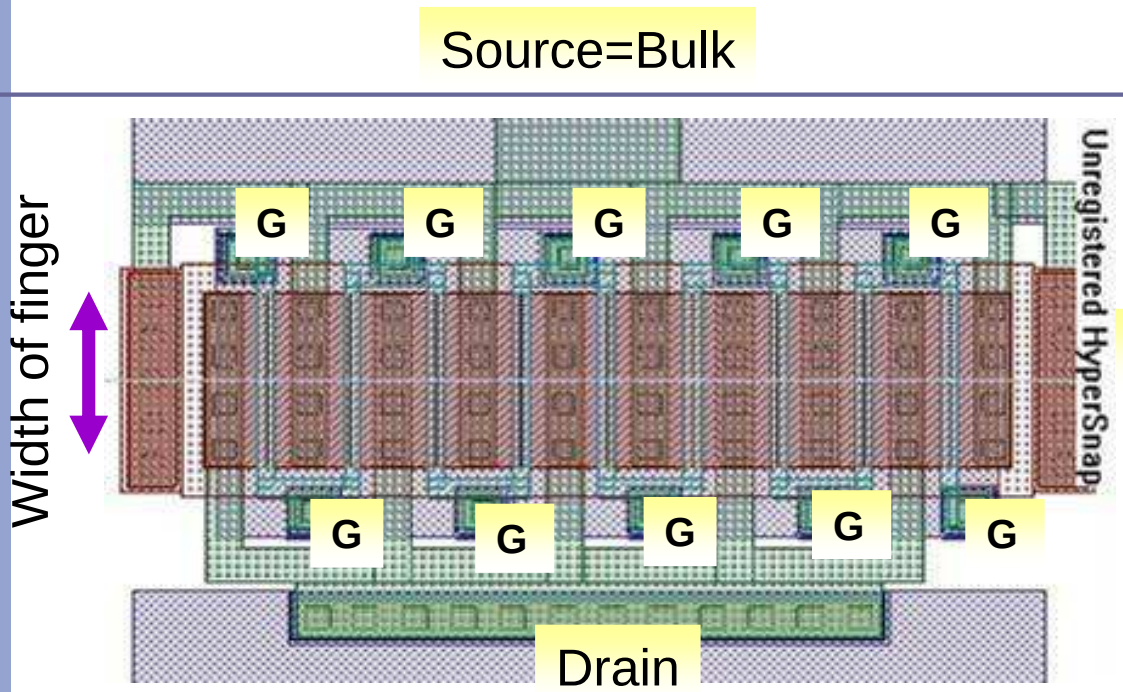
EKV3 scalable model for high frequency

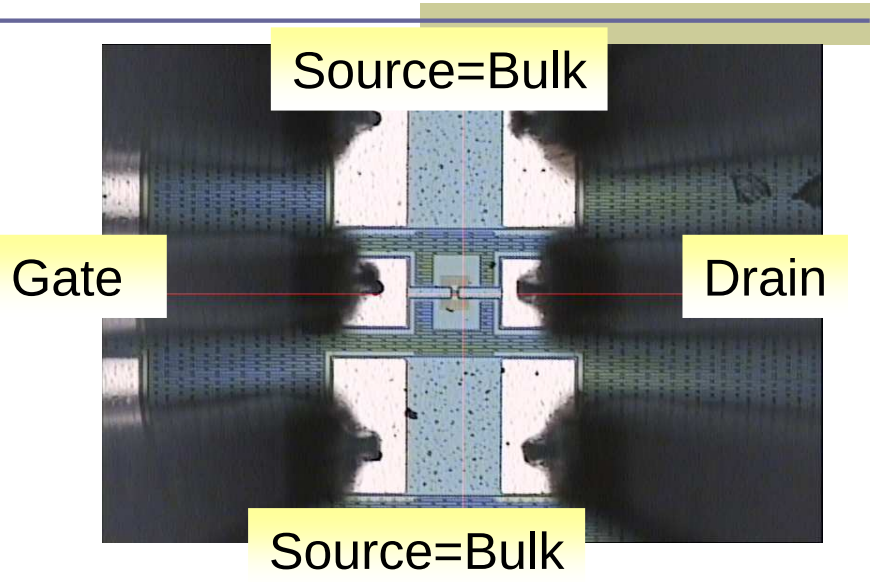


- Non quasi-static model (NQS)
  - channel segmentation
  - consistent AC/transient
- Gate- and substrate- parasitics scale with multi-finger layout

R_G	$\sim W_f/(L*N_F)$
R_{SB}, R_{DB}	$\sim 1/W_f$
R_B	$\sim 1/W_f$
R_{DSB}	$\sim L/(W_f*N_F)$

Multi-finger RF MOSFETs





- Layout of RF multi-finger MOSFET
  - Number of fingers – N_F
  - Finger Width – W_f
  - Gate Length – L
- Ground-Signal-Ground (GSG) RF Pads
  - 2 port configuration
- Open-Short de-embedding structures

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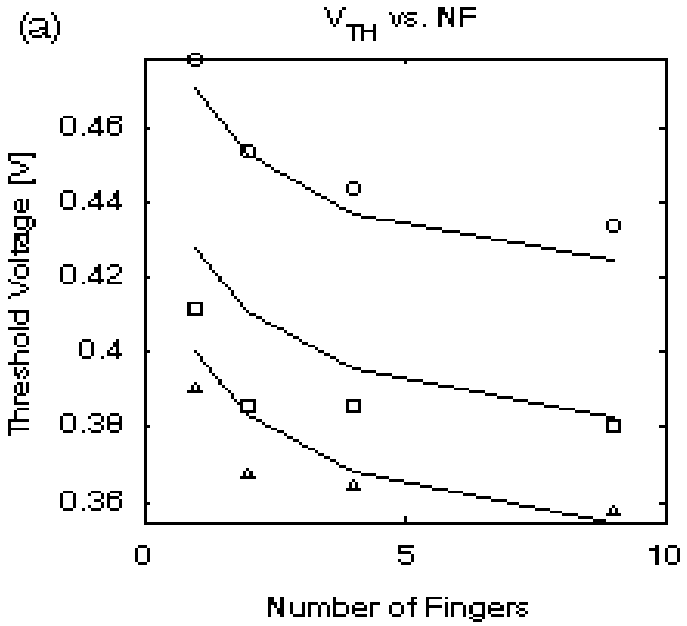
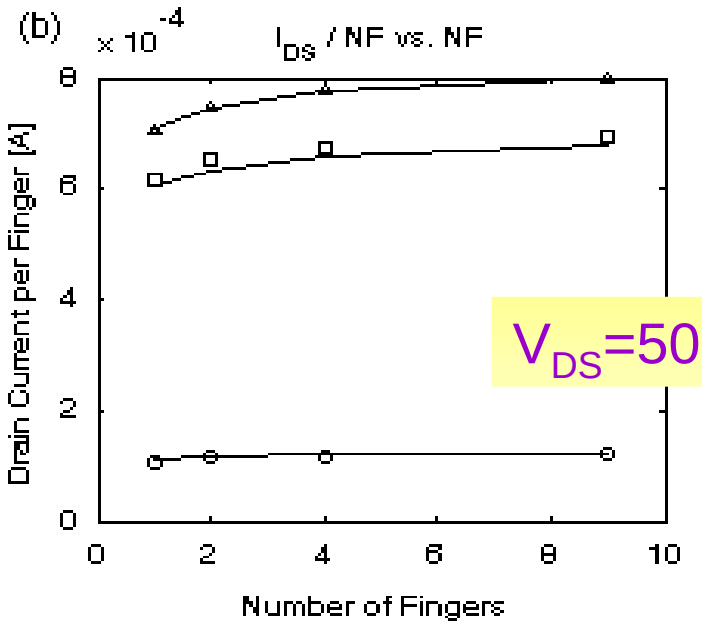
Case I: 180 nm CMOS

STI stress in multi-finger RF MOSFETs





V_{DS}=50m, 0.5, 1V

– EKV3

☐ meas.

- NMOS, L=180nm, W_f=2µm
- Stress effects due to shallow-trench isolation (STI)
  - Threshold voltage V_T vs. N_F
  - Max. drain current I_D / N_F vs. N_F

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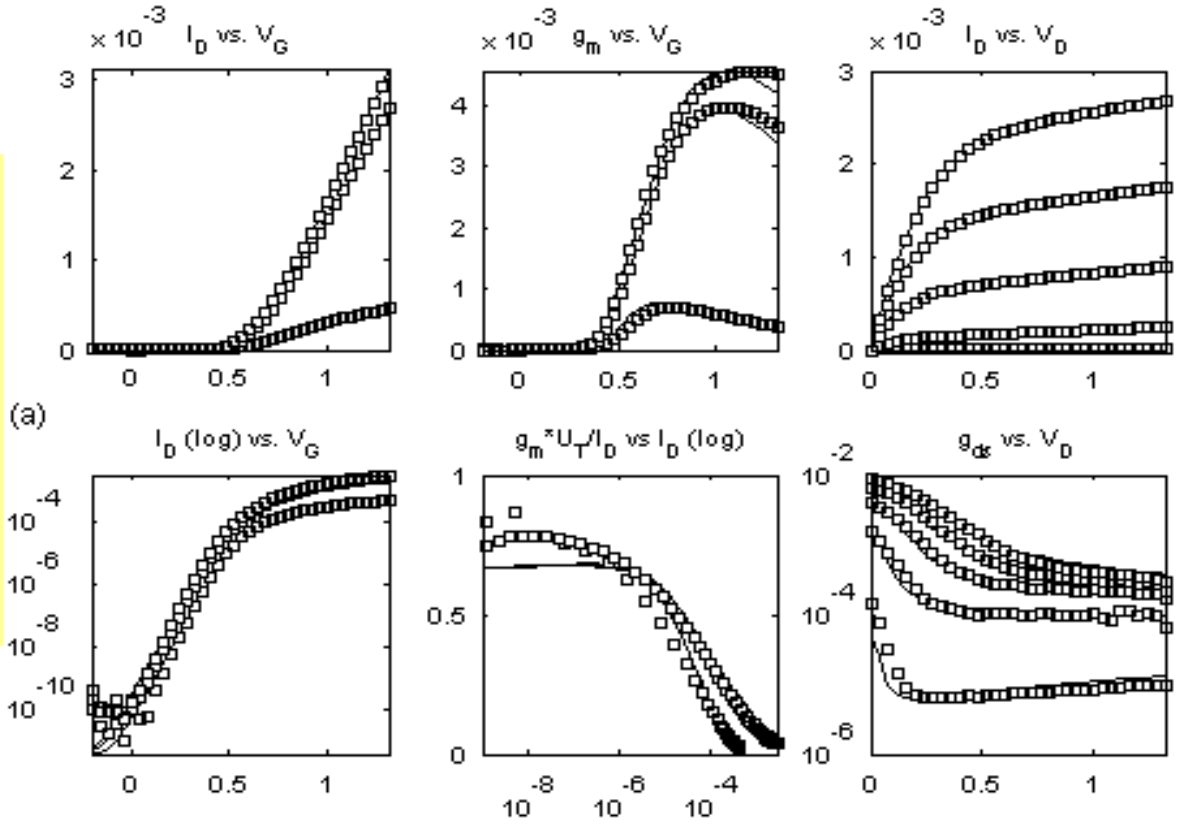
Static characteristics – NMOS



V_{DS}=50m, 0.5, 1V

V_{GS}=0.4, 0.6, 0.8, 1, 1.2V

– EKV3
☐ meas.

- NMOS, L=180nm, W_f=2µm, N_F=4
- I_D-V_G, g_m-V_G, $g_m.U_T/I_D$ – I_D
- I_D-V_D, g_{ds}-V_D

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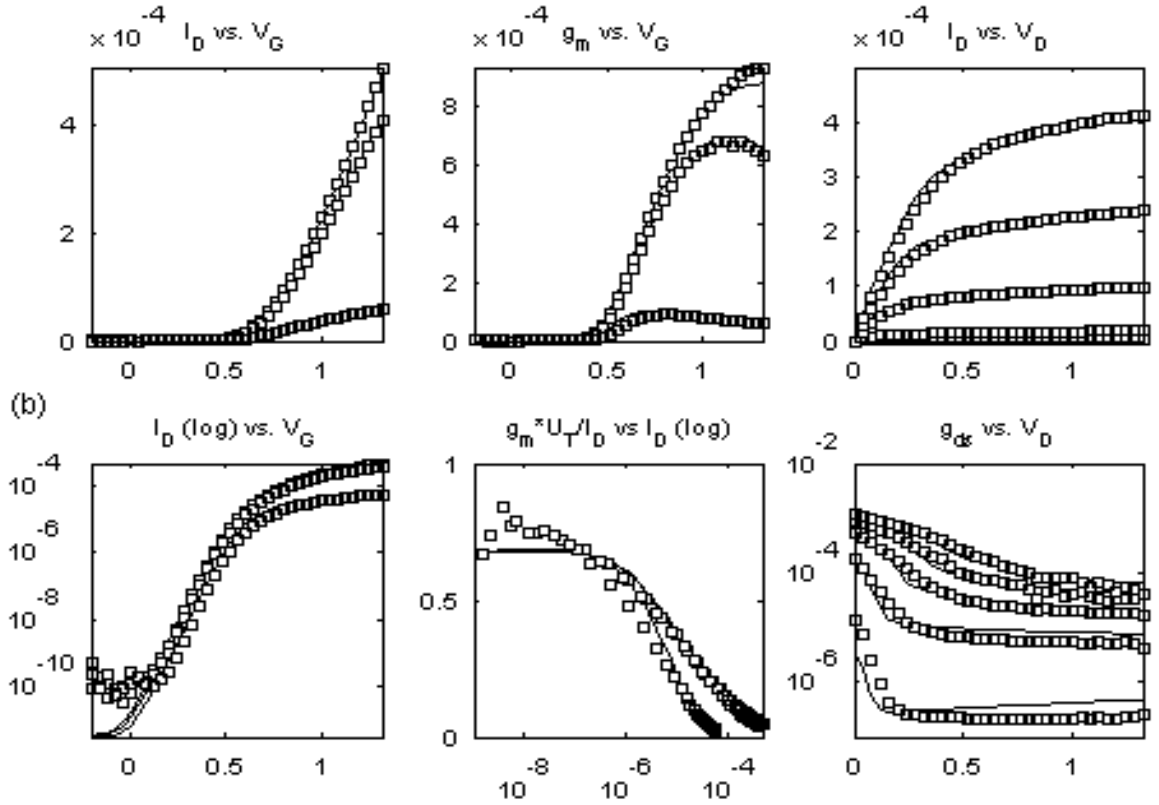
Static characteristics – PMOS

$-V_{DS}$=50m, 0.5, 1V



$-V_{GS}$=0.4, 0.6, 0.8, 1, 1.2V

– EKV3

☐ meas.

- PMOS, L=180nm, W_f=2µm, N_F=4
- I_D-V_G, g_m-V_G, $g_m.U_T/I_D$ – I_D
- I_D-V_D, g_{ds}-V_D

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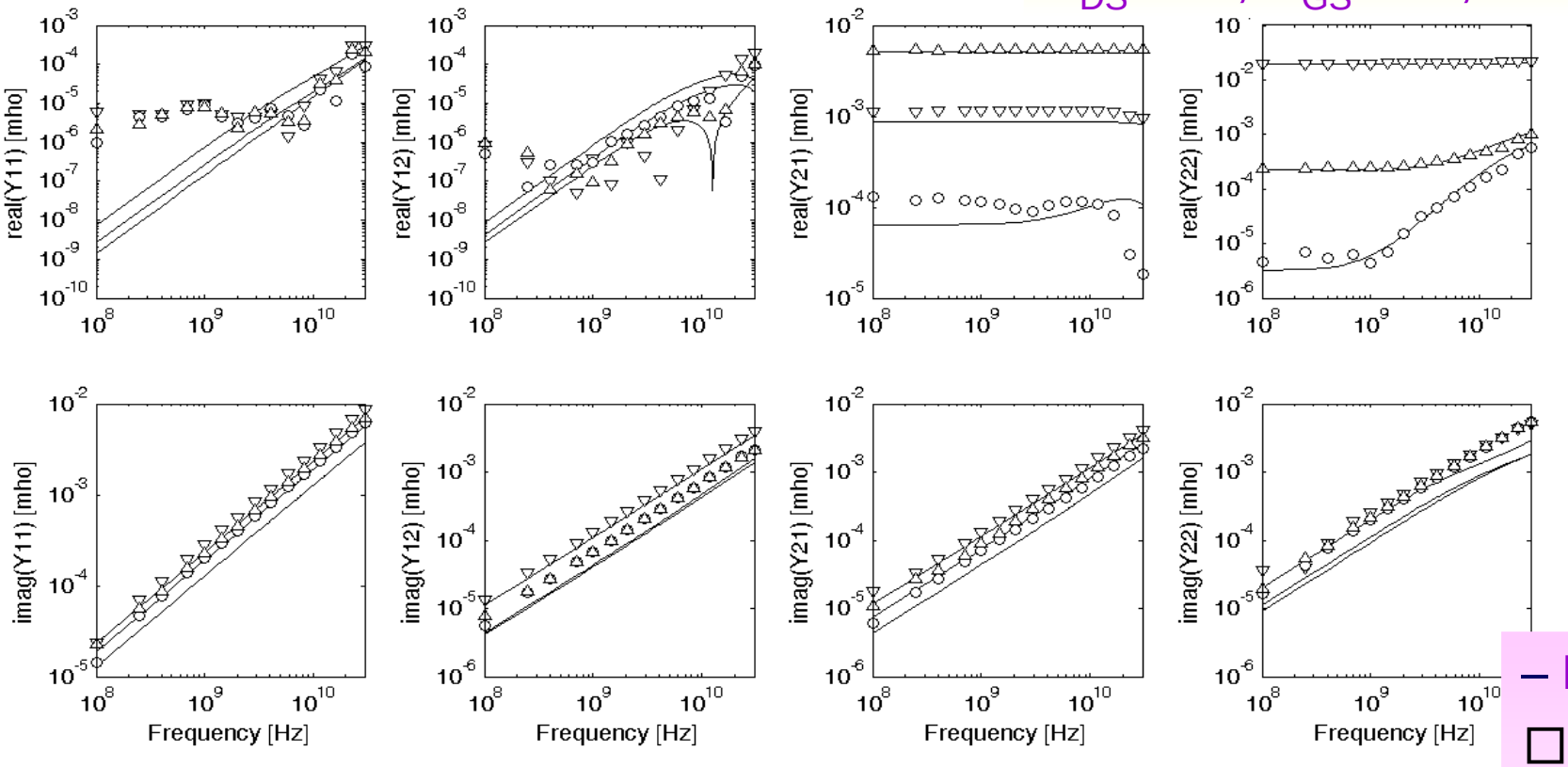
Y-parameters vs. frequency – NMOS

V_{DS}=0.3, V_{GS}=0.3, 0.6, 1.2V



- Real & Imaginary 2-port Y-parameters up to 30GHz
- NMOS, L=180nm, W_f=2µm, N_F=9

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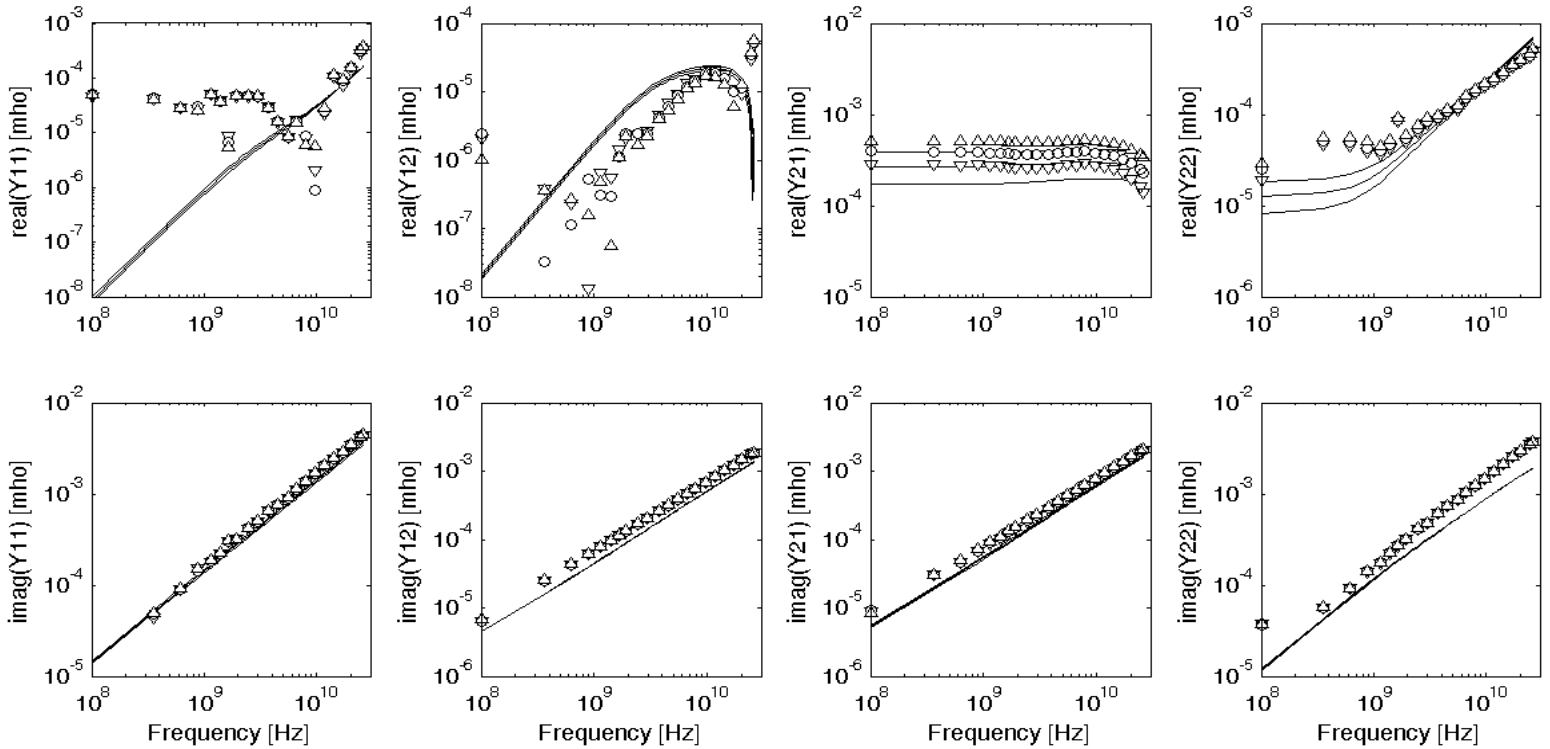
Y parameters vs. frequency – PMOS



– EKV3
☐ meas.

V_{DS}=-1.2V, -V_{GS}=0.3, 0.6, 1.2V

- Real & Imaginary 2-port Y-parameters up to 30GHz
- L=180nm, W_f=2µm, N_F=9

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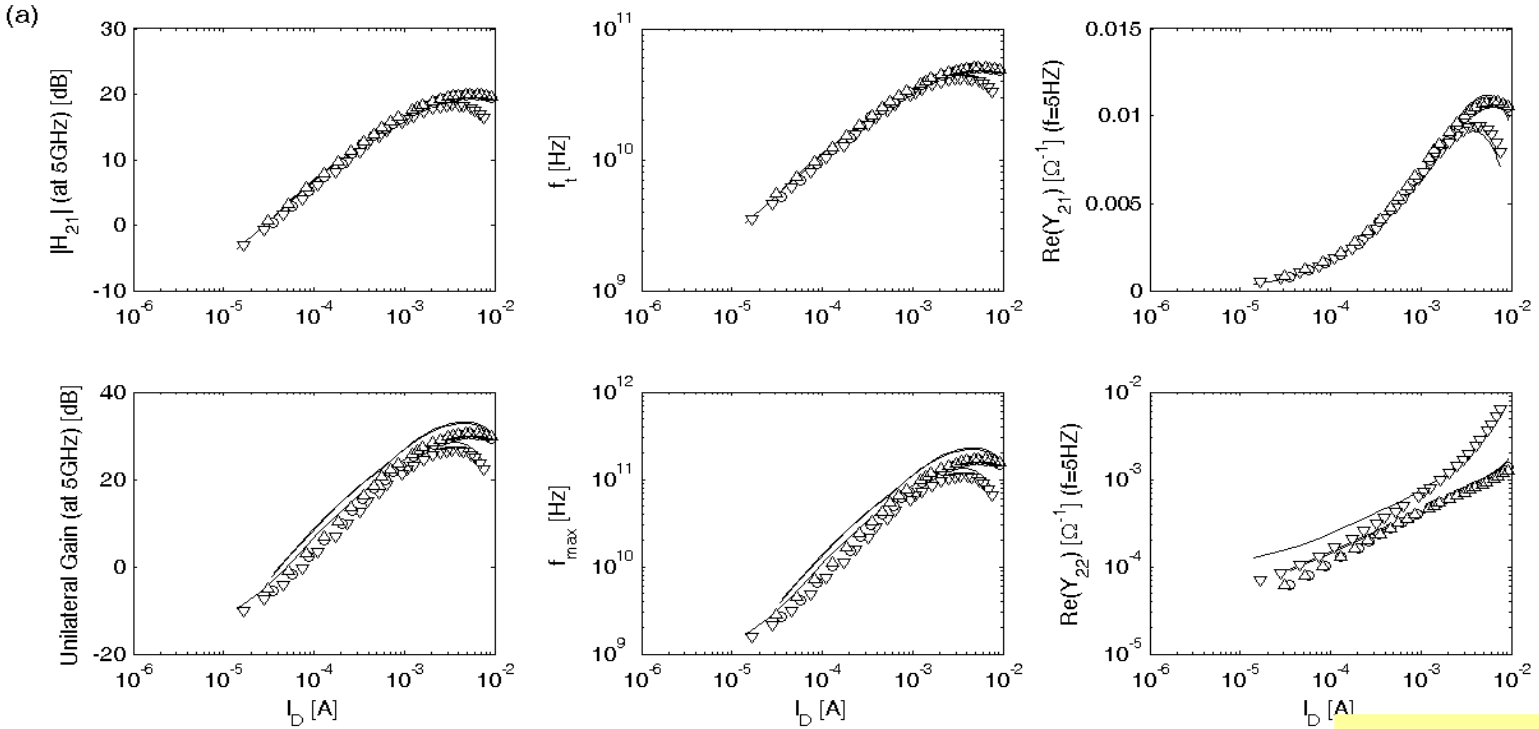
High-frequency parameters @5GHz vs. I_D – NMOS



– EKV3

☐ meas.

V_{DS}=0.5, 1.2, 1.3V

- $|H_{21}|$, U, F_T, F_{max}, $Re(Y_{21})$, $Re(Y_{22})$ vs. I_D
- L=180nm, W_f=2µm, N_F=9

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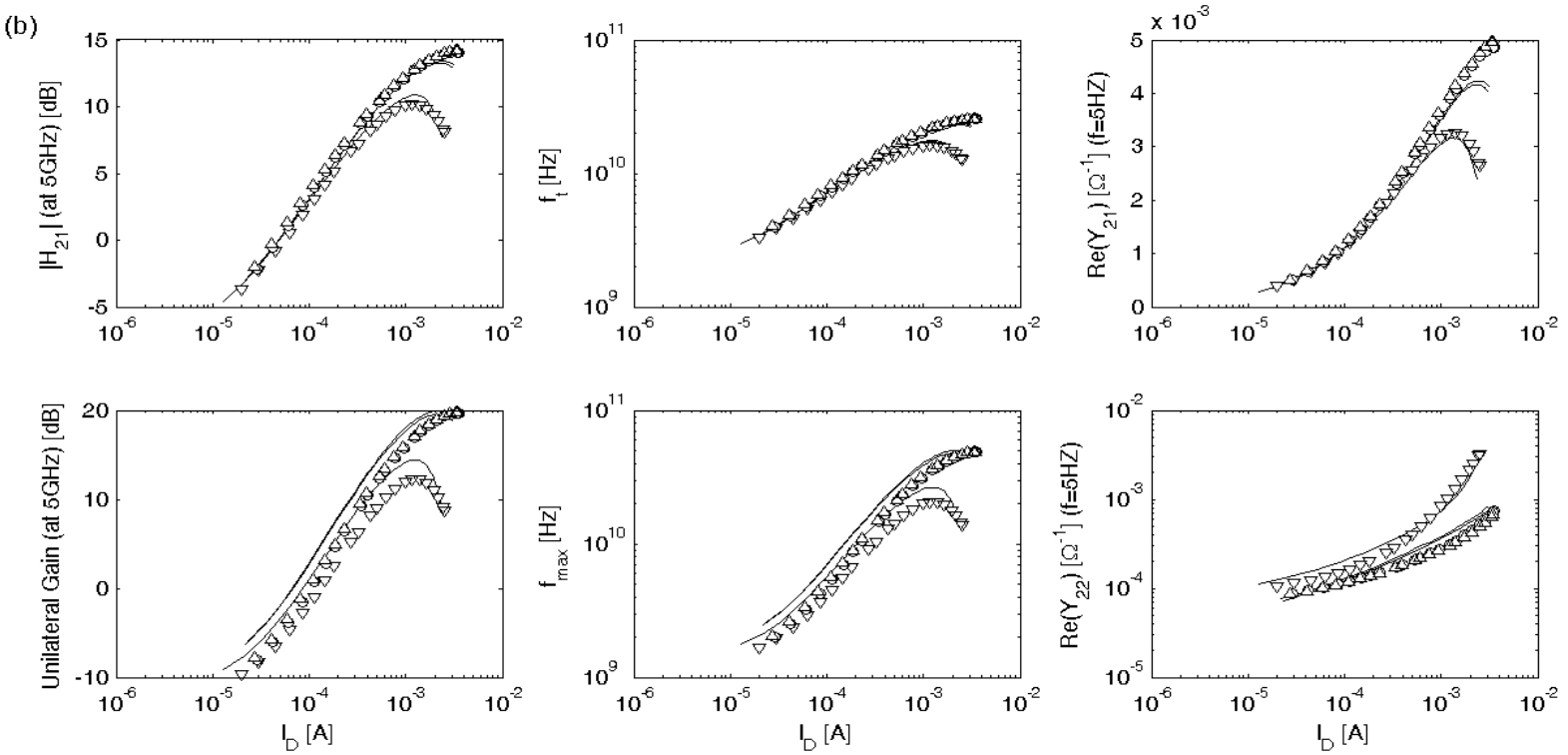
High-frequency parameters @5GHz vs. I_D – PMOS



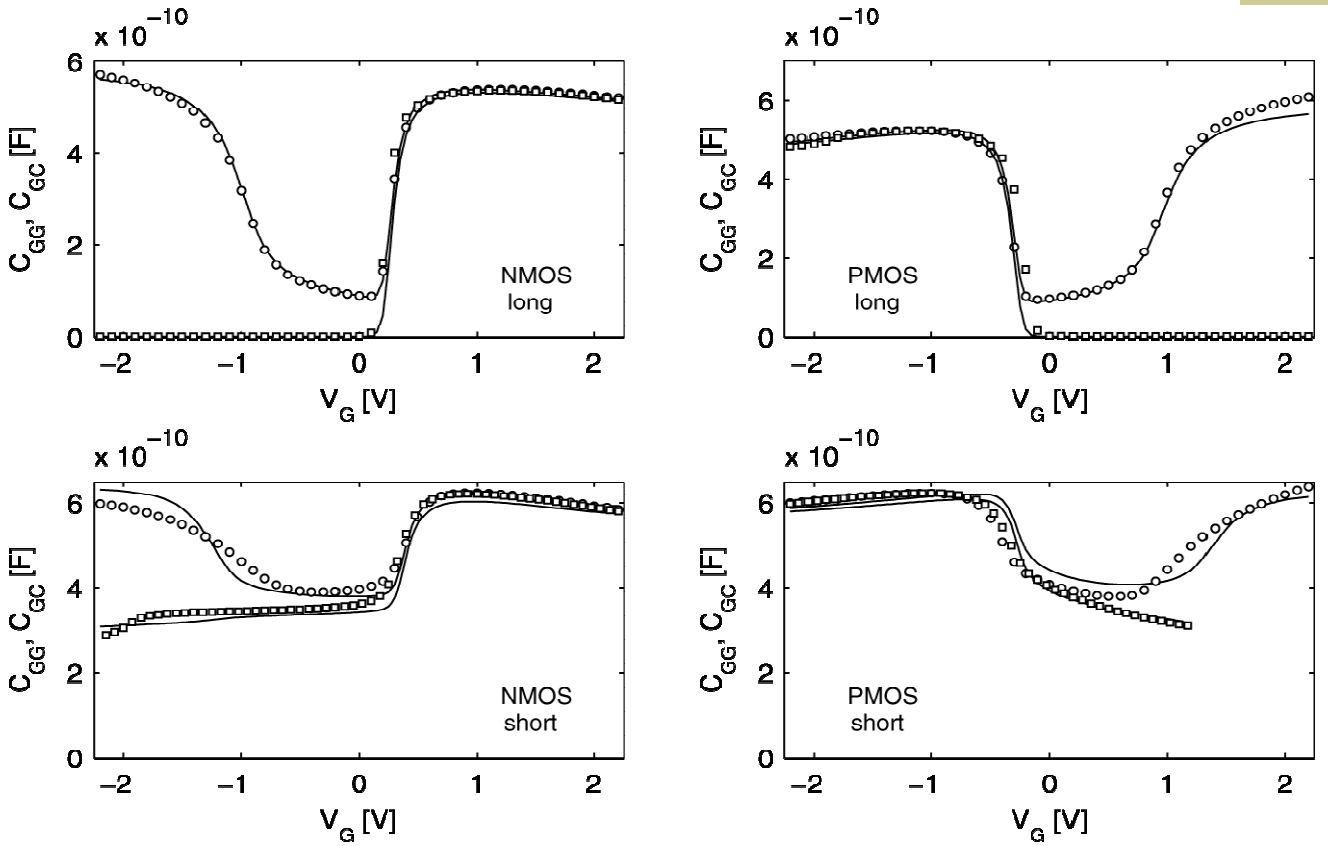
– EKV3
☐ meas.

$-V_{DS}$=0.5, 1.2, 1.3V

- $|H_{21}|$, U, F_T, F_{max}, $Re(Y_{21})$, $Re(Y_{22})$ vs. I_D
- L=180nm, W_f=2µm, N_F=9

Case II: 110 nm CMOS

Capacitance voltage characteristics



- Long/short gate and inversion capacitance

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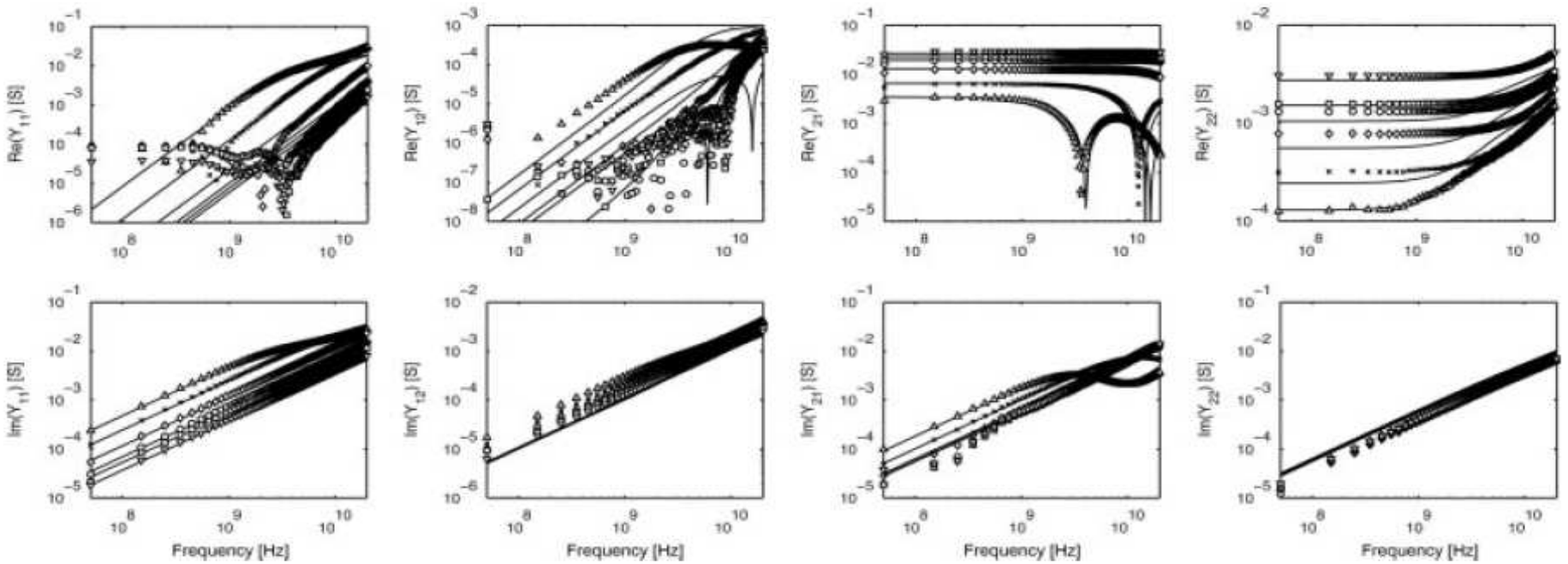
Case II: 110 nm CMOS
Scalability with L – NMOS



– EKV3
☐ meas.

- Y parameters for NMOS
  - L=110 nm, 180 nm, 250 nm, 450 nm, 1 um, 2um
  - W=5 um, NF=10
  - VG=0.6V, VD=0.5V

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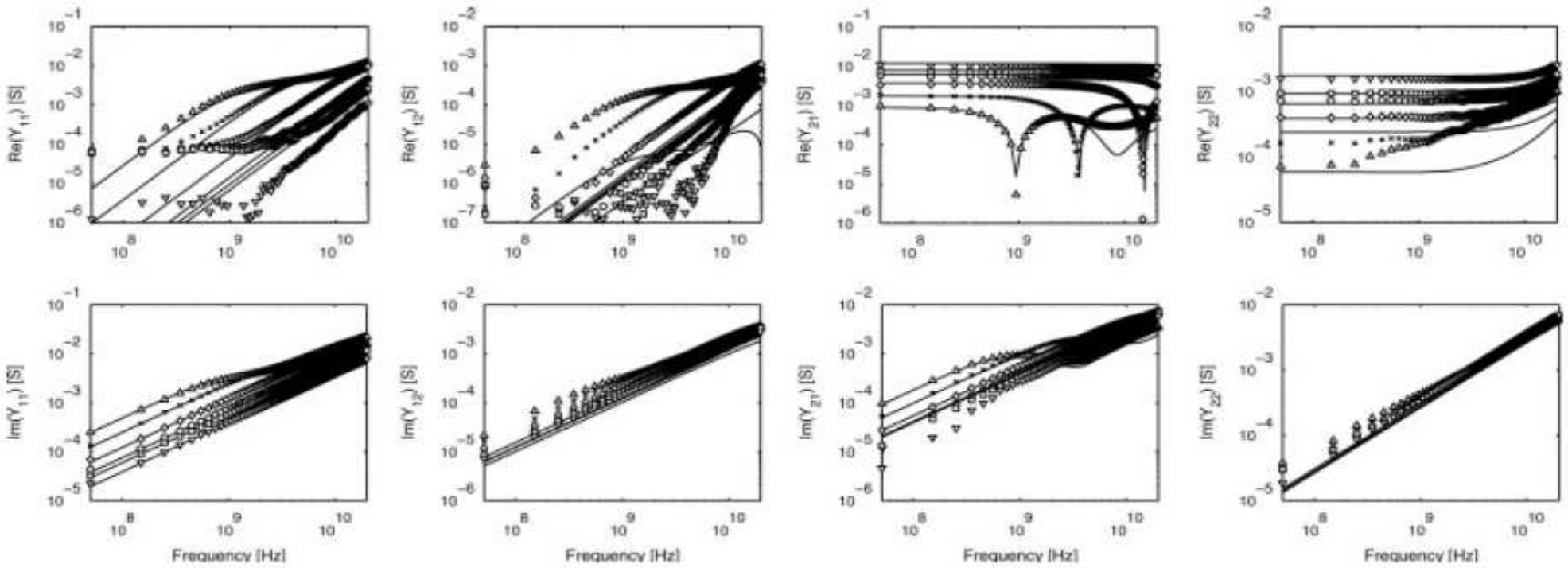
Scalability with L – PMOS



– EKV3
☐ meas.

- Y parameters for PMOS
  - L=110 nm, 180 nm, 250 nm, 450 nm, 1 um, 2um
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  - VG=0.6V, VD=0.5V

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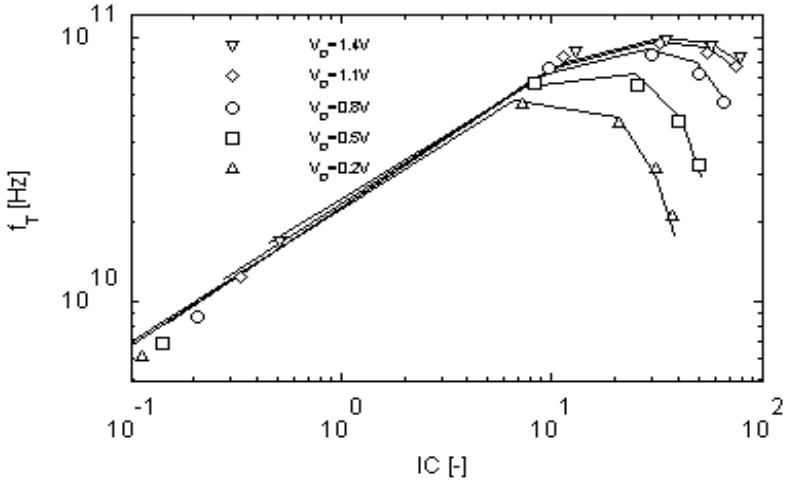
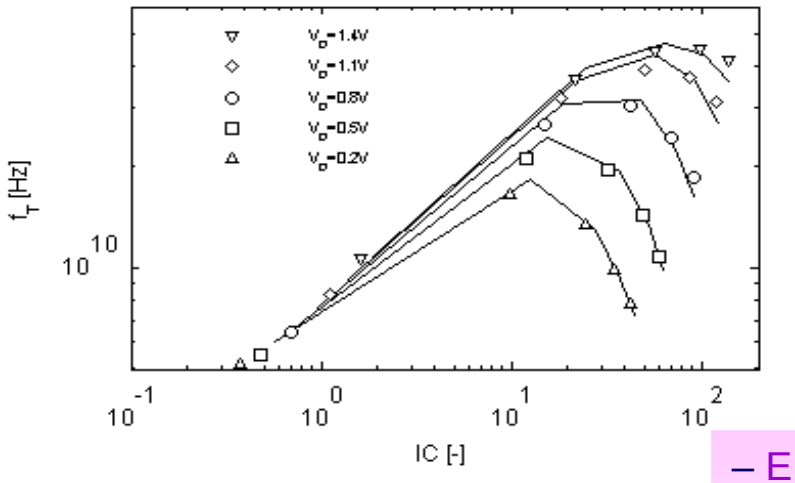
Case II: 110 nm CMOS



NMOS, L = 110nm



PMOS, L=110nm

– EKV3
☐ meas.

- f_T versus IC in 110nm CMOS, EKV301.02 model
  - IC = I_D / I_{spec} where I_{spec} = I_0*W/L
- Highest f_T is reached at IC ~10-30 (!)
- Most probable range for biasing of RF circuits for low noise is:
  1 < IC < 10 (depending on techn

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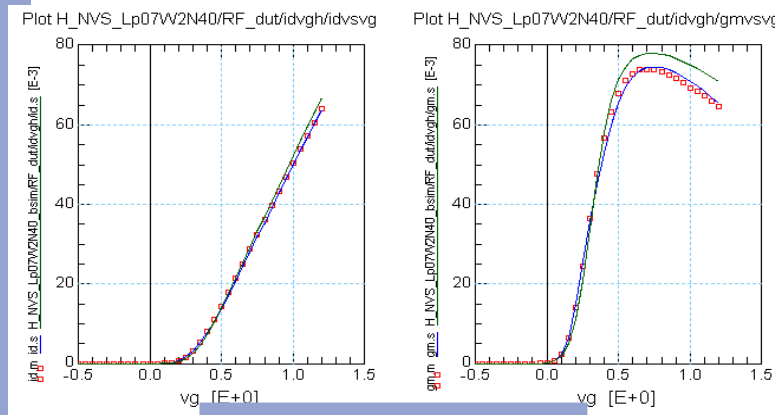
Case III: 90nm CMOS

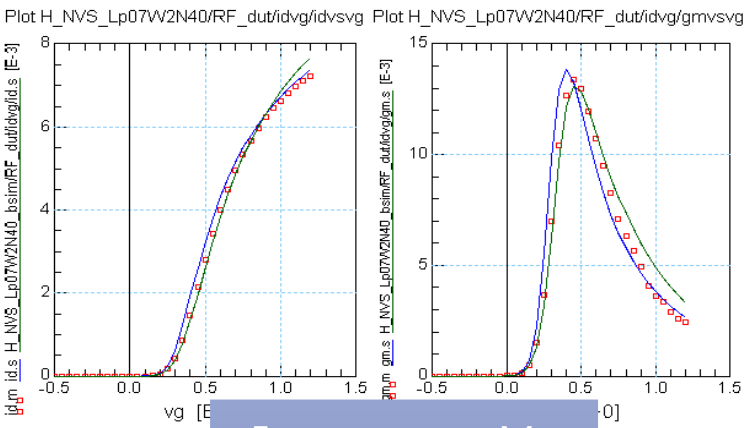
- DUTs: NMOS*, PMOS
  - nominal L = 70 nm, W = 2 um
  - multi-finger N_F = 40

* *Comparison with BSIM4*

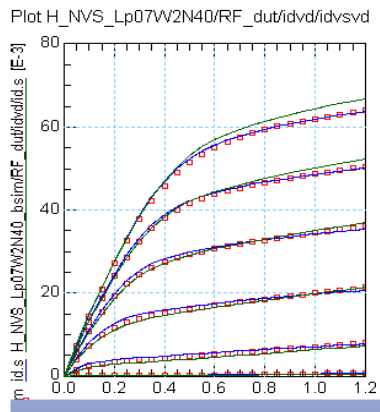
DUT: **NMOS**; W_F = 2um; L_F = 70nm; N_F = **40**
I_D vs. V_G (linear, saturation); V_{SB} = 0V



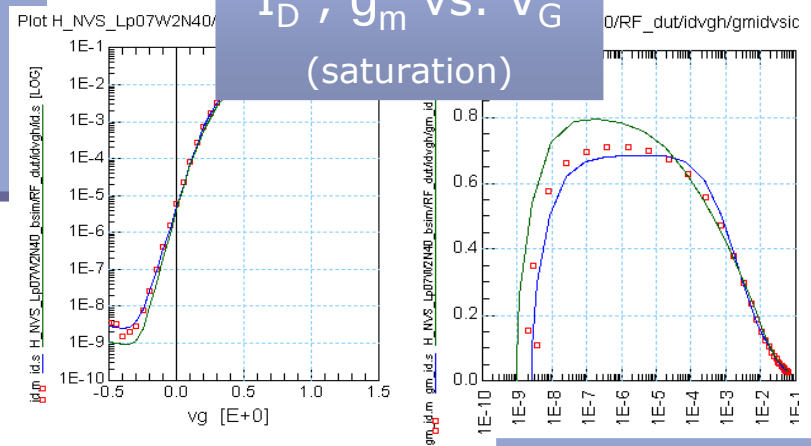
I_D , g_m vs. V_G (saturation)



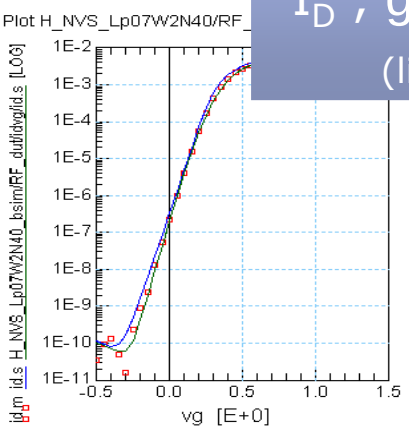
I_D , g_m vs. V_G (linear)

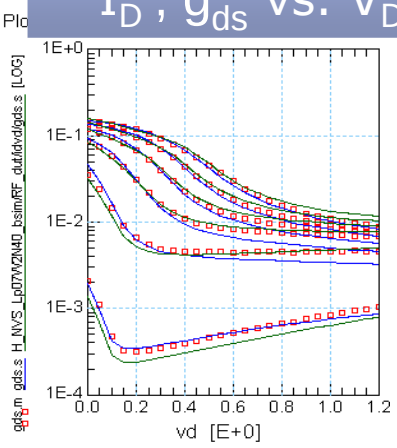


I_D , g_{ds} vs. V_D



g_m/I_D vs. I_D





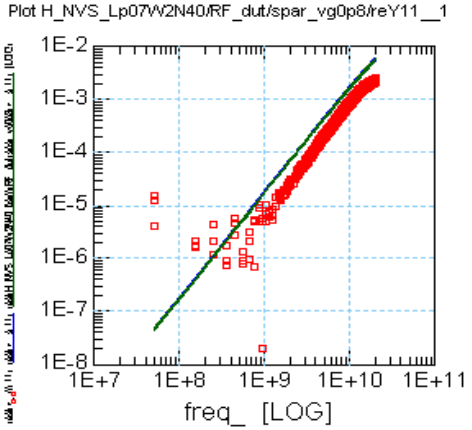
Measurements / EKV3 / BSIM4

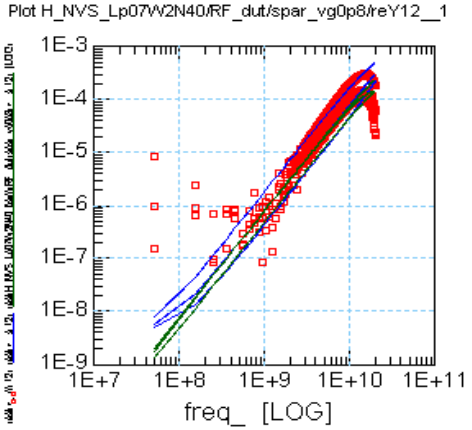
DUT: **NMOS**; W_F = 2um; L_F = 70nm; N_F = **40**
Y-parameters; V_{GS}=0.8V; V_{DS}={0.4, 0.6, 0.8}V; V_{SB}=0V

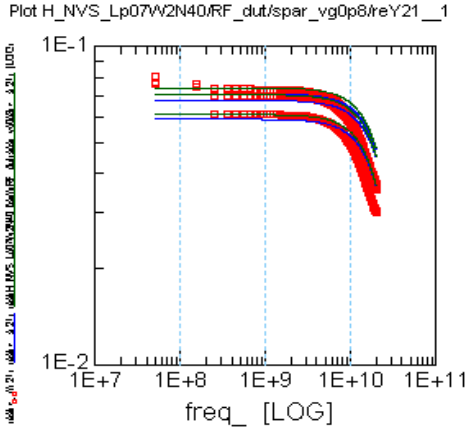
real

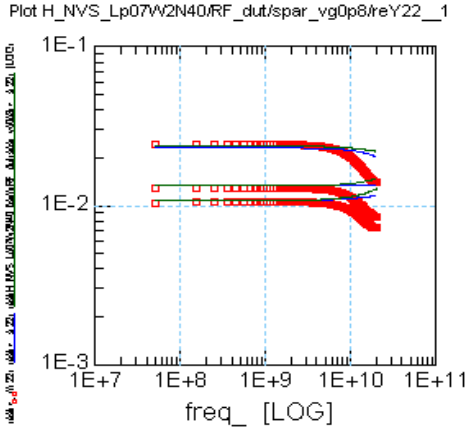
imaginary

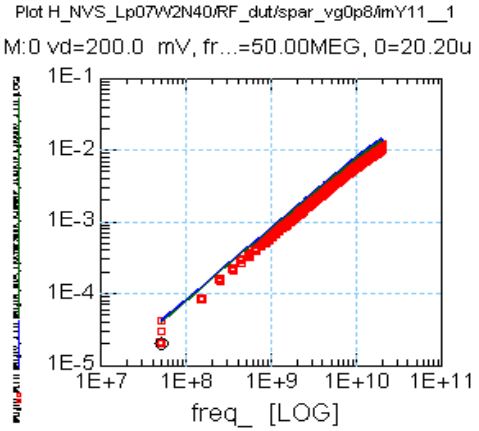
Y_{11} Y_{12} Y_{21} Y_{22}

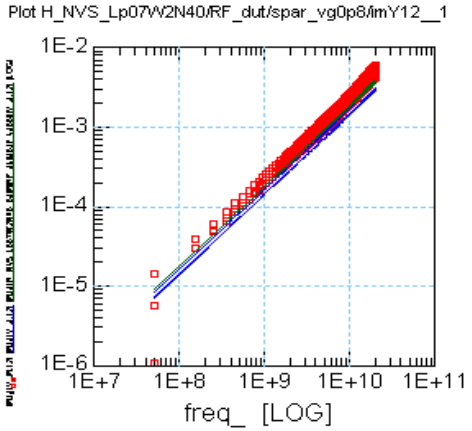


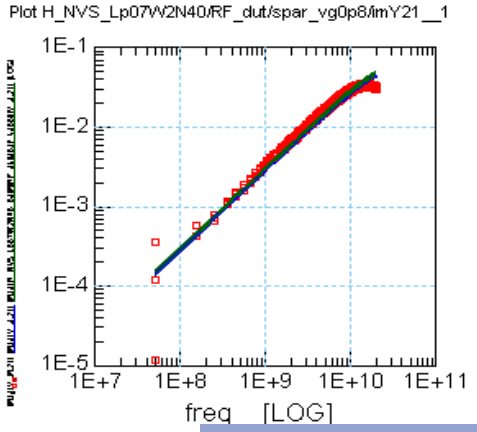


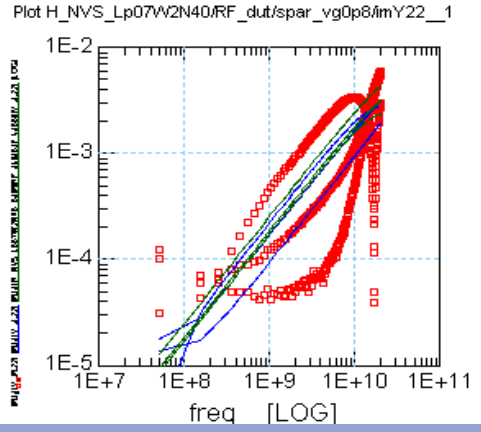












Measurements / EKV3 / BSIM4

DUT: **PMOS**; W_F = 2um; L_F = 70nm; N_F = **40**
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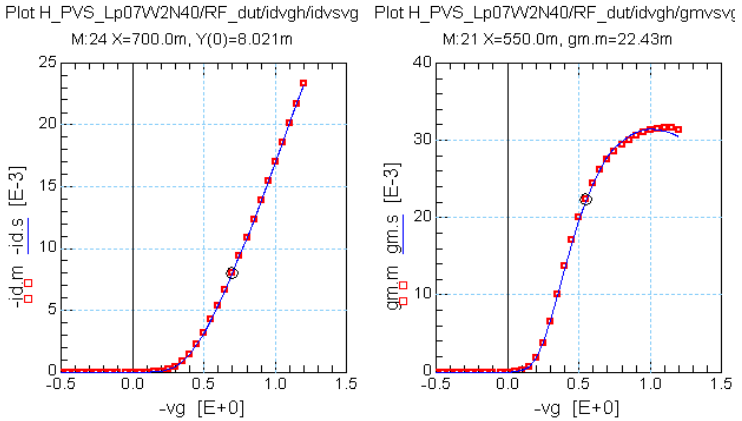
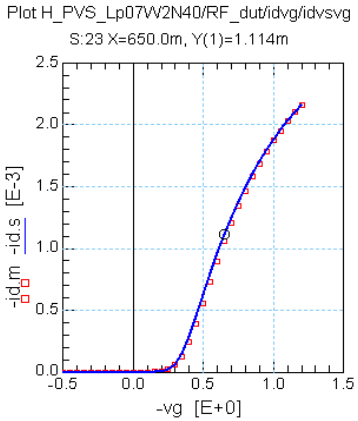
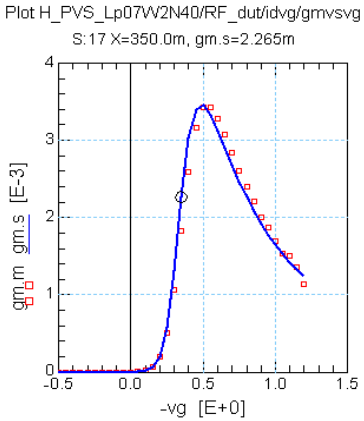
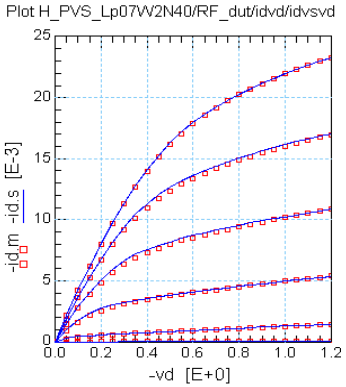
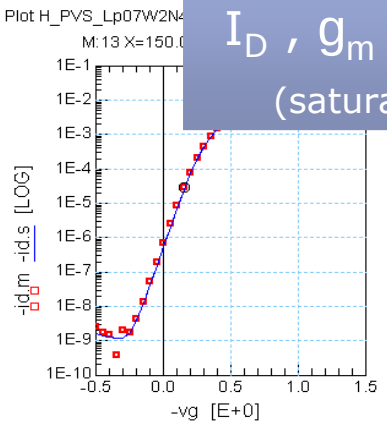


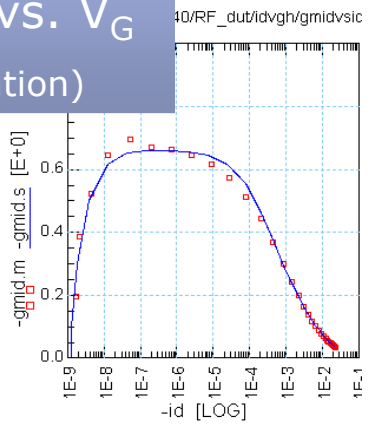






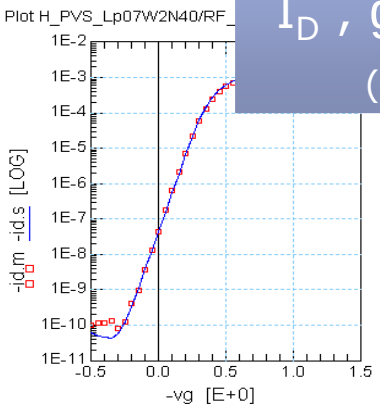
I_D , g_m vs. V_G (saturation)



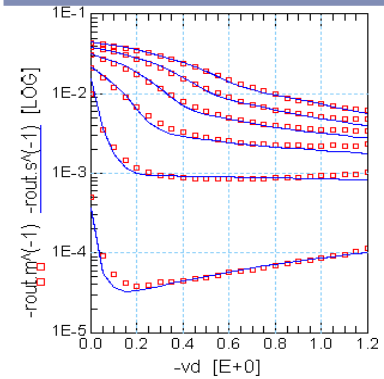


g_m/I_D vs. I_D

I_D , g_m vs. V_G (linear)



I_D , g_{ds} vs. V_D



Measurements / **EKV3**

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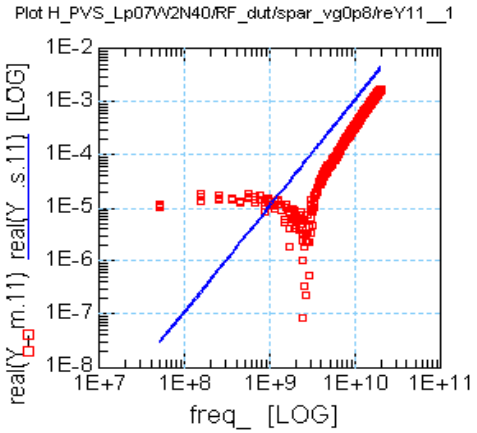
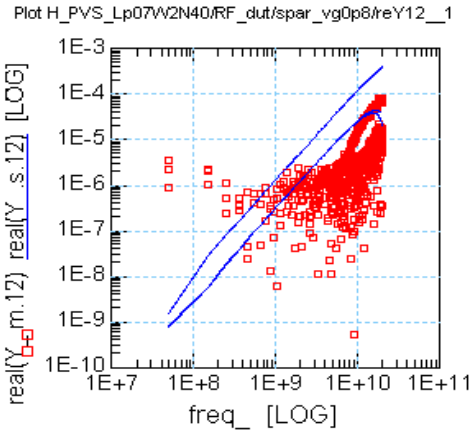
Y-parameters; $|V_{GS}|$=0.8V;$|V_{DS}|$={0.4,0.6,0.8}V;V_{SB}=0V

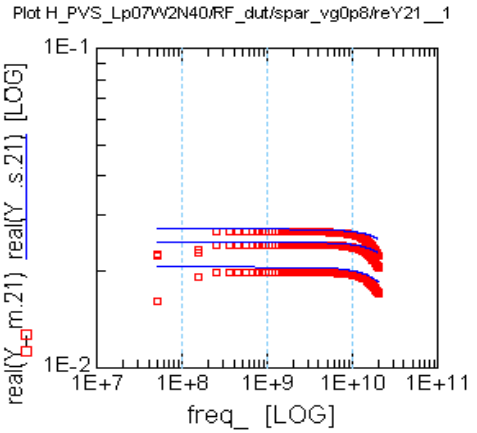
real

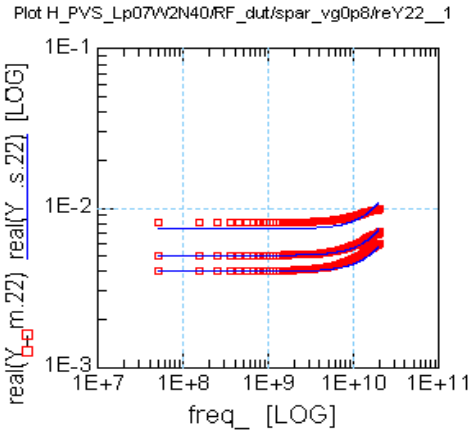
imaginary

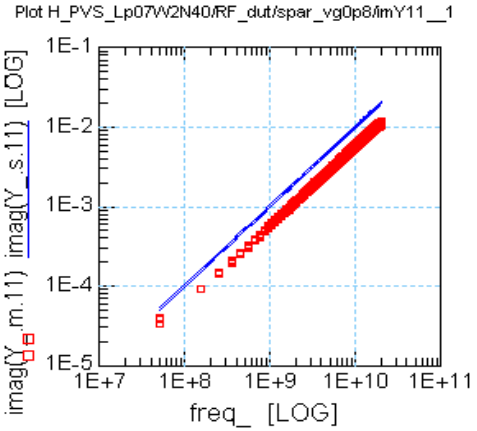
Y_{11} Y_{12} Y_{21} Y_{22}

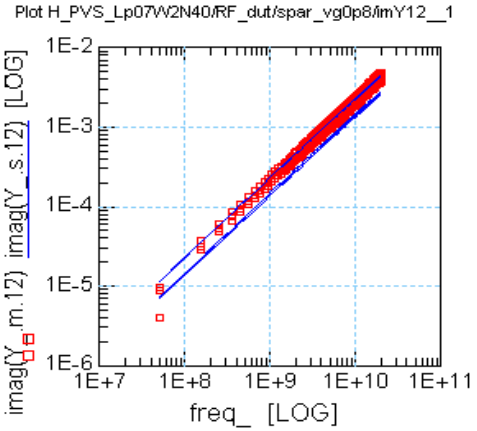


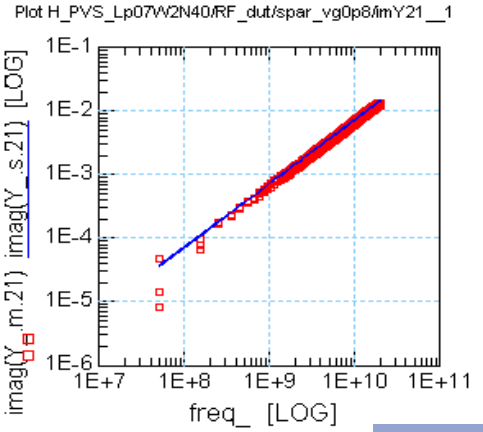


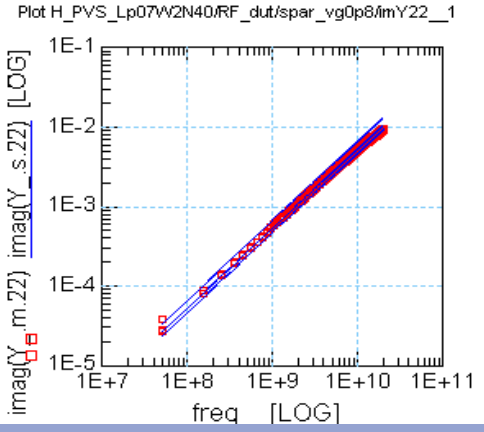












Measurements / EKV3

Conclusions

- EKV3: analog/RF IC design-oriented, charge-based, compact model
  - Implementations in:
    - ELDO (Mentor Graphics)
    - Smash (Dolphin)
    - Spectre (Cadence).
  - Parameter extraction support (GMC Suisse & AdMOS)
- Model covers all RF aspects from DC to RF (small/large signal including NQS) and Noise.
  - Extended RF validations in 180nm, 110nm, 90nm CMOS.
  - Fully scalable with L, W, NF, bias, f, technology
  - Simple model structure & parameter extraction.
- Relation to advanced analog/RF IC design.

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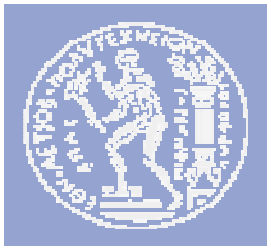

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