

ESSCIRC/ESSDERC Workshops, MOS-AK Meeting
Edinburgh, September 15-19, 2008

Aspects of High-Frequency Modelling with EKV3

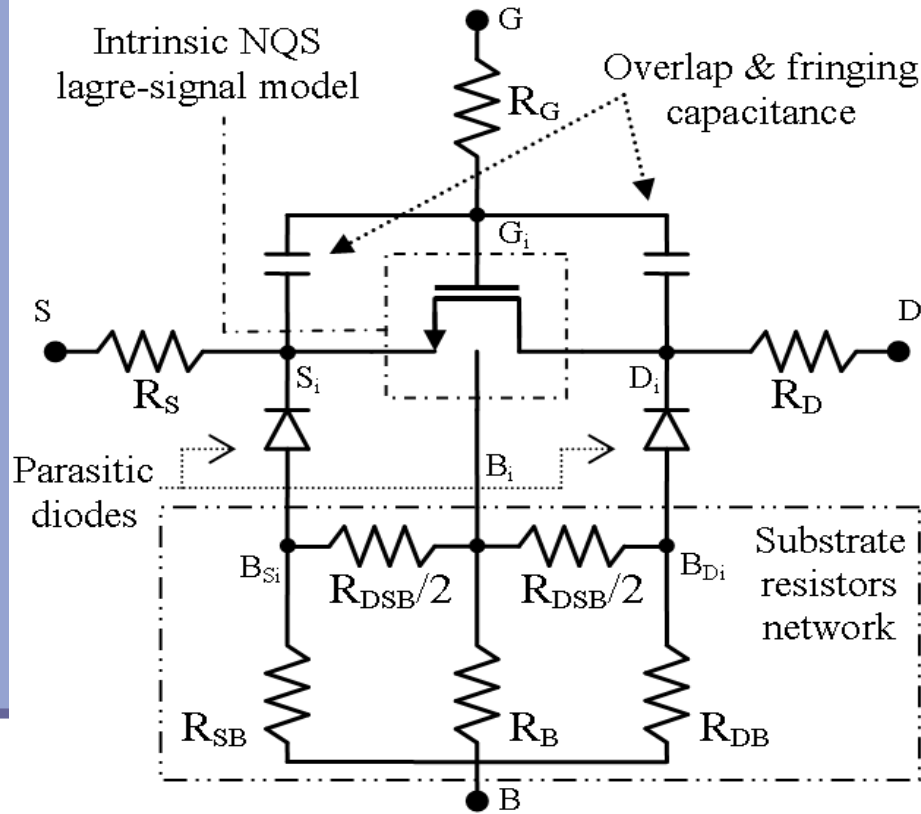
Matthias Bucher, Maria-Anna Chalkiadaki
Technical University of Crete (TUC), Chania, Greece

Antonios Bazigos
National Technical University of Athens (NTUA), Athens, Greece

Outline

- Introduction
- Case I: 180 nm CMOS
- Case II: 110 nm CMOS
- Case III: 90 nm CMOS
- Conclusions

EKV3 scalable model for high frequency

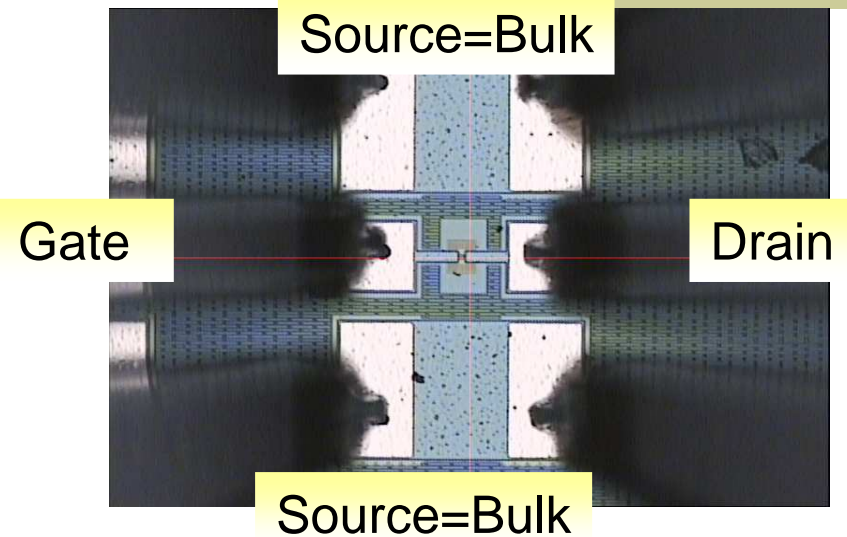
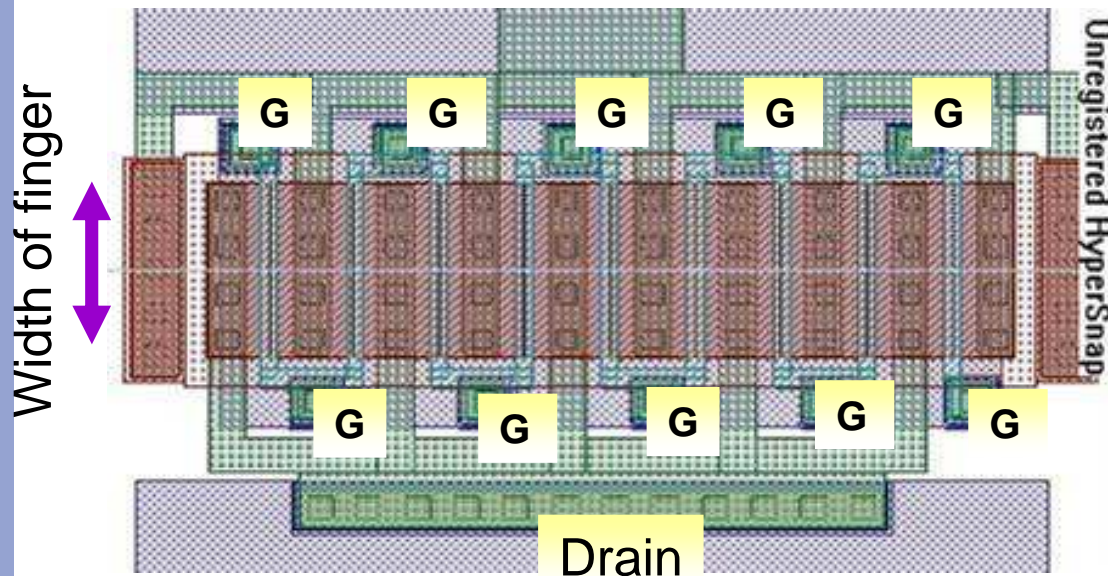


- Non quasi-static model (NQS)
 - channel segmentation
 - consistent AC/transient
- Gate- and substrate- parasitics scale with multi-finger layout

R_G	$\sim W_f / (L * N_F)$
R_{SB}, R_{DB}	$\sim 1 / W_f$
R_B	$\sim 1 / W_f$
R_{DSB}	$\sim L / (W_f * N_F)$

Multi-finger RF MOSFETs

Source=Bulk



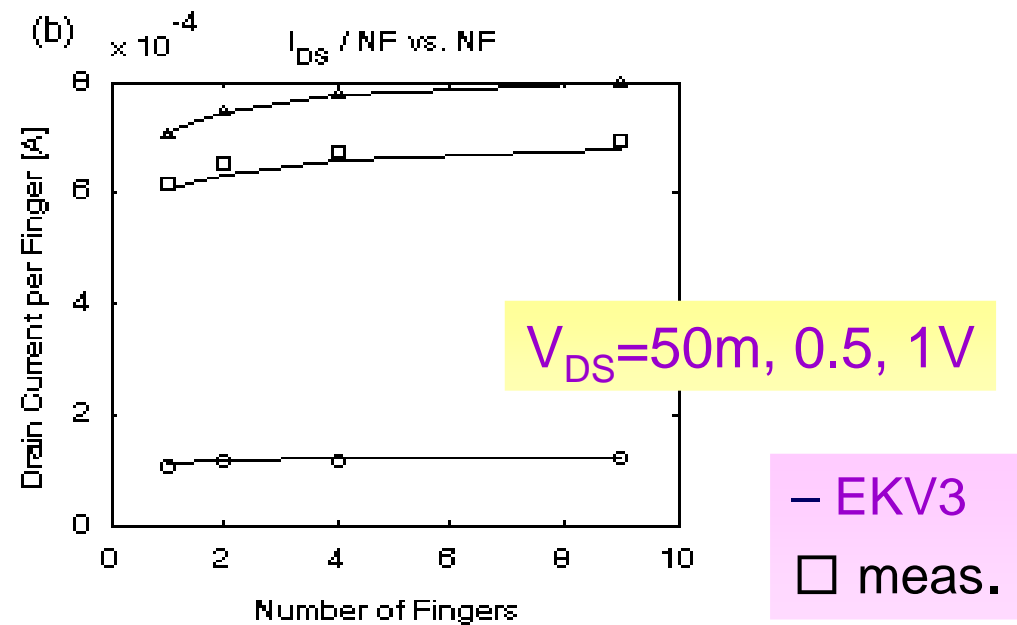
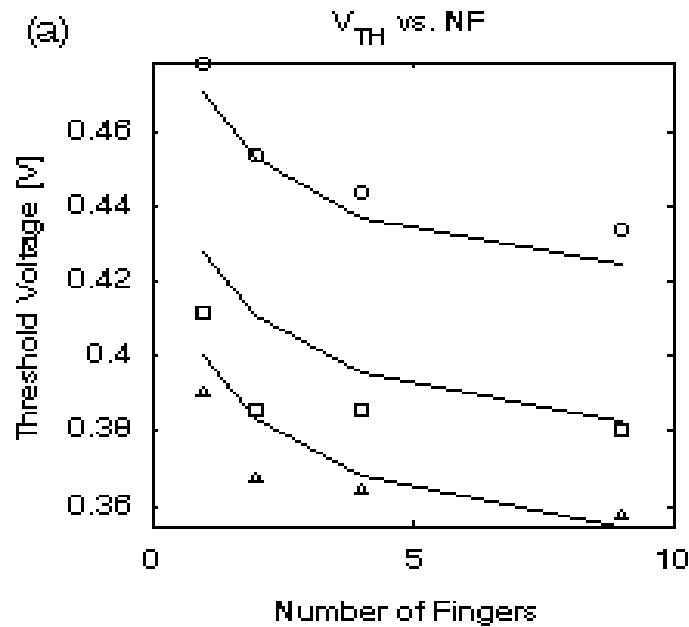
- Layout of RF multi-finger MOSFET
 - Number of fingers – N_F
 - Finger Width – W_f
 - Gate Length – L

- Ground-Signal-Ground (GSG) RF Pads
 - 2 port configuration
- Open-Short de-embedding structures

A. Bazigos e.a. Physica Status Solidi C, 2008

Case I: 180 nm CMOS

STI stress in multi-finger RF MOSFETs

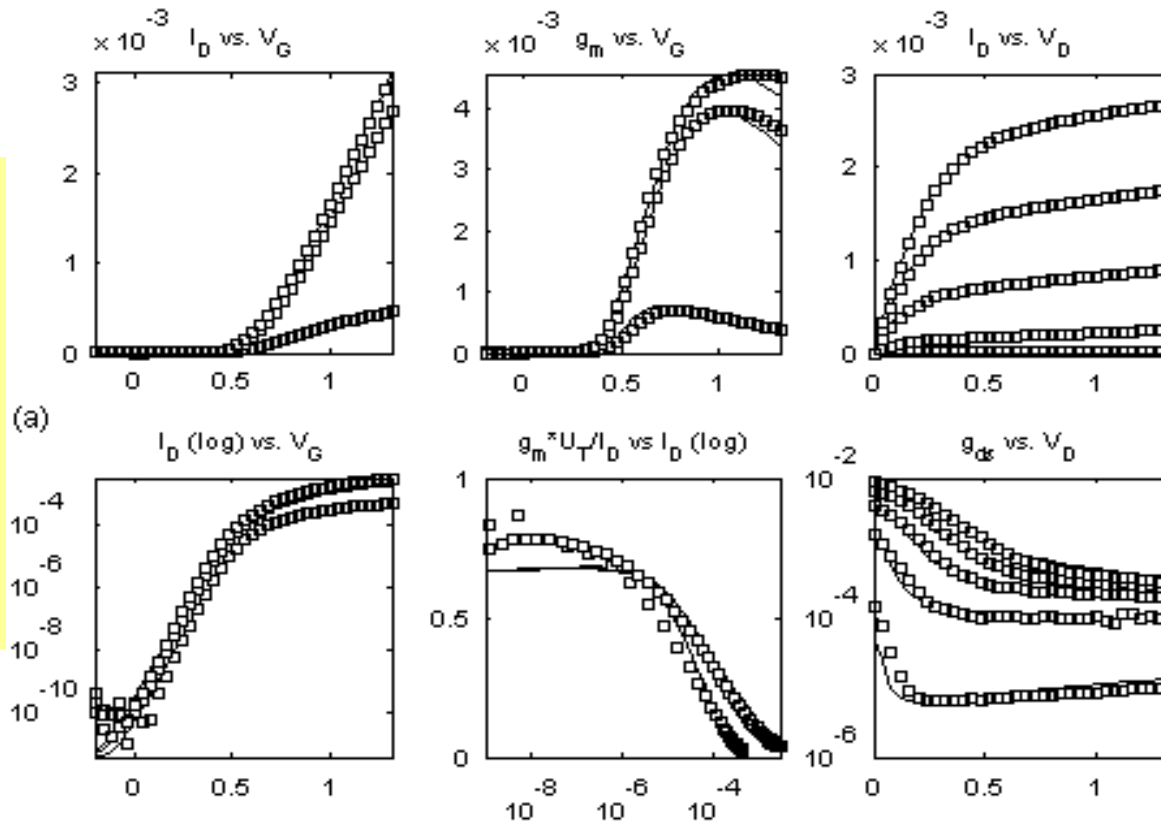


- NMOS, $L=180nm$, $W_f=2\mu m$
- Stress effects due to shallow-trench isolation (STI)
 - Threshold voltage V_T vs. N_F
 - Max. drain current I_D / N_F vs. N_F

A. Bazigos e.a. Physica Status Solidi C, 2008

Static characteristics – NMOS

$V_{DS}=50m, 0.5, 1V$



$V_{GS}=0.4, 0.6, 0.8, 1, 1.2V$

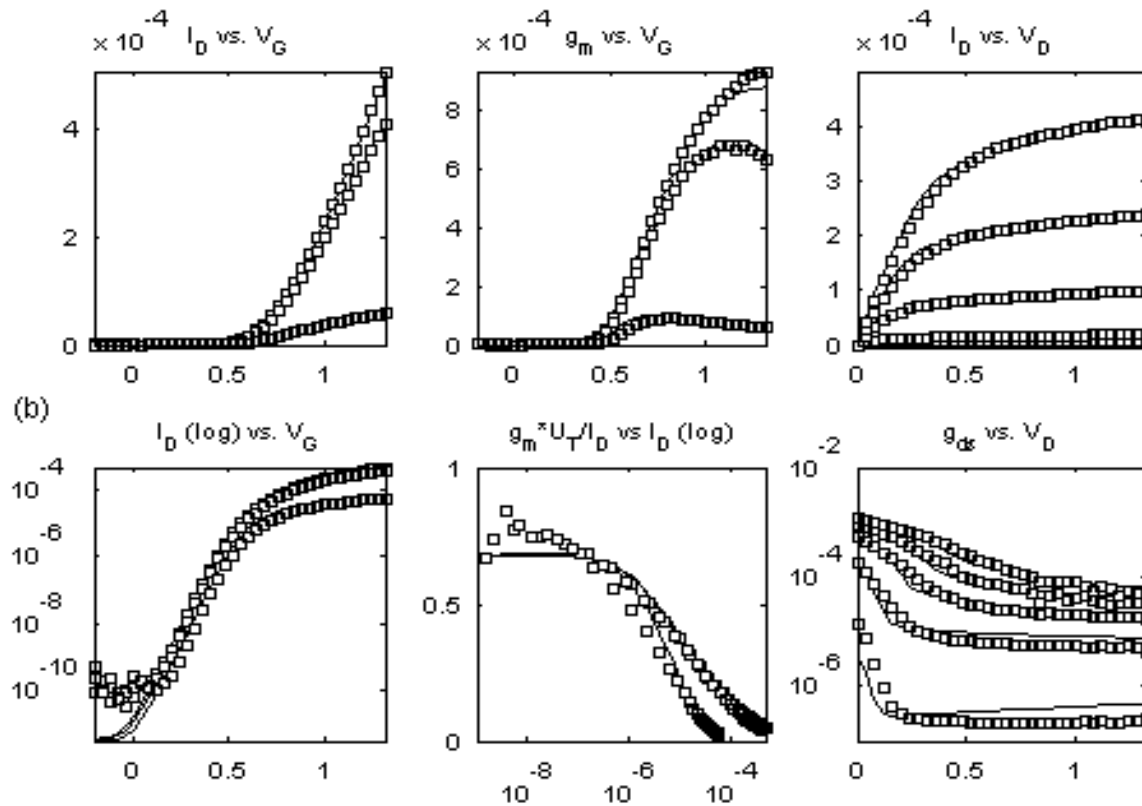
– EKV3
□ meas.

- NMOS, $L=180nm$, $W_f=2\mu m$, $N_F=4$
- I_D - V_G , g_m - V_G , $g_m \cdot U_T / I_D$ – I_D
- I_D - V_D , g_{ds} - V_D

A. Bazigos e.a. Physica Status Solidi C, 2008

Static characteristics – PMOS

$-V_{DS}=50\text{m}, 0.5, 1\text{V}$



$-V_{GS}=0.4, 0.6, 0.8, 1, 1.2\text{V}$

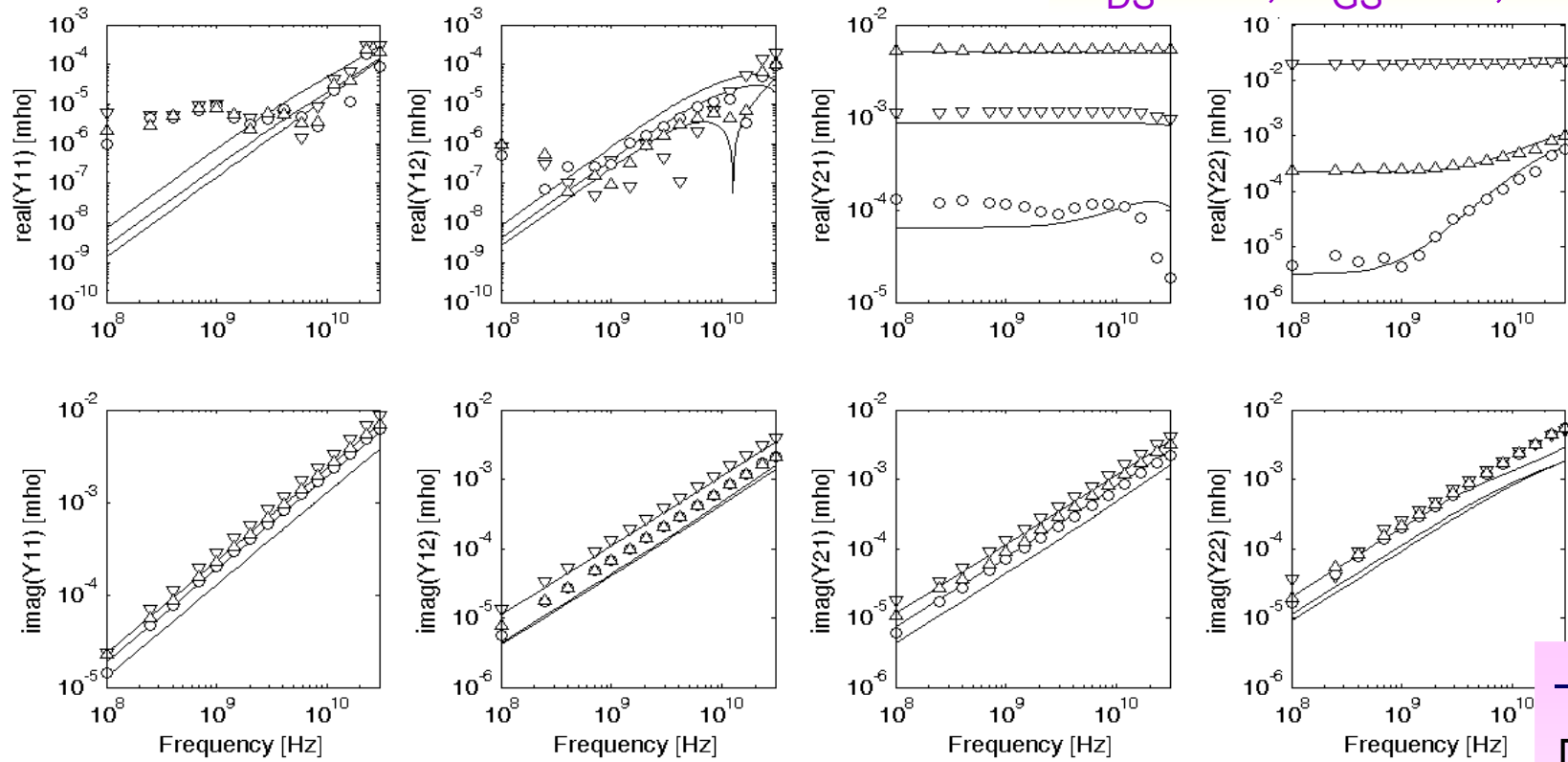
– EKV3
 □ meas.

- PMOS, $L=180\text{nm}$, $W_f=2\mu\text{m}$, $N_F=4$
- I_D - V_G , g_m - V_G , $g_m \cdot U_T / I_D - I_D$
- I_D - V_D , g_{ds} - V_D

A. Bazigos e.a. Physica Status Solidi C, 2008

Y-parameters vs. frequency – NMOS

$V_{DS}=0.3, V_{GS}=0.3, 0.6, 1.2V$

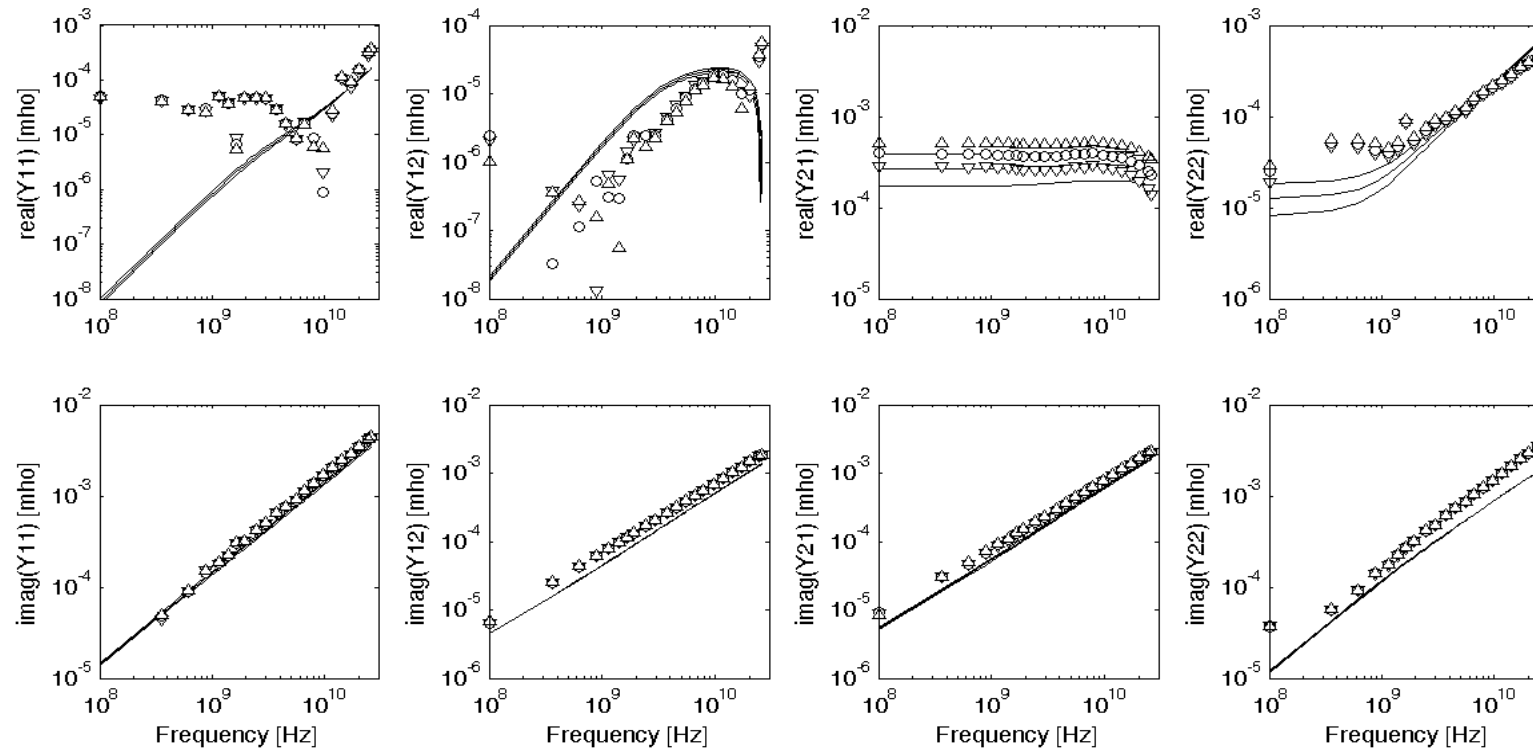


— EKV3
 □ meas.

- Real & Imaginary 2-port Y-parameters up to 30GHz
- NMOS, $L=180nm, W_f=2\mu m, N_F=9$

A. Bazigos e.a. Physica Status Solidi C, 2008

Y parameters vs. frequency – PMOS



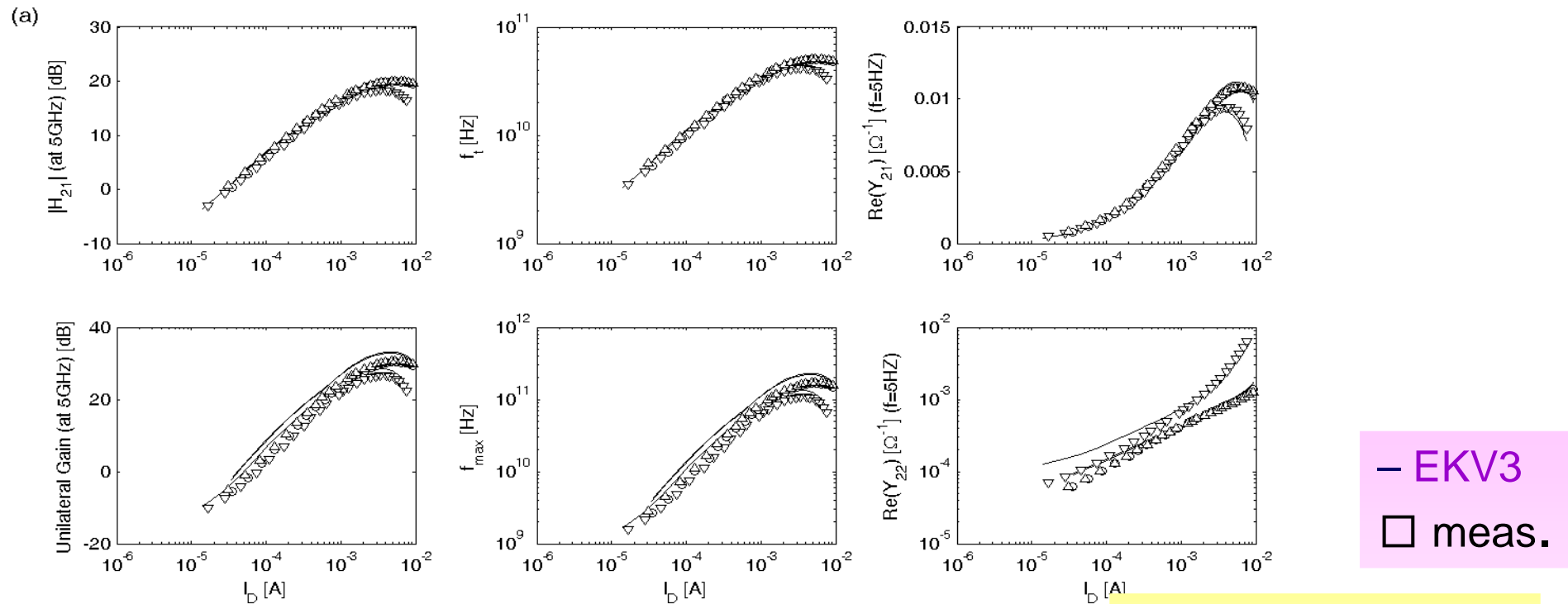
– EKV3
□ meas.

$V_{DS} = -1.2V, -V_{GS} = 0.3, 0.6, 1.2V$

- Real & Imaginary 2-port Y-parameters up to 30GHz
- $L=180\text{nm}, W_f=2\mu\text{m}, N_F=9$

A. Bazigos e.a. Physica Status Solidi C, 2008

High-frequency parameters @5GHz vs. I_D - NMOS

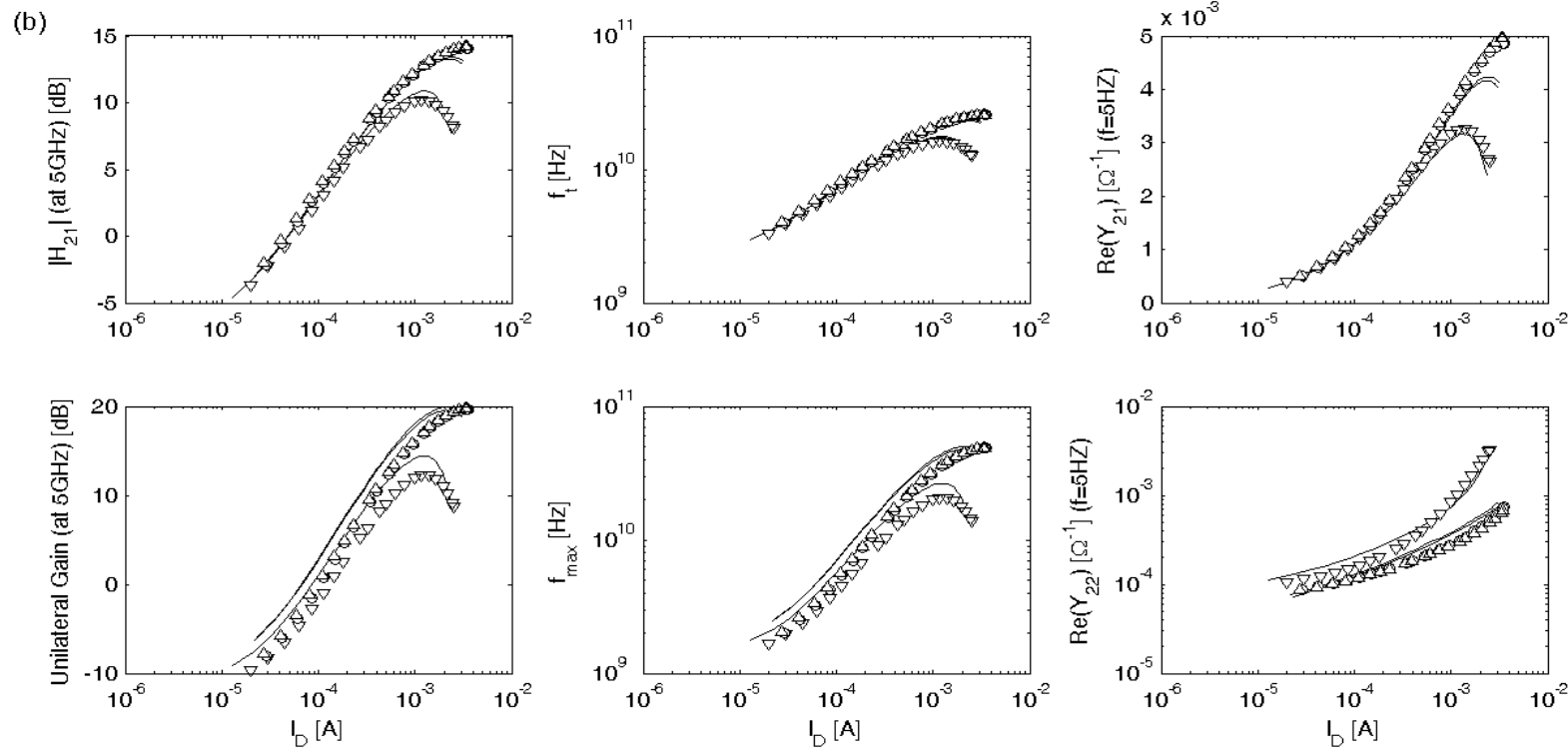


$V_{DS}=0.5, 1.2, 1.3\text{V}$

- $|H_{21}|$, U, F_T , F_{max} , $\text{Re}(Y_{21})$, $\text{Re}(Y_{22})$ vs. I_D
- $L=180\text{nm}$, $W_f=2\mu\text{m}$, $N_F=9$

A. Bazigos e.a. Physica Status Solidi C, 2008

High-frequency parameters @5GHz vs. I_D - PMOS



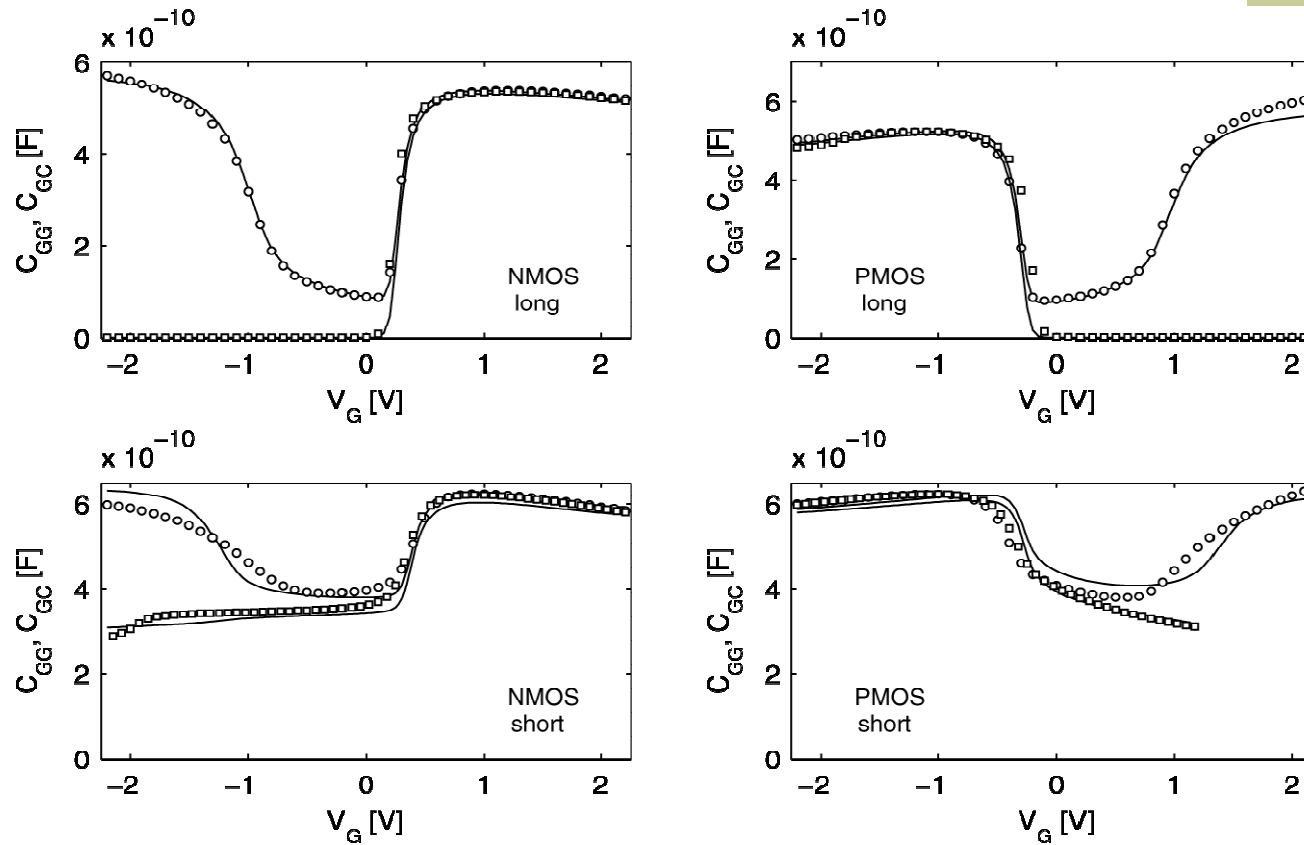
— EKV3
 □ meas.

$-V_{DS}=0.5, 1.2, 1.3V$

- $|H_{21}|, U, F_T, F_{max}, Re(Y_{21}), Re(Y_{22})$ vs. I_D
- $L=180nm, W_f=2\mu m, N_F=9$

Case II: 110 nm CMOS

Capacitance voltage characteristics

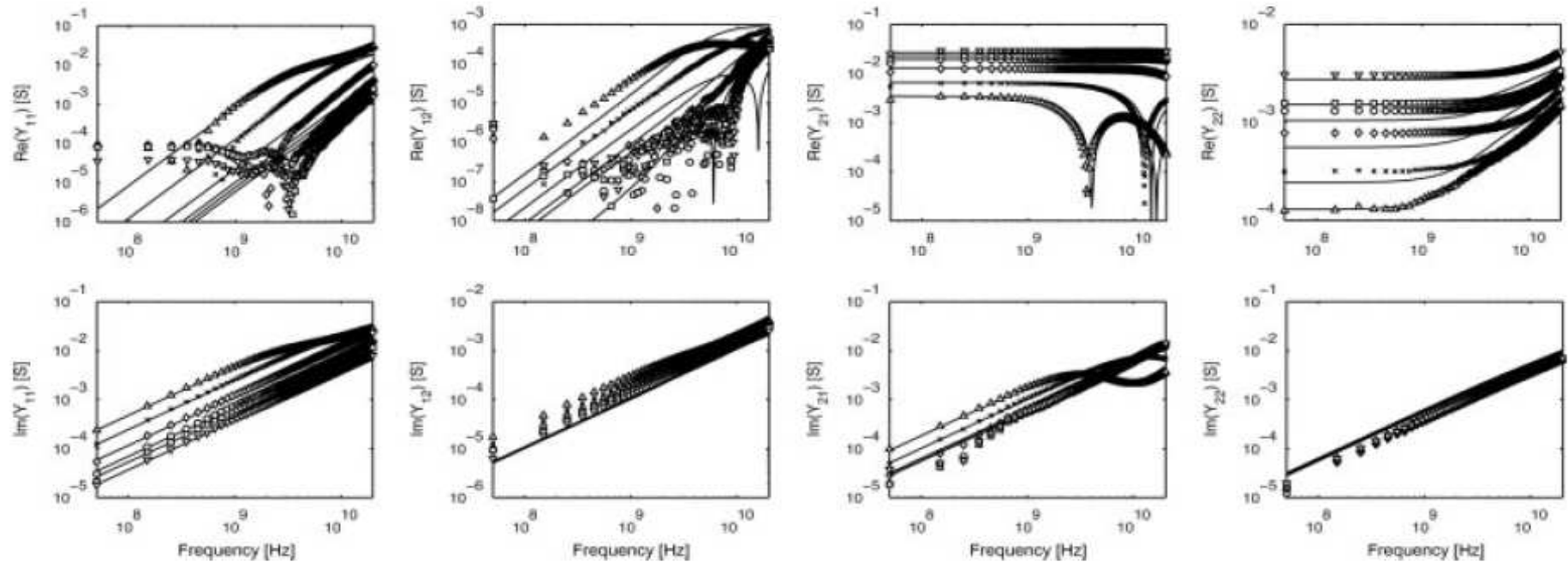


- Long/short gate and inversion capacitance

M. Bucher e.a. Int. J. RF and Microwave CAE, 2008

Case II: 110 nm CMOS

Scalability with L – NMOS



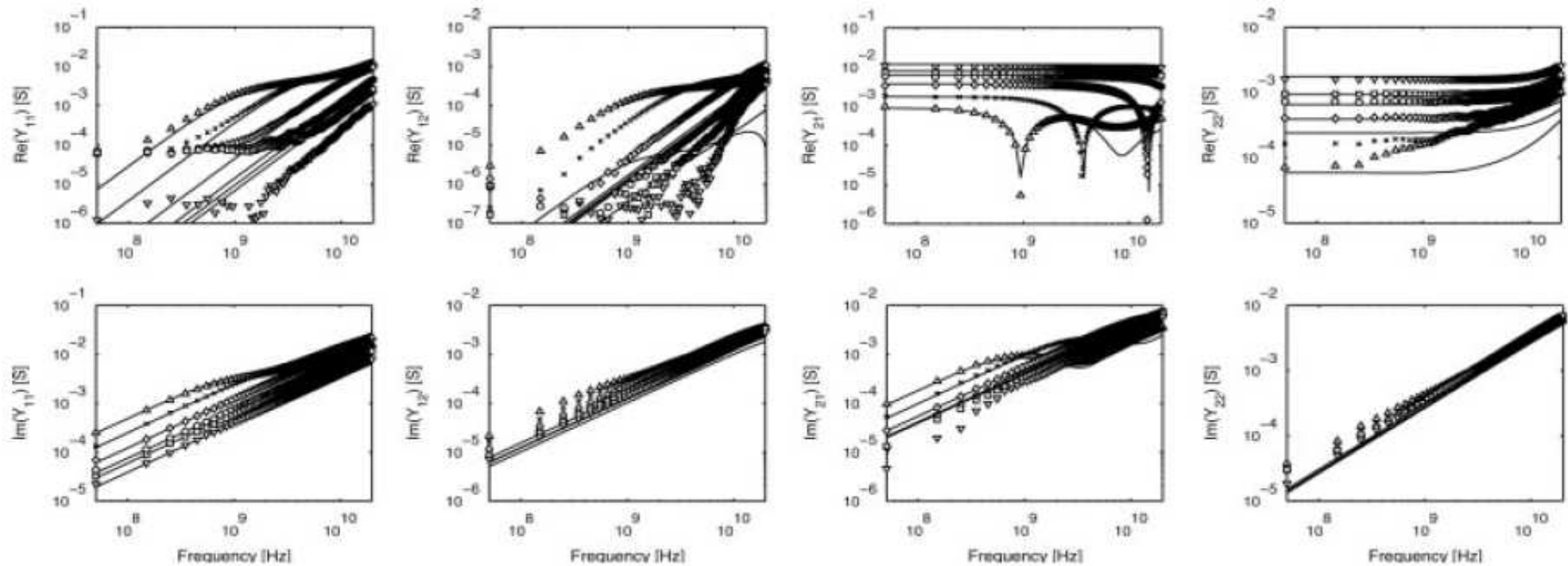
■ Y parameters for NMOS

- L=110 nm, 180 nm, 250 nm, 450 nm, 1 μ m, 2 μ m
- W=5 μ m, NF=10
- VG=0.6V, VD=0.5V

– EKV3
 □ meas.

M. Bucher e.a. Int. J. RF and Microwave CAE, 2008

Scalability with L – PMOS



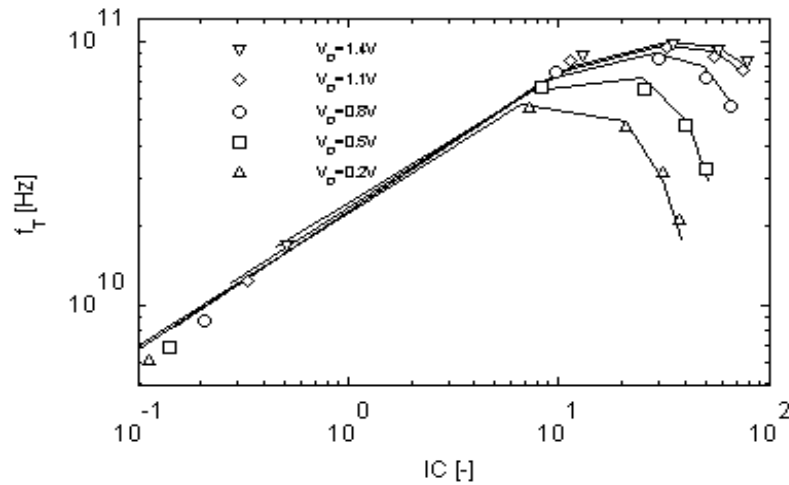
■ Y parameters for PMOS

- L=110 nm, 180 nm, 250 nm, 450 nm, 1 μ m, 2 μ m
- W=5 μ m, NF=10
- VG=0.6V, VD=0.5V

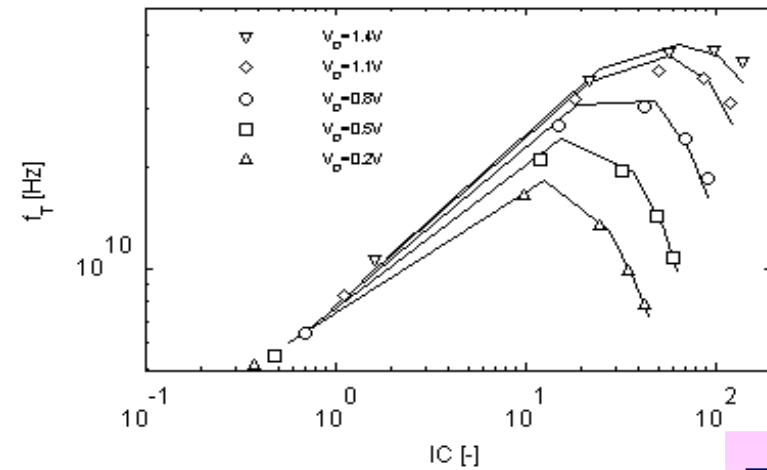
– EKV3
 □ meas.

M. Bucher e.a. Int. J. RF and Microwave CAE, 2008

Case II: 110 nm CMOS



NMOS, L = 110nm



PMOS, L = 110nm

– EKV3
□ meas.

- f_T versus IC in 110nm CMOS, EKV301.02 model

- $IC = I_D / I_{spec}$ where $I_{spec} = I_0 * W/L$

- Highest f_T is reached at $IC \sim 10-30$ (!)

- Most probable range for biasing of RF circuits for low noise is:

$1 < IC < 10$ (depending on techn

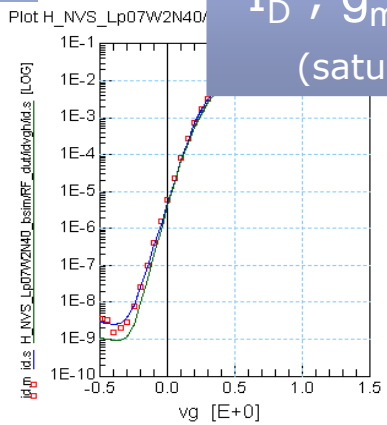
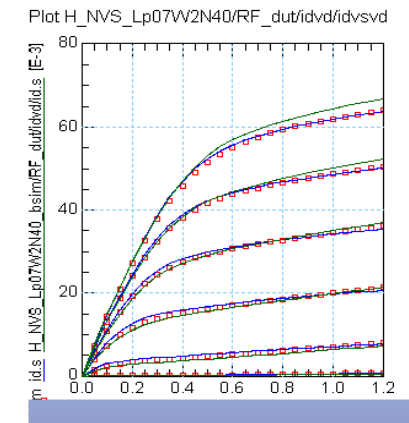
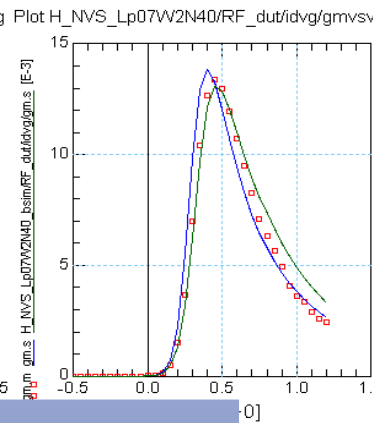
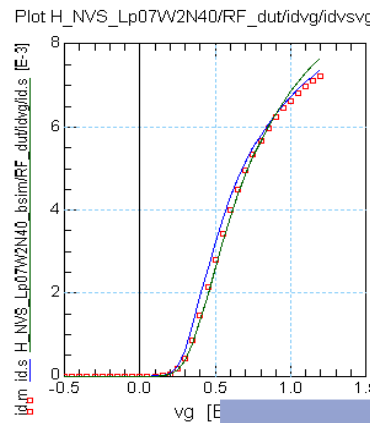
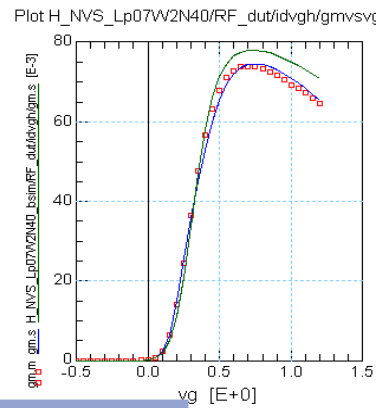
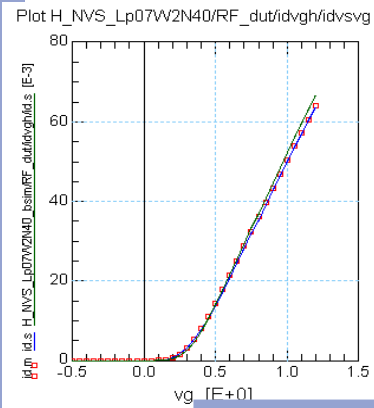
M. Bucher e.a. Int. J. RF and Microwave CAE, 2008

Case III: 90nm CMOS

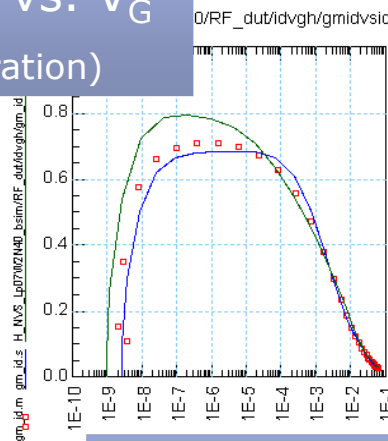
- DUTs: NMOS*, PMOS
 - nominal $L = 70 \text{ nm}$, $W = 2 \text{ } \mu\text{m}$
 - multi-finger $N_F = 40$

* *Comparison with BSIM4*

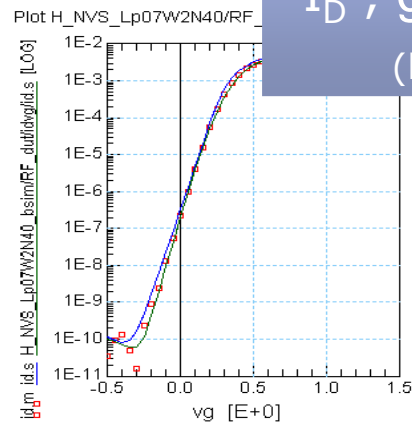
DUT: **NMOS**; $W_F = 2\mu\text{m}$; $L_F = 70\text{nm}$; $N_F = 40$
 I_D vs. V_G (linear, saturation); $V_{SB} = 0\text{V}$



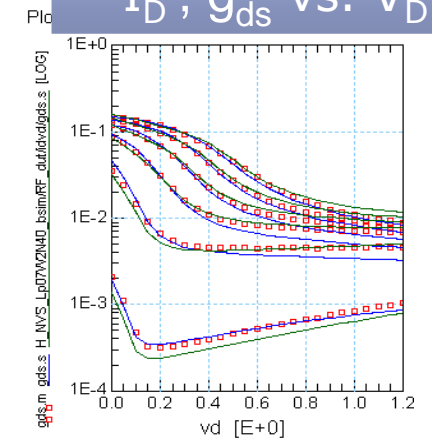
I_D, g_m vs. V_G
(saturation)



g_m/I_D vs. I_D



I_D, g_m vs. V_G
(linear)



I_D, g_{ds} vs. V_D

Measurements / EKV3 / BSIM4

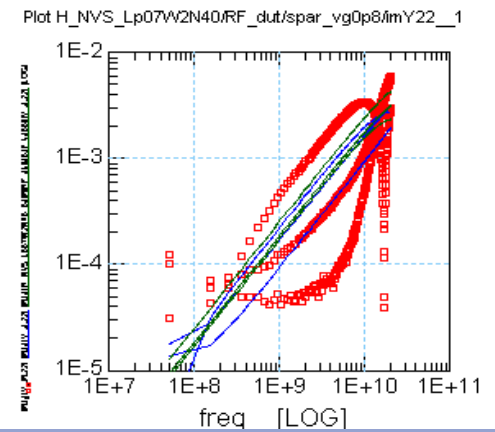
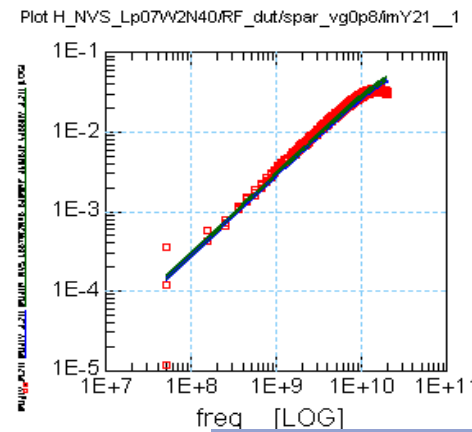
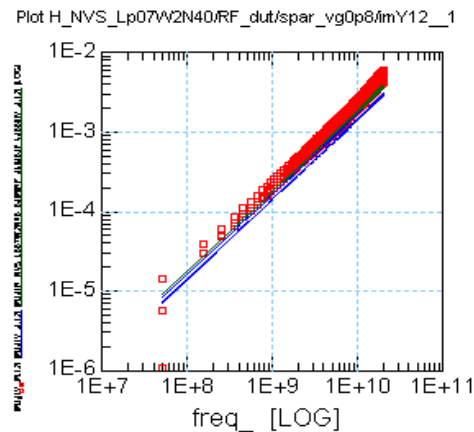
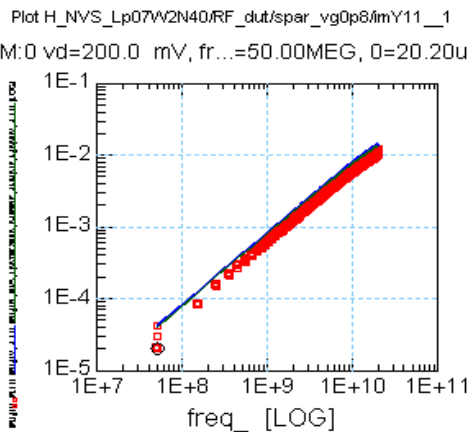
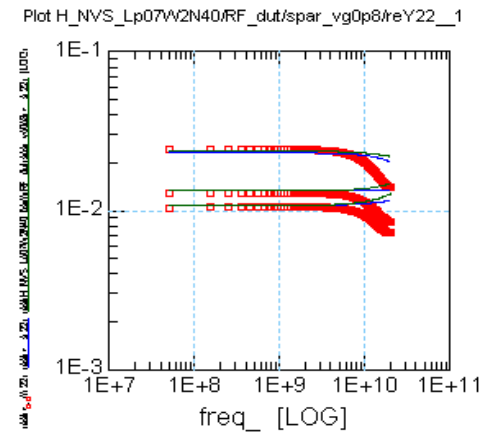
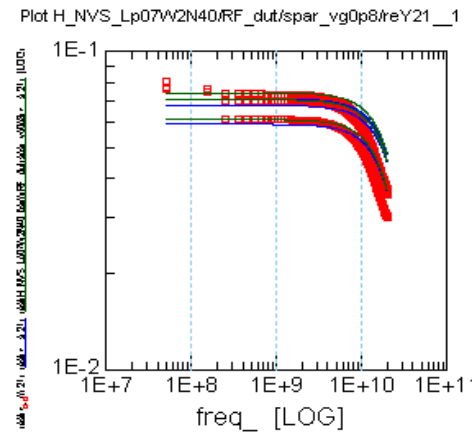
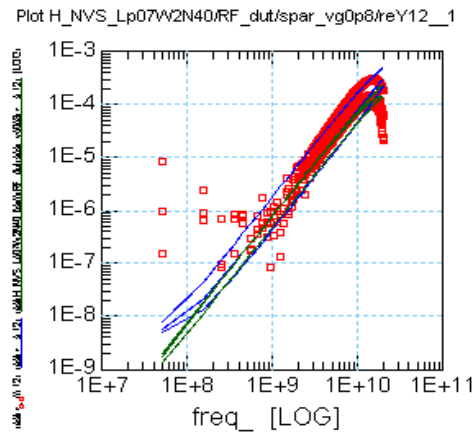
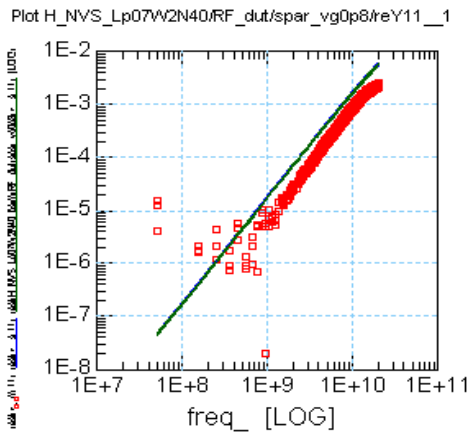
DUT: **NMOS**; $W_F = 2\mu\text{m}$; $L_F = 70\text{nm}$; $N_F = 40$
 Y-parameters; $V_{GS} = 0.8\text{V}$; $V_{DS} = \{0.4, 0.6, 0.8\}\text{V}$; $V_{SB} = 0\text{V}$

Y_{11}

Y_{12}

Y_{21}

Y_{22}



real

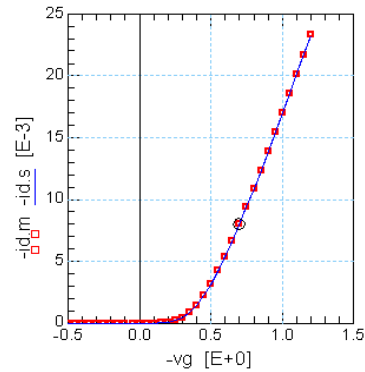
imaginary

Measurements / EKV3 / BSIM4

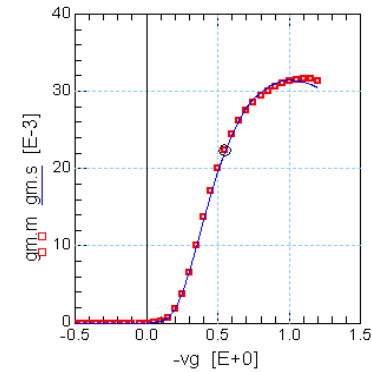
DUT: PMOS; $W_F = 2\mu\text{m}$; $L_F = 70\text{nm}$; $N_F = 40$

I_D vs. V_G (linear, saturation); $V_{SB} = 0\text{V}$

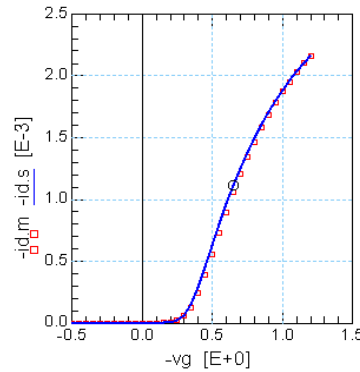
Plot H_PVS_Lp07W2N40/RF_dut/ldvgh/ldvsvg
M:24 X=700.0m, Y(0)=8.021m



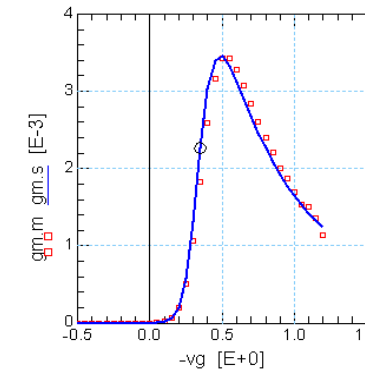
Plot H_PVS_Lp07W2N40/RF_dut/ldvgh/gmvsy
M:21 X=550.0m, gm,m=22.43m



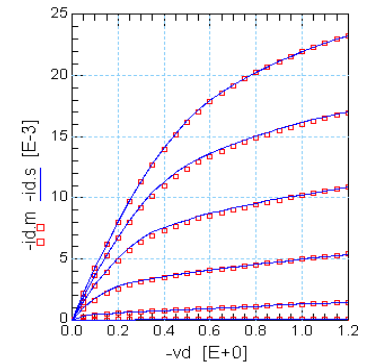
Plot H_PVS_Lp07W2N40/RF_dut/ldvgh/ldvsvg
S:23 X=650.0m, Y(1)=1.114m



Plot H_PVS_Lp07W2N40/RF_dut/ldvgh/gmvsy
S:17 X=350.0m, gm,s=2.265m

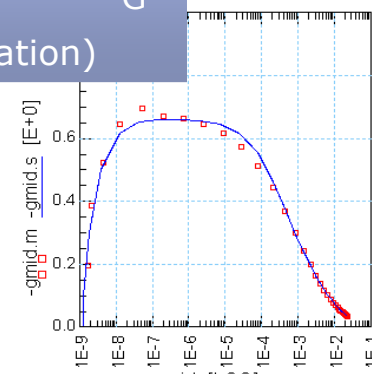
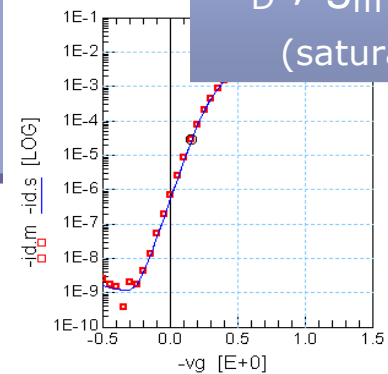


Plot H_PVS_Lp07W2N40/RF_dut/ldvd/ldvsvd



Plot H_PVS_Lp07W2N40/RF_dut/ldvgh/gmidvsic
M:13 X=150.0m, Y(0)=1.114m

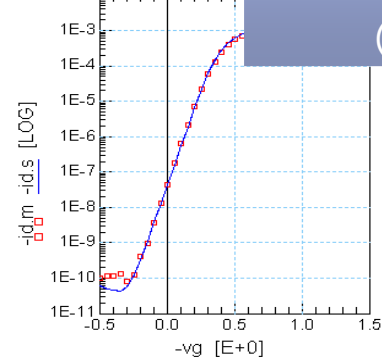
I_D, g_m vs. V_G
(saturation)



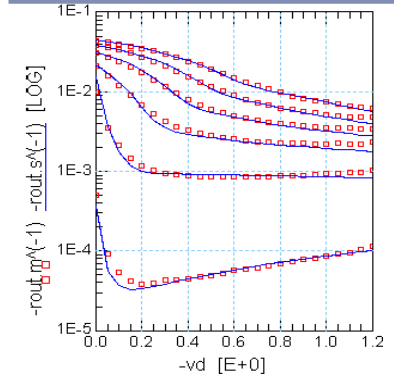
g_m/I_D vs. I_D

Plot H_PVS_Lp07W2N40/RF_dut/ldvgh/ldvsvg
M:13 X=150.0m, Y(0)=1.114m

I_D, g_m vs. V_G
(linear)



I_D, g_{ds} vs. V_D



DUT: **PMOS**; $W_F = 2\mu\text{m}$; $L_F = 70\text{nm}$; $N_F = 40$
 Y-parameters; $|V_{GS}| = 0.8\text{V}$; $|V_{DS}| = \{0.4, 0.6, 0.8\}\text{V}$; $V_{SB} = 0\text{V}$

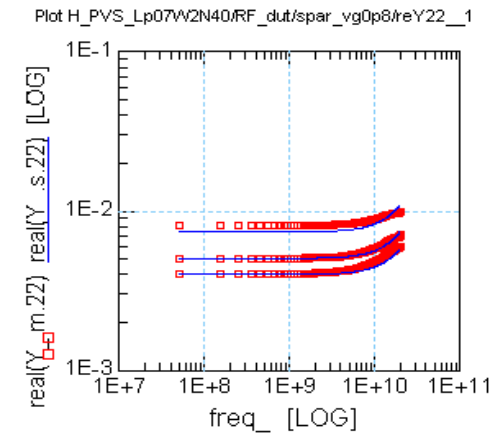
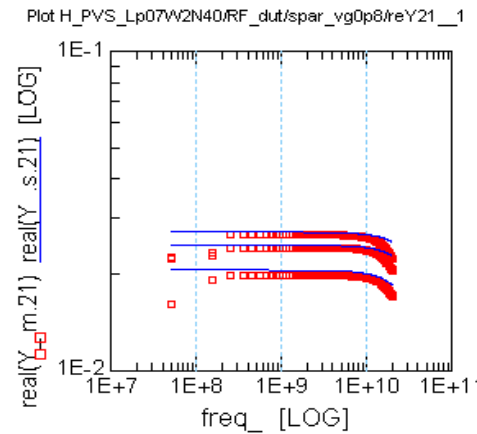
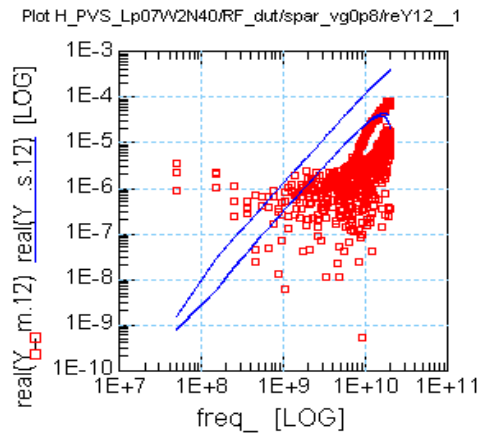
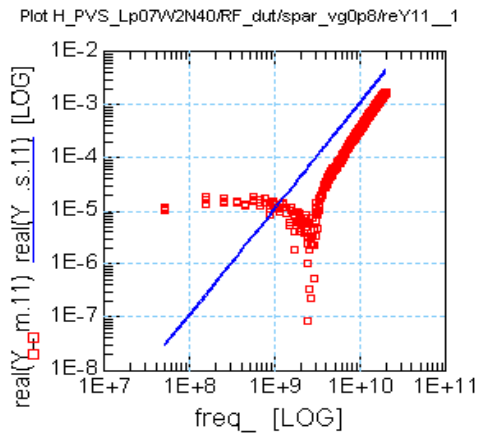
Y_{11}

Y_{12}

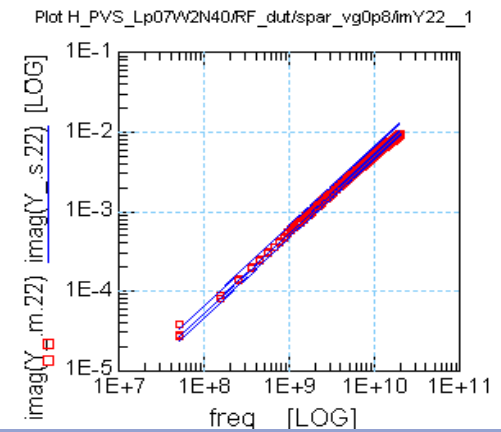
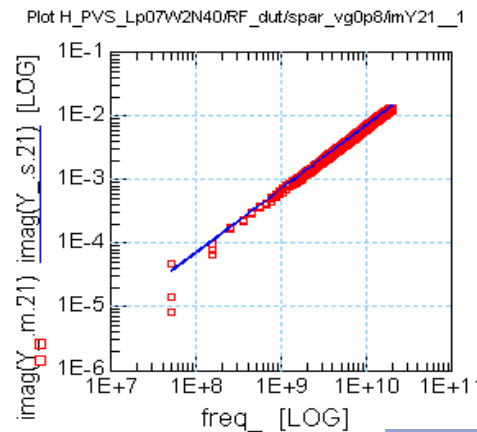
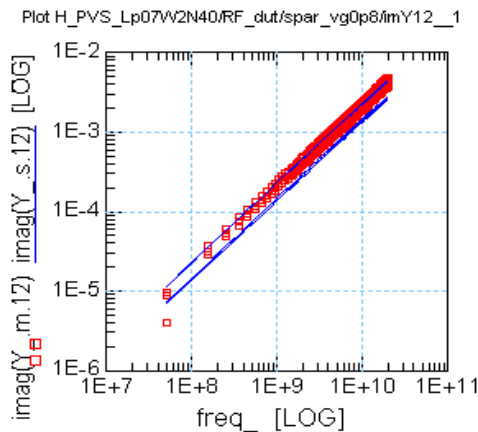
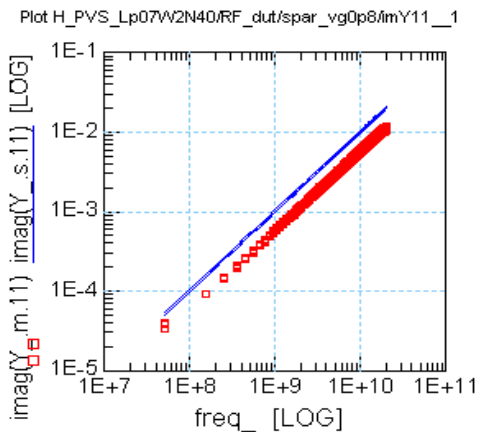
Y_{21}

Y_{22}

real



imaginary



Measurements / EKV3

Conclusions

- EKV3: analog/RF IC design-oriented, charge-based, compact model
 - Implementations in:
 - ELDO (Mentor Graphics)
 - Smash (Dolphin)
 - Spectre (Cadence).
 - Parameter extraction support (GMC Suisse & AdMOS)
- Model covers all RF aspects from DC to RF (small/large signal including NQS) and Noise.
 - Extended RF validations in 180nm, 110nm, 90nm CMOS.
 - Fully scalable with L, W, NF, bias, f, technology
 - Simple model structure & parameter extraction.
- Relation to advanced analog/RF IC design.

Acknowledgments

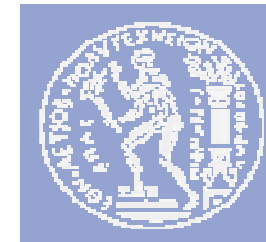
- Dr. S. Yoshitomi, TOSHIBA
- Mr. W. Kraus, ATMEL
- Prof. M. Schroter, Dr. P. Sakalas TU Dresden
- Dr. W. Grabinski & All EKV Team

TOSHIBA



Contact:

Prof. Matthias Bucher
Electronics Laboratory
Technical University of Crete
73100 Chania, Crete, Greece
phone: +30 28210 37210
fax: +30 28210 37542
[bucher`at`electronics.tuc.gr](mailto:bucher@electronics.tuc.gr)
<http://www.electronics.tuc.gr>
<http://www.rfic.tuc.gr>



References

- M. Bucher, A. Bazigos, S. Yoshitomi, N. Itoh, „A Scalable Advanced RF IC Design-Oriented MOSFET Model”, *Int. Journal of RF and Microwave Computer Aided Engineering*, Vol. 18, N°4, pp. 314-325, 2008.
- M. Bucher, A. Bazigos, “An Efficient Channel Segmentation Approach for a Large-Signal NQS MOSFET Model”, *Solid-State Electronics*, Vol. 52, N°2, pp. 275-281, February 2008 (DOI: 10.1016/j.sse.2007.08.015).
- A. Bazigos, M. Bucher, P. Sakalas, M. Schroter, W. Kraus, „High-frequency Compact Modelling of Si-RF CMOS“, accepted, *Phys. Status Solidi (c), Current Topics in Solid State Physics*.
- A. Bazigos, M. Bucher, F. Krummenacher, J.-M. Sallese, A.-S. Roy, C. Enz, "EKV3 Compact MOSFET Model Documentation, Model Version 301.01", *Technical Report*, Technical University of Crete, November 23, 2007.
- S. Yoshitomi, A. Bazigos, M. Bucher, „The EKV3 Model Parameter Extraction and Characterization of 90nm RF-CMOS Technology”, *Proc. 14th Int. Conf. on Mixed Design of Integrated Circuits and Systems (MIXDES 2007)*, pp. 74-79, Ciechocinek, Poland, June 21-23, 2007.
- C. Enz, E. Vittoz, “Charge-based MOS Transistor Modeling, The EKV model for low-power and RF IC design”, ISBN 978-0-470-85541-6, Wiley, 2006.