Compact Modelling Techniques in Thin Film SOI MOSFETs

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Goals

- Review of the main compact modeling issues in thin film SOI MOSFET modelling

- Review of the main compact modelling approaches in different types of thin film SOI MOSFET modelling

- Utilisation of models for technological and performance predictions

Outline

- Introduction
- General electrostatics
- Fully-Depleted (FD) SOI MOSFET
- Accumulation-Mode (AM) SOI MOSFETs
- Multi-Gate MOSFETs
- RF and noise modelling
- Conclusions

Introduction

- MOSFET scaling trend in near future will not be as straightforward as it has been in the past because fundamental material and process limits are imminent.

- In order to reach below the 32 nm technology node, implementation of advanced, non-classical MOSFETs with enhanced drive current and acceptable control of short channel effects are needed.

- Advanced thin-film SOI MOSFETs (e.g., single or multiple-gate MOSFETs) are very promising structures for the downscaling of MOSFETs below the 32 nm technological node.
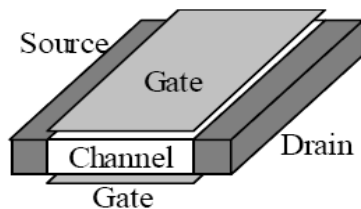
Introduction

◆ Thin film Fully Depleted SOI MOSFETs offer important advantages over Partially-Depleted SOI MOSFETs:

- Lower body factor
- Better subthreshold slope
- Reduced short-channel effects

  Higher saturation current

  Smaller mobility degradation

polysilicon gate

silicide

n+ implant

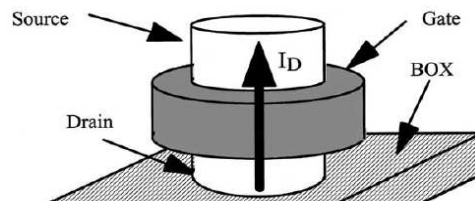buried oxide

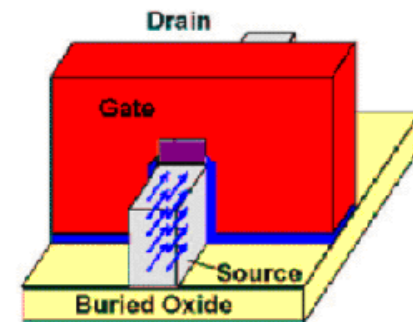depletion limit
(a)

silicon substrate

(b)
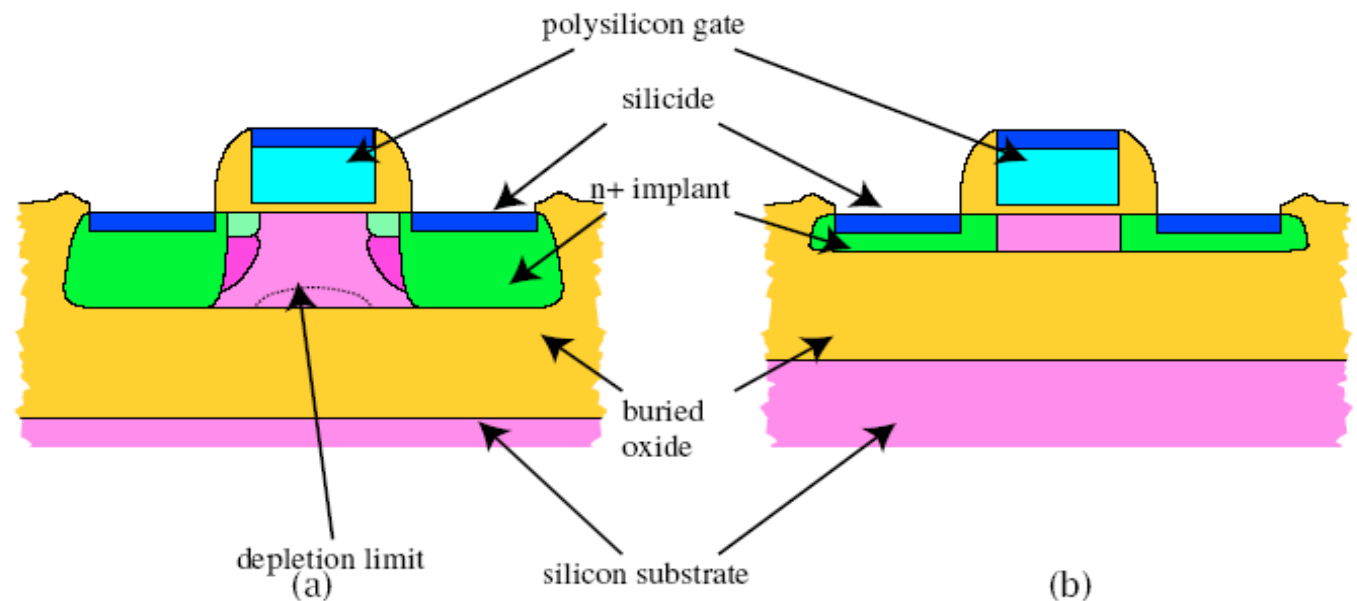
Introduction

◆ The non-classical multi-gate devices such as Double-Gate (DG) MOSFETs, FinFETs or Gate-All-Around (GAA) MOSFETs show an even stronger control of short channel effects, and increase of on-currents taking advantage of volume inversion/accumulation.

DG MOSFET

GAA MOSFET

FinFET

Introduction

♦ The availability of accurate compact models of Multiple-Gate MOSFETs in integrated circuits is critical for the future design of circuits using those devices

♦ Circuit design requires a complete small-signal model, with analytical or semi-analytical expressions of:

  ▪ Current
  ▪ Total charges
  ▪ Transconductance and conductance
  ▪ Transcapacitances

General Electrostatics

- The good electrostatic control of the channel by the gate in ultrathin body MOSFETs (full depletion in subthreshold, i.e., no punchtrough) allows to use undoped or lightly-doped Si bodies. Mobility is higher in undoped bodies than in doped ones.
- In ultrathin body MOSFETs, a proper description of the electrostatics should take into account the effects of both dopants and charge carriers.
- In FD SOI MOSFETs the Si film is fully depleted, while the front and back interface can be inverted, depleted or accumulated
    - The practical case is: front interface inverted and back interface accumulated
- In Multi-Gate MOSFETs, the Si body can be fully inverted or accumulated (volume inversion or accumulation)

General Electrostatics

♦ Generally, in single or double-gate SOI MOSFETs the electrostatic potential in the semiconductor body, $\varphi(x,y)$, is given by Poisson's equation:

$$\nabla^2 \varphi(x, y) = \frac{q}{\varepsilon_{si}}(N_a + n)$$

♦ where x and y are the direction parallel and perpendicular to the gate, respectively, and N_a is the acceptor doping density in the silicon body (n-channel device), n is the electron density and ε_{Si} is the dielectric permittivity of silicon.

General Electrostatics

- If we consider that the device is in quasi-equilibrium (which is consistent with the drift-diffusion transport mechanism), and we neglect quantum confinement, the electron density becomes:

- $n = \dfrac{n_i^2}{N_a} e^{(\varphi - \phi_F)/V_T}$ in the doped device and

- $n = n_i e^{(\varphi - \phi_F)/V_T}$ in an undoped device.

- Here, n_i is the intrinsic carrier density in silicon, V_T is the thermal voltage, and ϕ_F is the non-equilibrium quasi-Fermi level referenced to the Fermi level in the source. It satisfies the following boundary conditions:

- $\phi_F(0, y) = 0$ at the source and $\phi_F(L, y) = V_{DS}$ at the drain, where V_{DS} is the drain-source bias.

- The corresponding boundary conditions for φ are:

$$\varphi(0, y) = V_{bi} \qquad\qquad \varphi(L, y) = V_{bi} + V_{DS}$$

General Electrostatics

♦ In addition, the boundary conditions for at a given silicon-insulator interface is:

$$C_{oxi}(V_{GS} - \phi_{MS} - \varphi(x, t_i)) = \varepsilon_{Si} \left. \frac{\partial \varphi(x, y)}{\partial y} \right|_{y=t_i} \equiv Q_i$$

♦ where $C_{oxi} = \varepsilon_{ox}/t_{oxi}$ is the gate insulator capacitance per unit area, ε_{ox} and t_{oxi} are the insulator permittivity and thickness, respectively, t_{Si} is the silicon body thickness, V_{GS} is the gate-source voltage, ϕ_{MS} is the gate work function referenced to the silicon body, V_{bi} is the built-in voltage between the body and the source or drain contacts, and Q_i is the total charge sheet density (per unit area of the gate) controlled by the vertical field at the i-interface .

♦ The above equation arises from the continuity of the normal component of the displacement vector across interfaces.

General Electrostatics

- In general, multiple gates with different properties and/or gate biases, require separate boundary conditions.

- However, for a symmetrical DG MOSFET, we have the following additional boundary condition at the center plane:

$$\left.\frac{\partial \varphi}{\partial y}\right|_{y=0} = 0$$

- The same boundary condition (referred to the field in the radial direction) holds at the axis of a cylindrical GAA MOSFET

$$\left.\frac{\partial \varphi}{\partial r}\right|_{r=0} = 0$$

1D models

The first step to develop a compact model is to consider a well behaved device, with good electrostatic control by the vertical field (from the gate) and where the derivative of the lateral field in the direction of the channel length can be neglected compared to the derivative of the vertical field in the direction perpendicular to the channel.

- This is the gradual channel approximation, and simplifies the electrostatic analysis.

- This leads to neglect the short-channel effects

- In thin-film SOI MOSFETs, we expect that a long-channel device model can be applied to significantly shorter channels than in standard MOSFETs

- We also have considered an n-channel device, with acceptor doping or with no doping. The hole concentration can be neglected in the normal operation regime.

  - Of course, our analysis can easily be extended to p-channel devices

1D models: doped SOI MOSFET

◆ In a doped thin-film SOI MOSFET:

$$\frac{d^2\phi(x,y)}{dy^2} = \frac{q}{\varepsilon_{Si}}\left[N_A + n(x,y)\right] = \frac{q}{\varepsilon_{Si}}\left[N_A + \frac{n_i^2}{N_A}e^{\frac{q}{kT}[\phi(x,y)-V(x)]}\right]$$

◆ The surface electric field can be written in terms of the mobile charge density (in absolute value) per unit area at each interface, Q, and the depletion charge density per unit area (in absolute value) Q_{Dep}=q$N_A$$t_{Si}$ (t_{Si} being the Si film thickness) whatever x:

$$E_S(x) = \frac{Q(x) + \dfrac{Q_{Dep}}{2}}{\varepsilon_{Si}}$$

1D models: FD SOI MOSFET

- This 1D Poisson's solution cannot be solved analytically

- In Single-Gate FD SOI MOSFETs an analytical solution, valid for all operating regimes, is possible with the following assumptions:
  - Back interface in depletion (practical case)
  - Charge sheet approximation (the channel has an infinitesimal thickness compared to the thickness of the depleted region, i.e., the Si film)

$$Q(x) = C_{oxf}\left(V_{GF} - V_{fb} - \frac{Q_d}{2C_{oxf}} - \frac{C_{bb}}{C_{oxf}}\left(V_{GB} - V_{fbb} + \frac{Q_d}{2C_{oxf}}\right) - \alpha\varphi_s(x)\right)$$

$$C_{bb} = \frac{C_{oxb}C_b}{C_{oxb} + C_b}$$

$$\alpha = 1 + \frac{C_{oxb}C_b}{C_{oxf}(C_{oxb} + C_b)}$$

$$C_b = \frac{\varepsilon_{Si}}{t_{Si}}$$

- Linear relationship between mobile charge density and surface potential
- The charge sheet approximation may not be valid in Single-Gate UTB SOI MOSFETs, where the front channel may occupy a non-negligible portion of the Si thickness

1D models: FD SOI MOSFET

◆ No need to linearize the charge in FD SOI MOSFETs to obtain a relatively simple model

◆ Charge-based and surface-potential based models are equivalent

$$I_{DS} = \frac{W\mu}{L}\left[\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2\alpha C_{oxf}}\right]$$

◆ Expressions of total charges can be derived from this linear relationship
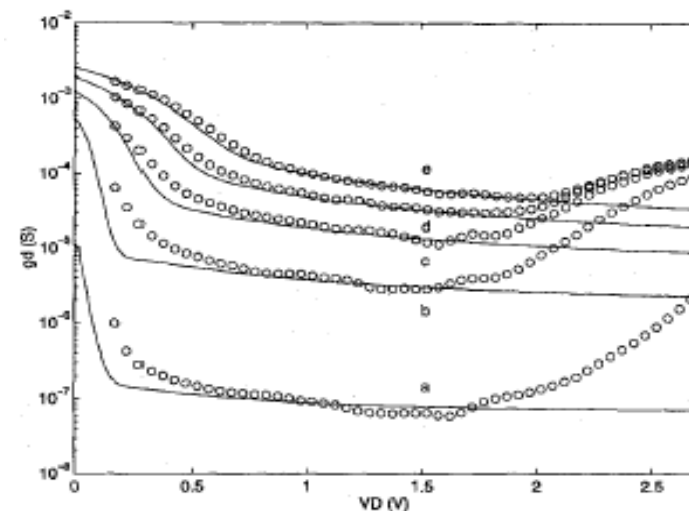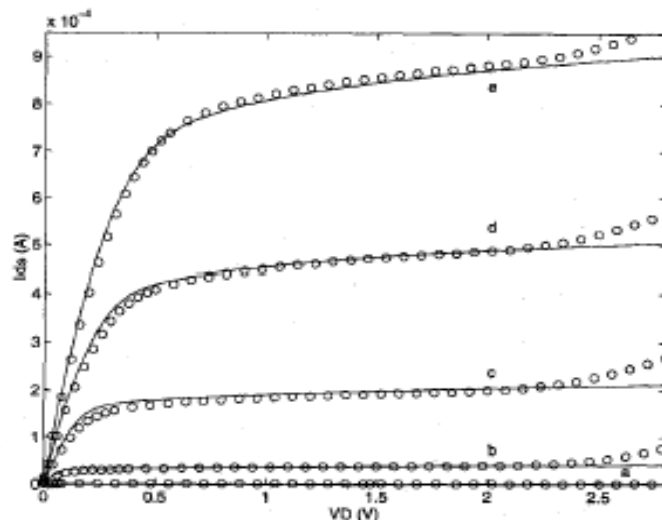
◆

Short-Channel Effects

- If the doping is high, and the mobile charge can be neglected in the subthreshold regime, a simple solution for the potential can be obtained, which leads to an analytical expression of the threshold voltage that includes the scaling dependences (and therefore the threshold voltage roll-off and DIBL):

- $$\varphi(x, y) = \varphi_1(y) + \varphi_2(x, y)$$

- In planar SOI MOSFETs, this solution is written as a superposition ,where $\varphi_1(y)$ is the solution of the 1D Poisson's equation, which includes the doping charge term, and $\varphi_2(x, y)$ is the solution of the remaining 2D Laplace equation.

- Additional approximations are needed to solve the 2D Laplace's equation

Short-Channel Effects

- In FD SOI MOSFETs the 2D Poisson's equation in subthreshold can by solved by neglecting the mobile charge density, which is much lower than the doped charge density

- An analytical expression of the threshold voltage, that takes into account the scaling dependencies, the roll-off and the DIBL can be obtained from that solution after using several approximations and a few adjustable parameters (quasi-2D model). The electrostatic short-channel effects are accounted for (in many models) by means of the threshold voltage expression, which is used in the drain current expression derived for long-channel devices

- Standard FD SOI MOSFET models take into account the short-channel effects using this approach

First explicit charge-based compact FD SOI MOSFET model

- Developed by B. **Iñiguez, D. Flandre et al (1994)**
- **It is charge-based and charge conserving**
- **Available in IsSpice (Intusoft)**

Standard Models of FD SOI MOSFETs

- ◆ BSIMSOI
- ◆ UFSOI
- ◆ HiSIM-SOI

BSIMSOI

- ◆ Developed as an extension of a bulk MOSFET model
- ◆ It extends a strong inversion explicit model by using proper interpolation functions
- ◆ It includes a smooth transition between the PD and the FD regime (Dynamically Depleted SOI MOSFET)
- ◆ Temperature dependence of threshold voltage, mobility, saturation velocity, parasitic resistance, and diode currents

- ◆ Different gate resistance options for RF simulation:
  - ■ Intrinsic input gate resistance, reflected to the gate from the intrinsic channel region. It is bias dependent and a first-order non-quasi static model, for RF and rapid transientMOSFET operations
- ◆ Last version: BSIMSOI 4.0: addresses several new issues in modeling sub-0.13 micron CMOS/SOI high-speed and RF circuit simulation.

BSIMSOI

- ◆ Improvements of BSIM 4.0:
- ◆ Asymmetric current/capacitance model S/D diode and asymmetric S/D resistance;
- ◆ Improved GIDL model with BSIM4 GIDL compatibility
- ◆ Noise model Improvements;
  - ▪ Improved width/length dependence on flicker noise
  - ▪ SPICE2 thermal noise model is introduced as TNOIMOD=2 with parameter NTNOI that adjusts the magnitude of the noise density
  - ▪ Body contact resistance induced thermal noise
  - ▪ Thermal noise induced by the body resistance network
  - ▪ Shot noises induced by Ibs and Ibd separated
- ◆ A two resistance body resistance network introduced for RF simulation;
- ◆ Threshold voltage model enhancement;
  - ▪ Long channel DIBL effect model added
  - ▪ Channel-length dependence of body effect improved
- ◆ Drain induced threshold shift(DITS) model introduced in output conductance;
- ◆ Improved model accuracy in moderate inversion region with BSIM4 compatible Vgsteff;

FD/SOI UFSOI

- The University of Florida developed one model for PD SOI MOSFETs (UFPDB) and one model for FD SOI MOSFETS (FD/SOI UFSOI)
- It is charge-based, and considers 5 terminals
- It is strongly physically-based, and needs iterations
- The model accounts for the charge coupling between the front and back gates
- It includes a two-dimensional analysis of the electrostatic potential in the SOI film and underlying BOX for subthreshold-region operation.
- The model assumes that the film is strongly FD, except in and near the accumulation region where it accounts for the majority-carrier charge, and hence dynamic floating-body effects.
- Two dimensional analysis for weak-inversion current
- Spline interpolations of current and charge across a physically defined, bias-dependent moderate-inversion region linking the weak- and strong-inversion formalisms

FD/SOI UFSOI

- ◆ **Temperature dependence is also implemented, without the need for any additional parameters**
- ◆ **Physics-based noise modeling for AC simulation, which accounts for thermal noise from the channel and parasitic series rresistances, shot noise at the source and drain junctions, and flicker noise in the channel.**
- ◆ **The temperature-dependence modeling is the basis for a self-heating option, which uses special iterate control for the local device temperature node.**
- ◆ **Because of the process basis of the models, parameter evaluation can be based in part on device structure**
- ◆ **Option for a strained Si/SiGe channel.**

HiSIM SOI

- Based on a complete surface-potential description.
- The surface potential in the MOSFET channel, and the potentials at both surfaces of the buried oxide
- This allows to include all relevant device features of the SOI-MOSFET
- An additional parasitic electric field, induced by the surface-potential distribution at the buried oxide, has to be included for accurate modeling of the short-channel effects.
- It seems to have better convergence properties than BSIMSOI and UFSOI
- It includes a 1/f noise model

AM SOI MOSFET modelling

◆ In thin-film SOI CMOS circuits, nMOS devices are FD SOI MOSFETs, but pMOS devices can be AM SOI MOSFETs

◆ Different operating regimes have to be considered in AM SOI MOSFETs: subthreshold (full depletion), above threshold conduction in the quasi-neutral region, and surface accumulation
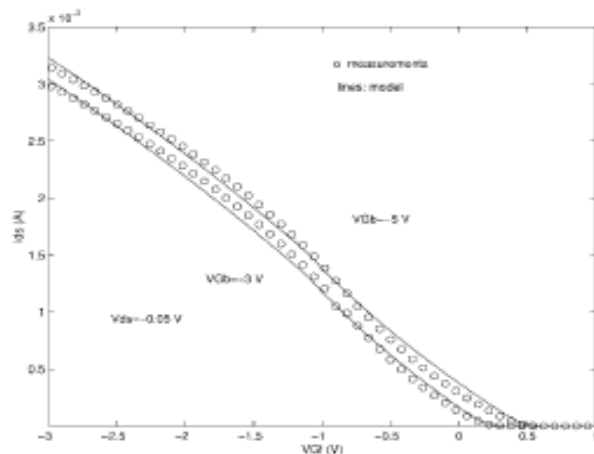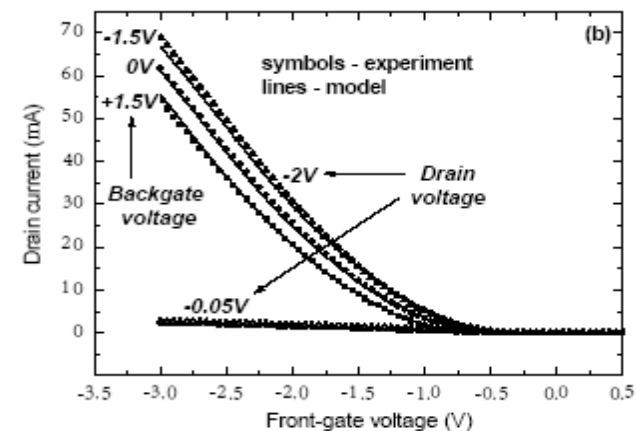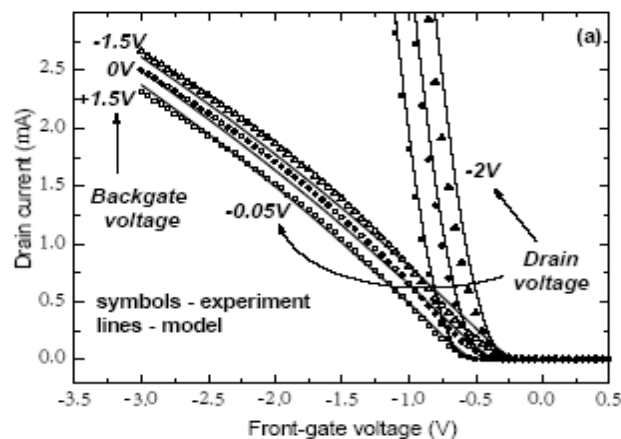
AM SOI MOSFET modelling

Case 4
thin film current   accumulated current

Case 5

Case 6

Case 7

AM SOI MOSFET modelling

- The first compact models for AM SOI MOSFETs were developed by K. W. Su and J. B. Kuo (DC model, 1997) and B. Iñiguez et al (charge-based model, 1999).

- No model is available in commercial circuit simulators.

- AM SOI MOS modeling is more complex than FD SOI MOS modeling. A square root dependent depletion region width, changing along the channel, must be considered, as well as an equation relating the accumulation charge sheet density with the surface potential.

- J. B. Kuo et al linearized later the square root.

AM SOI MOSFET modelling

♦ In very thin **AM SOI MOSFETs** surface accumulation takes place with full film depletion

♦ The resulting model has the same form as a FD SOI MOSFET model

Multi-Gate MOSFET modelling

- No models currently available in circuit simulators.
- They face important challenges for nanoscale devices: scaling with volume inversion/accumulation, quantum confinement, hydrodinamic transport
- Models under development:
    - BSIM-MG (based on BSIMSOI)
    - UFDG (extension of FD/SOU UFSOI)
        - Applicable to symmetrical DG, assymmetrical DG MOSFETs, UTB SOI MOSFETs and FinFETs
        - It considers quantum confinement self consistently (**Compact Poisson-Schrödinger Solver**)
        - It accounts for velocity overshoot
        - **The carrier transport and channel current are modeled as quasi-ballistic via an accounting for velocity overshoot, derived from the Boltzmann transport equation and its moments, and a QM-based characterization of mobility**

1D models: doped DG MOSFET

◆ By integrating the Poisson´s equation between the centre (y=0) and the top surface of the film (y=-t$_{si}$/2) we get:

$$E_S(x) = \sqrt{\frac{2qN_A}{\varepsilon_{Si}}} \sqrt{(\phi_s - \phi_0) + \frac{kT}{q}\frac{n_i^2}{N_A^2}e^{\frac{q}{kT}[\phi_s - V(x)]}\left(1 - e^{-\frac{q}{kT}(\phi_s - \phi_0)}\right)}$$

◆ where $\phi_S = \phi(x, -t_{Si}/2)$ is the surface potential and $\phi_o = \phi(x,0)$ is the potential in the middle of the film.

◆ Unfortunately, the potential at the center is unknown and we cannot analytically integrated for the potential.

◆ An analytical model is possible with an approximate expression of the difference between the two potentials:

  ■ The constant value obtained in the subthreshold/depletion region to well above threshold [Francis 94, Moldovan 07]; this is valid up to well above threshold.

  ■ An empirical expression that, using adjustable parameters, fits the entire range of operation [Cerdeira 08]

1D models: undoped DG MOSFET

♦ For undoped DG MOSFETs, Poisson's equation is:

$$\frac{d^2\psi(x)}{dx^2} = \frac{d^2(\psi(x)-V)}{dx^2} = \frac{q}{\varepsilon_{Si}} \cdot n_i \cdot e^{\frac{q(\psi(x)-V)}{kT}}$$

♦ By solving Poisson's equation with the appropriate boundary conditions [Taur 04]:

$$\psi(r) = V - \frac{2kT}{q}\log\left(\frac{t_{Si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{Si}kT}}\cos\left(\frac{2\beta x}{t_{Si}}\right)\right)$$

   ▪ Where β is a constant obtained from the boundary conditions

♦ The following relation is obtained:

$$\frac{q(V_{GS}-\Delta\varphi-V)}{2kT} - \log\left(\frac{2}{t_{Si}}\sqrt{\frac{2\varepsilon_{Si}kT}{q^2 n_i}}\right) = \log(\beta) - \log[\cos(\beta)] + \frac{2\varepsilon_{Si}t_{ox}}{\varepsilon_{ox}t_{Si}}\beta\tan(\beta)$$

   ▪ where $\Delta\varphi$ is the work function difference between the gate electrode and the intrinsic silicon

1D models: undoped DG MOSFET

- The drain current is obtained as:

$$I_{DS} = \frac{W\mu}{L} \int_0^{V_{DS}} Q(V)\,dV$$

- From Gauss'law

$$Q = 2\varepsilon_{Si} \left.\frac{d\psi}{dy}\right|_{y=t_{Si}/2} = 2\varepsilon_{Si}\frac{2kT}{q}\frac{2\beta}{t_{Si}}\tan(\beta)$$

- The following expression of the drain current is obtained [Taur 04]:

$$I_D = \frac{W}{L}\frac{4\varepsilon_{Si}}{t_{Si}}\left(\frac{2kT}{q}\right)^2\left[\beta\tan(\beta) - \frac{\beta^2}{2} + \frac{\varepsilon_{Si}t_{ox}}{\varepsilon_{ox}t_{Si}}\beta^2\tan^2(\beta)\right]_{\beta_d}^{\beta_s}$$

- Shortcoming: I_D cannot be written in a charge-based form

1D models: undoped DG MOSFET

However, the a unified charge control model can be obtained by making a few approximations [Sallese]:

$$(Vgs - \Delta\varphi - \mathrm{V}) + \frac{kT}{q}\log\left(\frac{qn_i t_{Si}}{8C_{ox}\frac{kT}{q}}\right) - \frac{kT}{q}\log\left(\frac{C_{ox}}{C_{Si}}\right) = \frac{Q}{2C_{ox}} + \frac{kT}{q}\left(\log\left(\frac{Q}{8C_{ox}\frac{kT}{q}}\right) + \log\left(\frac{C_{Si}}{C_{ox}} + \frac{Q}{8C_{ox}\frac{kT}{q}}\right)\right)$$

- where C_{Si} is the silicon capacitance and C_{ox} is the oxide capacitance.

◆　　 The same type of charge control model was obtained in doped DG MOSFETs, with the needed approximations

1D models: undoped DG MOSFET

♦ The drain current is obtained as:

$$I_{DS} = \frac{W\mu}{L} \int_0^{V_{DS}} Q(V)\,dV$$

♦ From the charge control model:

$$dV = -\frac{dQ}{2C_{ox}} - \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+2Q_0}\right)$$

♦ Where

$$Q_0 = 4\frac{kT}{q}C_{Si}$$

♦ Finally we get the expression:

$$I_{DS} = \frac{W\mu}{L}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{Si}\log\left[\frac{Q_d + 2Q_0}{Q_s + 2Q_0}\right]\right]$$

1D models: Cylindrical GAA MOSFET

- In a well-behaved cylindrical GAA MOSFET, the electrostatic behaviour of the device is described by the 1D Poisson's equation in the radial direction.

- In an undoped cylindrical n-type SGT-MOSFET Poisson's equation takes the following form (in cylindrical coordinates):

$$\frac{d^2\psi}{dr^2} + \frac{1}{r}\frac{d\psi}{dr} = \frac{kT}{q}\,\delta \cdot e^{\frac{q(\psi - V)}{kT}}$$

- where $\delta = q^2 n_i / kT\varepsilon_{Si}$, $\psi(r)$ the electrostatic potential and V the electron quasi-Fermi potential.

- Boundary conditions:

$$\frac{d\psi}{dr}(r = 0) = 0, \qquad \psi(r = R) = \psi_s$$

Exact solution:

$$\psi(r) = V + \frac{kT}{q}\log\left(\frac{-8B}{\delta(1 + Br^2)^2}\right)$$

B determined from boundary conditions

1D models: Cylindrical GAA MOSFET

- From Gauss law:

$$C_{ox}(V_{GS} - \Delta\varphi - \psi_s) = Q = \varepsilon_{Si}\left.\frac{d\psi}{dr}\right|_{r=R} \quad (4)$$

- Using $\left.\dfrac{d\psi}{dr}\right|_{r=R} = -\dfrac{kT}{q}\dfrac{4BR}{1+BR^2}$, the charge control model that is obtained is:

$$(V_{GS} - \Delta\varphi - V) - \frac{kT}{q}\log\left(\frac{8}{\delta R^2}\right) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

- where

$$Q_0 = \frac{4\varepsilon_{Si}}{R}\frac{kT}{q}$$

- The drain current is calculated from:

$$I_{DS} = \mu\frac{2\pi R}{L}\int_0^{V_{DS}} Q(V)dV$$

- Using $dV = -\dfrac{dQ}{C_{ox}} + \dfrac{kT}{q}\left(\dfrac{dQ}{Q} + \dfrac{dQ}{Q+Q_0}\right)$ we obtain:

$$I_{ds} = \frac{2\pi R}{L}\mu\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kT}{q}Q_0\log\left[\frac{Q_d + Q_0}{Q_s + Q_0}\right]\right]$$

1D models: DG MOSFET

Transfer characteristics, for V_{DS}=0.05V (a) and for V_{DS}=1V (b) in linear scale and in logarithmic scale Solid line: Atlas simulation; Symbol line: our compact model
doping level N_A=6.10^{17} cm^{-3}; silicon thickness t_{Si}=31nm; oxide thickness t_{ox}=2nm; channel length L=1μm and width W=1μm.

1D models: Cylindrical GAA MOSFET

Output and transfer characteristics obtained from the analytical model (solid lines) compared with numerical simulations from DESSIS-ISE® (symbols).

1D models: FinFET

In general, in symmetric Multi-Gate MOSFETs

$$\left(V_{GS} - V_0 - V\right) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q + Q_0}{Q_0}\right)$$

Charge associated to top, lateral and total charge calculated with ATLAS 3-D simulations and with the unified charge control model (FinFET with W_{fin}=10 nm, H_{fin}=50 nm)

1D models: Independently-Biased DG MOSFET

◆ A similar unified charge control model is obtained assuming the back interface in weak inversion, but without assuming the charge sheet approximation:

$$\frac{1}{1+\alpha}V_{GS} + \frac{\alpha}{1+\alpha}V_{GB} - V - \frac{1}{1+\alpha}v_{fb1} - \frac{\alpha}{1+\alpha}v_{fb2} - \frac{kT}{q}\log\left[\frac{1}{2}\cdot\left(\frac{4C_{Si}\left(V_{GS} - V_{GB} + v_{fb2} - v_{fb1}\right)}{C_{ox}\frac{kT}{q}}\right)^2\right] -$$

$$- \frac{kT}{q}\log\left(\frac{1-\alpha}{1+\alpha}\right) + \frac{kT}{q}\log(2a^2) = \frac{Q}{C_{ox}(1+\alpha)} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{2Q}{Q_0} + 1\right)$$

◆ **Where**
$$\alpha = \frac{C_{Si}}{C_{Si} + C_{ox}}$$
$$C_{Si} = \frac{\varepsilon_{ox}}{t_{Si}}$$
$$Q_0 = 4C_{Si}\left(V_{GS} + v_{fb2} - v_{fb1}\right)$$
$$a = \frac{\varepsilon_{Si}}{\varepsilon_{ox}}\frac{t_{ox}}{L_D}$$
$$L_D = \sqrt{\frac{kT\varepsilon_{Si}}{q^2 n_i}}$$

1D models: Independently-Biased DG MOSFET

channel length L=1μm, width W=1 μm, silicon oxide thickness t_{ox}=2 nm and silicon film thickness t_{Si}=31 nm .

2D models Multi-Gate MOSFETs

- If the doping is high, and the mobile charge can be neglected in the subthreshold regime, a simple solution for the potential can be obtained, which leads to an analytical expression of the threshold voltage that includes the scaling dependences (and therefore the threshold voltage roll-off and DIBL):

  $$\varphi(x, y) = \varphi_1(y) + \varphi_2(x, y)$$

- In DG SOI MOSFETs, this solution is written as a superposition ,where $\varphi_1(y)$ is the solution of the 1D Poisson's equation, which includes the doping charge term, and $\varphi_2(x, y)$ is the solution of the remaining 2D Laplace equation.

- In GAA MOSFETs, the solution is written as:

  $$\varphi(x, r) = \varphi_1(r) + \varphi_2(x, r)$$

- Additional approximations are needed to solve the 2D Laplace's equation

2D models

- An analytical expression of the threshold voltage, that takes into account the scaling dependencies, the roll-off and the DIBL can be obtained from that solution after using several approximations and a few adjustable parameters (quasi-2D model). The electrostatic short-channel effects are accounted for (in many models) by means of the threshold voltage expression, which is used in the drain current expression

- More rigorous solutions (fully 2D or 3D models, or "predictive models"):

  - Truncation of series of hyperbolic functions (DG MOSFETs, FinFETs), or Bessel functions (GAA MOSFETs)
  - **Conformal mapping**

2D models (series truncation method): DG MOSFET

Subthreshold Swing

$$Swing = \frac{V_t}{1 - S_{gs}} \cdot \ln(10)$$

with t_{ox}=2nm. **V_{DS}=10 mV**.

Threshold Voltage Model

The threshold voltage is defined as the value of the gate voltage to obtain a certain value of the mobile sheet charge density at the position of the potential minimum (virtual cathode)

$$Q_{inv} = 2 \int_0^{t_0} n_i \, e^{\phi[x_{min}, y]/V_T} \, dy$$

$$V_{TH} = \phi_{ms} + \frac{1}{1 - S_{gs}} \cdot \left(V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot t_o}\right) - S_{ds} \right)$$

For Long Channel DG MOSFET

$$V_{TH} = \phi_{ms} + V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot t_o}\right)$$

2D models (series truncation method): DG MOSFET

Threshold Voltage Roll-off, and DIBL Models

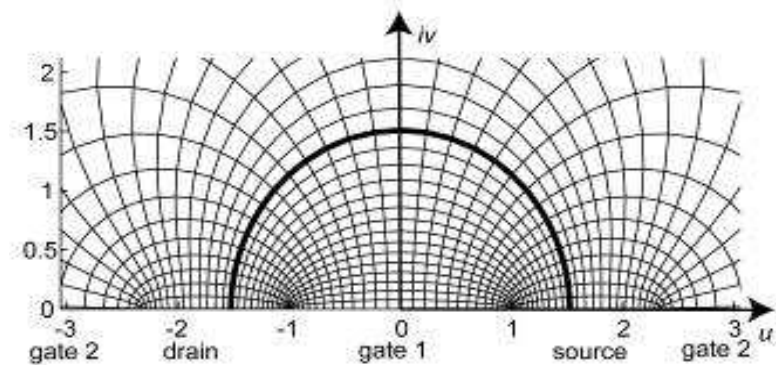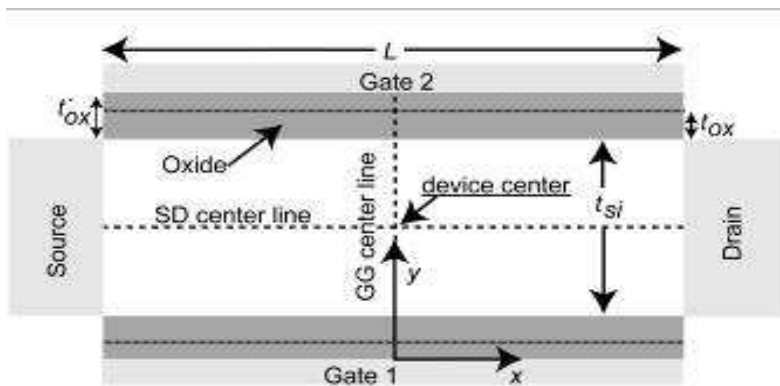$$\Delta V_{TH} = V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot t_o}\right)\left[1 - \frac{1}{1 - S_{gs}}\right] - S_{ds}$$

$$DIBL = \left\{ V_T \ln\left(\frac{Q_{TH}}{2n_i \cdot t_o}\right)\left[\frac{1}{1 - S_{gso}} - \frac{1}{1 - S_{gs}}\right] - \left[\frac{S_{dso}}{1 - S_{gso}} - \frac{S_{ds}}{1 - S_{gso}}\right] \right\}$$
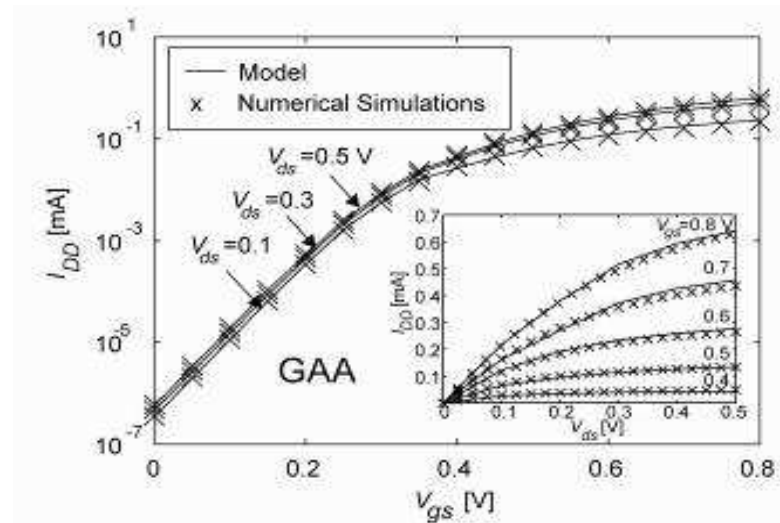

S_{gso} and S_{dso} are the values of S_{gs} and S_{ds} at low V_{DS}
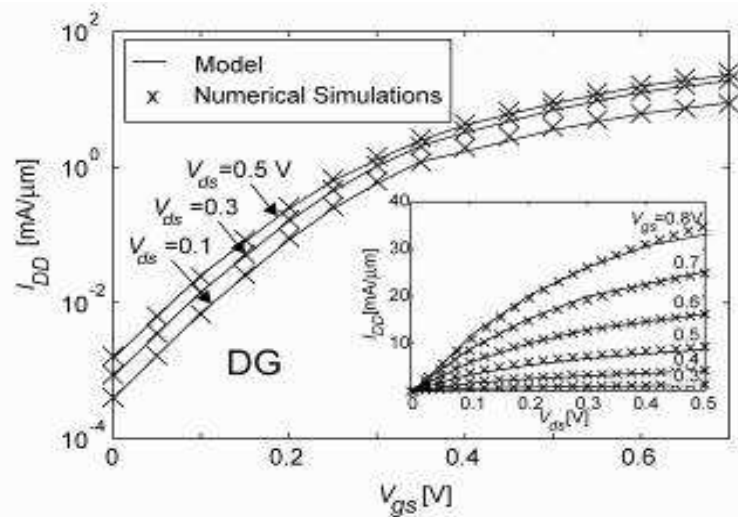
2D/3D models (conformal mapping technique)

Schematic view of the DG MOSFET cross-section (a).
The extended body maps into the upper half-plane of the (u, iv)
plane (b), where the u-axis, the iv-axis, and the bold semicircle
with radius $1/\sqrt{k}$ represent the boundary, the G-G and the S-D
symmetry axis, respectively. The four corners of the boundary are
located at $u = \pm 1$ and $\pm 1/k$.

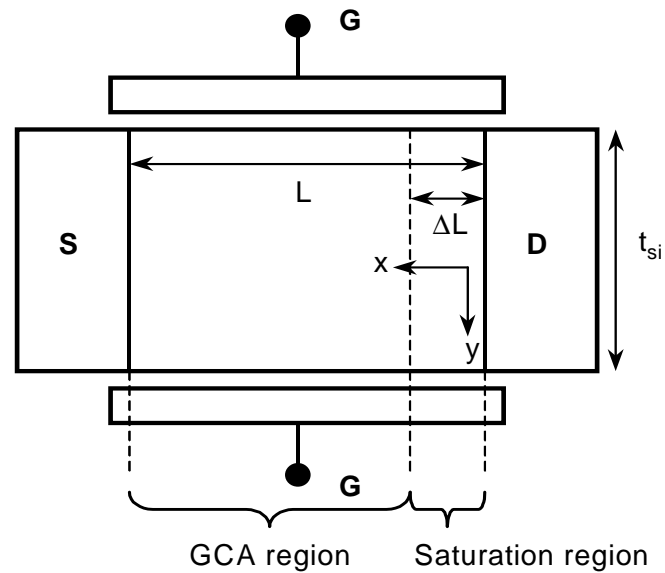# 2D/3D models (conformal mapping technique)

2D/3D potential model in subthreshold derived using conformal mapping

1D potential model well above threshold (kernel model)

4th order polynomial expression of the potential in the transition regime, imposing continuity everywhere

2D models: Analysis of the saturated region in DG MOSFETs

2D models: Analysis of the saturated region in DG MOSFETs

♦ Poisson's equation is solved in the saturated region:

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = -\frac{-q\, n_e(x,y)}{\varepsilon_{si}}$$

$$\left. \frac{d\phi}{dy} \right|_{y=tsi/2} = 0 \qquad \qquad \varepsilon_{si} \left. \frac{d\phi}{dy} \right|_{y=0} = \varepsilon_{ox} \frac{\phi_S - V_{gs} + \Delta\varphi}{t_{ox}}$$

♦ we chose a power law as an approximation for the potential profile along y

$$\phi(x,y) = a + b(x)y + c(x)y^n$$

2D models: Analysis of the saturated region in DG MOSFETs

$$\phi(x,y) = \phi_S + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_S - V_{gs} + V_{FB}}{t_{ox}} y - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_S - V_{gs} + V_{FB}}{n \cdot t_{ox}} \left(\frac{2}{t_{si}}\right)^{n-1} y^n \qquad \text{for} \qquad y \le t_{si}/2$$

$$\phi(x,y) = \phi_S + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_S - V_{gs} + \Delta\varphi}{t_{ox}} (t_{si} - y) - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_S - V_{gs} + \Delta\varphi}{n \cdot t_{ox}} \left(\frac{2}{t_{si}}\right)^{n-1} (t_{si} - y)^n \qquad \text{for} \qquad y > t_{si}/2$$

Integrating:
$$\int_0^{tsi} \frac{\partial^2 \phi}{\partial x^2} \, dy = -\frac{Q_m}{\varepsilon_{si}} + 2\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_S - V_{gs} + V_{FB}}{t_{ox}}$$

Q_m is considered constant in the saturated region

We have to solve in the x-direction:

$$\frac{\partial^2 \varphi}{\partial x^2} - \frac{\varphi}{\lambda^2} = 0$$

$$\varphi = \phi_S - V_{gs} + \Delta\varphi - \frac{Q_m}{2C_{ox}}$$

$$\lambda = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{2\varepsilon_{ox}} + \frac{t_{si}^2}{8}\left(1 - \frac{2}{n(n+1)}\right)} = \frac{t_{si}}{2}\sqrt{\frac{1}{2} + \frac{1}{2r} - \frac{1}{n(n+1)}}$$

2D models: Analysis of the saturated region in DG MOSFETs

Boundary conditions:

$$\varphi(x = -\Delta L) = \varphi(\phi_S = V_{deff} + \phi_b) = \varphi_{sat}$$

$$\left.\frac{d\varphi}{dx}\right|_{x=-\Delta L} = \frac{k\,v_{sat}}{\mu}$$

ΔL, v_{sat}, V_{deff} being respectively the length of the saturation region, the saturation velocity, and the effective drain-source voltage.

ϕ_b is the surface potential at the source and at threshold condition

k=2 for nMOSFETs. k=1 for pMOSFETs

We obtain the following solution:

$$\varphi(x) = \varphi_{sat}\cosh\left(\frac{\Delta L + x}{\lambda}\right) + \frac{k\,v_{sat}}{\mu}\lambda\sinh\left(\frac{\Delta L + x}{\lambda}\right)$$

2D models: Analysis of the saturated region in DG MOSFETs
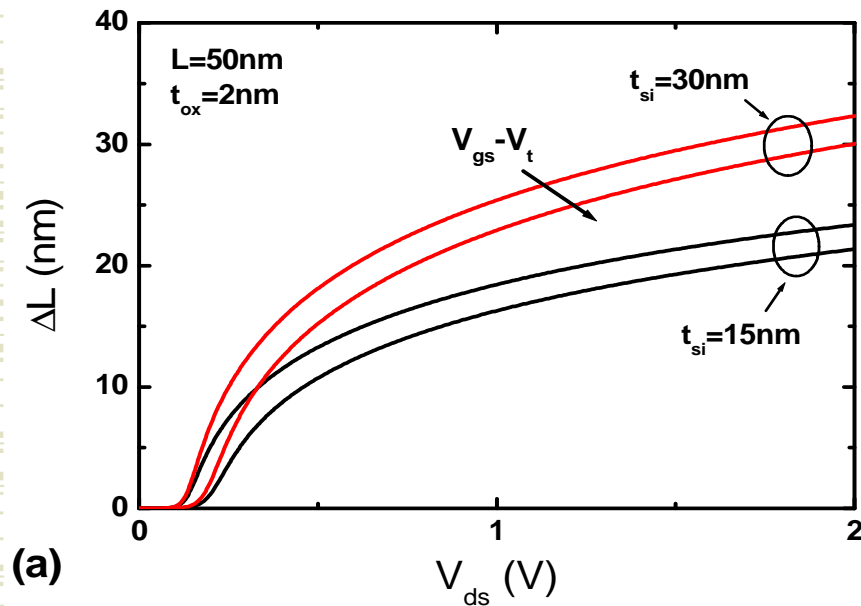
ΔL is then obtained from $\qquad \varphi_d = \varphi(x=0) = \varphi(\phi_S = V_{ds} + \phi_b)$

$$\Delta L = \lambda \ln\left(\frac{\varphi_d + \sqrt{\varphi_d^2 - \varphi_{sat}^2 + \left(\frac{k\,v_{sat}}{\mu}\lambda\right)^2}}{\varphi_{sat} + \frac{k\,v_{sat}}{\mu}\lambda}\right)$$
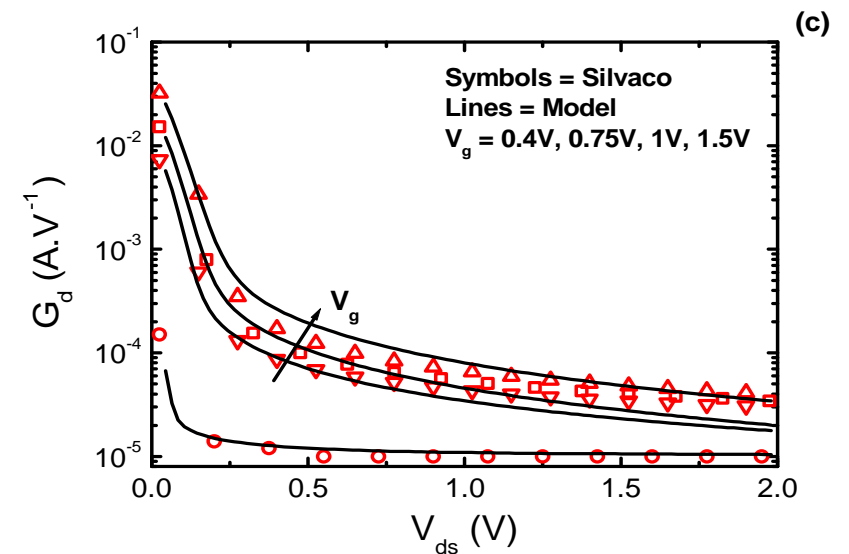
$$\varphi_{sat} = V_{deff} - V_{gs} + V_t - \frac{Q_m}{2C_{ox}} \approx V_{deff} + \frac{Q_s + Q_m}{4C_{ox}} - \frac{Q_m}{2C_{ox}}$$

$$\varphi_d = V_{ds} - V_{gs} + V_t - \frac{Q_m}{2C_{ox}} \approx V_{ds} + \frac{Q_s + Q_m}{4C_{ox}} - \frac{Q_m}{2C_{ox}}$$

2D models: Analysis of the saturated region in DG MOSFETs

(a)

Vgs-Vt=0.25 and 0.5V. L = 50nm

Comparison of the model with Silvaco simulations, for a DG-MOSFET with tox=2nm, tsi=15nm and L=50nm.

3D models:FinFET

◆ This modelling technique can be extended to FinFETs, considering that the electrostatic potential solution will be the sum of several components:

$$\phi(x, y, z) = \phi_{2D}(y, z) + \phi_{3D}(x, y, z)$$

■ Where $\phi_{2D}(y,z)$ is the 2D potential and related to 1D potential as

$$\phi_{2D}(y, z) = \phi_{1D}(y) + \alpha_o(y) \cdot z + \alpha_1(y) \cdot z^2$$

■ With boundary conditions

$$C_{ox1} \cdot \left[V_{GS1} - \phi_{ms} - \phi_{2D}(y, z = h_o) \right] = -\varepsilon_{Si} \left. \frac{\partial \phi_{2D}(y, z)}{\partial z} \right|_{z=h_0} \qquad C_{ox2} \cdot \left[V_{GS2} - \phi_{ms} - \phi_{2D}(y, z = -h_o) \right] = \varepsilon_{Si} \left. \frac{\partial \phi_{2D}(y, z)}{\partial z} \right|_{z=h_0}$$

■ V_{GS1} is the potential applied on both left/right and top gate and V_{GS2} is the potential applied on the bottom gate

3D models:FinFET

♦ $\phi_{1D}(y)$ is the 1D potential solution:

$$\frac{\partial^2 \phi(y)}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\phi(y)/V_t}$$

♦ With boundary conditions:

$$\left.\frac{\partial \phi_{1D}(y)}{\partial y}\right|_{y=0} = 0 \qquad\qquad C_{oxo} \cdot \left[V_{GS1} - \phi_{ms} - \phi_{1D}(y = t_o)\right] = -\varepsilon_{si} \cdot \left.\frac{\partial \phi_0}{\partial y}\right|_{y=t_o}$$

♦ An analytical expression is found for $\phi_{1D}(y)$

3D models:FinFET

- The 3D potential component is the solution of the remaining 3D Laplace's equation with boundary conditions

$$C_{ox1} \cdot [0 - \phi_{3D}(x, y, z = h_o)] = -\varepsilon_{Si} \left. \frac{\partial \phi_{3D}(x, y, z)}{\partial z} \right|_{z=h_0}$$

$$C_{ox2} \cdot [0 - \phi_{2D}(y, z = -h_o)] = \varepsilon_{Si} \left. \frac{\partial \phi_{3D}(x, y, z)}{\partial z} \right|_{z=h_0}$$

$$\phi_{3D}(0, y, z)\big| = V_{bi} - \phi_{2D}(y, z)$$

$$\phi_{3D}(L, y, z)\big| = V_{DS} + V_{bi} - \phi_{2D}(y, z)$$

- An analytical expression is found for ϕ_{3D}

- The approximations used to obtain the analytical solution were to consider that:

  - ϕ_F is constant along the channel (which is valid in subthreshold) and equal to its value at the source end of the channel

  - the short-channel effects are not very severe, so that ϕ_{1D} is the dominant potential contribution for the electron charge density
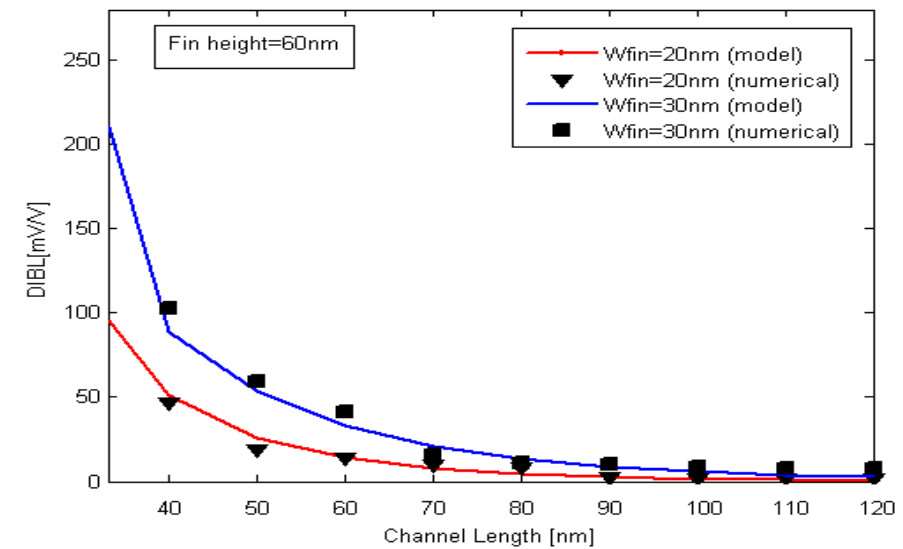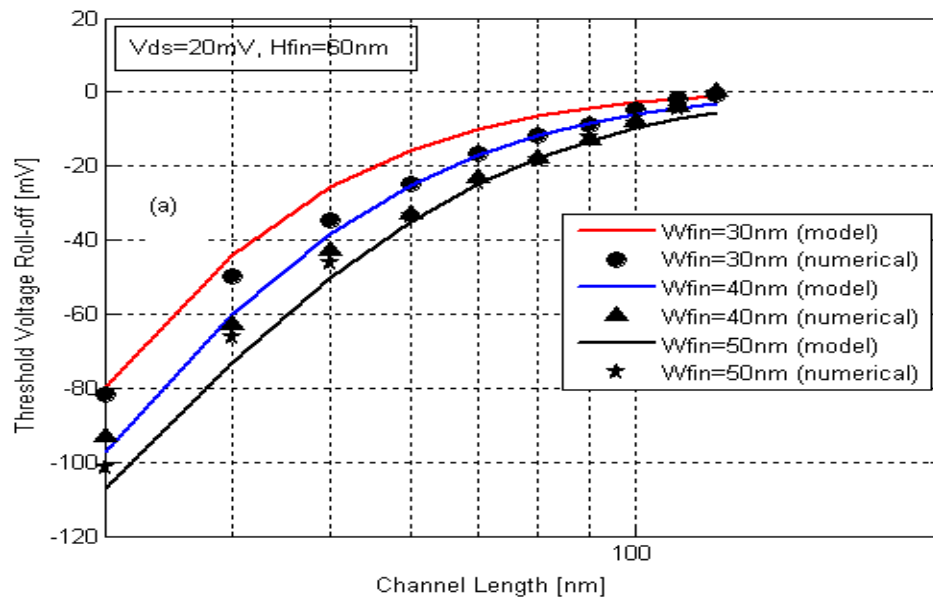
3D models:FinFET

- Using our analytical model for the electrostatic potential, we obtain an analytical expression of the location of the virtual cathode (the point along the channel where the potential is minimum, and therefore, of the minimum value ϕ_{min}

- The position of the virtual cathode will be instrumental to derive the subthreshold swing and threshold voltage expressions.

- Subthreshold swing and threshold voltage models can be developed by taking the values of the integrands at the conduction path (y_c, z_c)

3D models:FinFET

Good agreement with ·3D numerical simulations (DESSIS-ISE) and experimental measurement (devices fabricated by IMEC, Belgium, and measured at UCL, Belgium)

3D models:FinFET

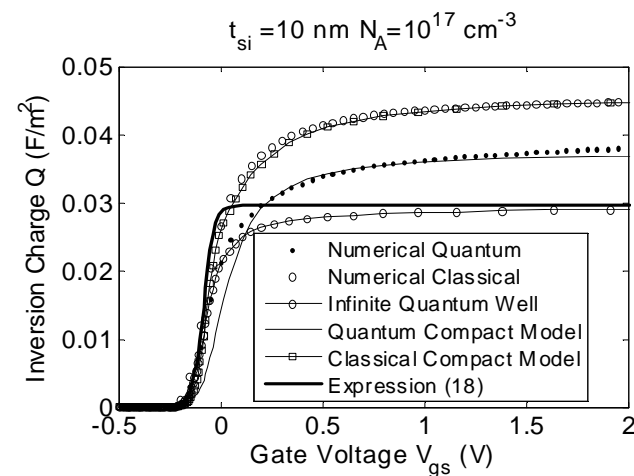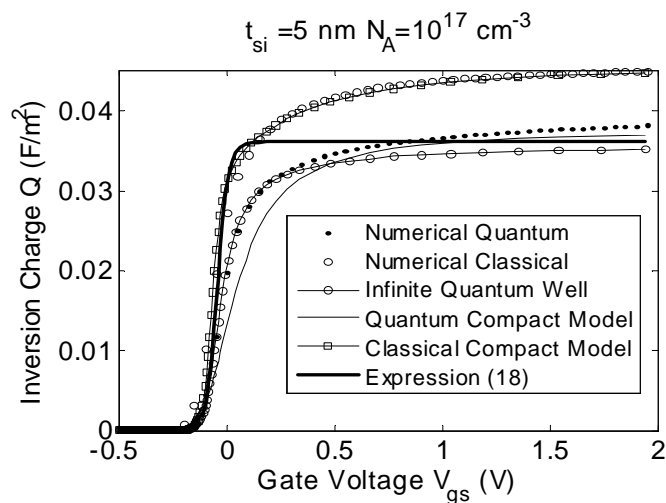
Threshold voltage roll off and DIBL

Quantum effects

- If the silicon layer in the DG and GAA MOSFETs is thinner than 10 nm, quantum confinement cannot be ignored, and Poisson's equation should be solved self-consistently with Schrödinger's equation.

- For this case, an analytical solution is not possible without making assumptions of either the shape of the potential distribution or of the electron distribution.

Quantum effects

◆   The classical compact model can be extended to include quantum effects by using an effective oxide capacitance that takes into account the position of the inversion centroid, which is a function of the inversion charge:
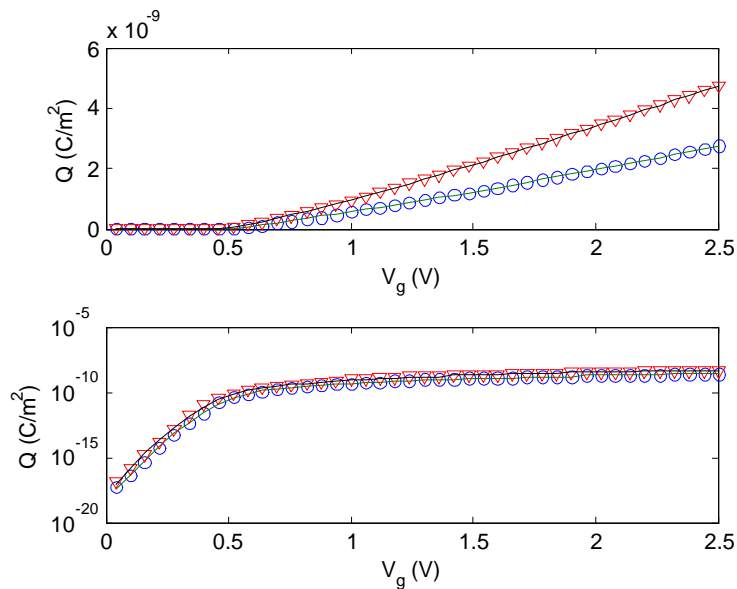
$$C_{ox}^* = \frac{C_{ox}}{1 + C_{ox}\dfrac{y_I}{\varepsilon_{si}}}$$

$$\frac{1}{y_I} = \frac{1}{a + b \cdot t_{si}} + \frac{1}{y_{I0}}\left(\frac{N_I}{N_{I0}}\right)^n$$

$t_{si} = 5$ nm $N_A = 10^{17}$ cm^{-3}

Legend:
- Numerical Quantum
- Numerical Classical
- Infinite Quantum Well
- Quantum Compact Model
- Classical Compact Model
- Expression (18)

$t_{si} = 10$ nm $N_A = 10^{17}$ cm^{-3}

Legend:
- Numerical Quantum
- Numerical Classical
- Infinite Quantum Well
- Quantum Compact Model
- Classical Compact Model
- Expression (18)

Quantum effects

- This modeling of the quantum confinent has been extended to FinFETs

- Total charge sheet density numerically calculated (classic and o quantum) and the charge control model (solid-line) for a FinFET with (Wfin=10 nm, Hfin=30 nm, tox=1.5 nm, tbox=50 nm).

Hydrodynamic model

◆ In extremely short channel DG MOSFET the channel is quasi-ballistic, thus an important overshoot velocity is expected

◆ Using a simplified energy-balance model, the electron mobility is a function of the electron temperature related to the average energy of the carriers.

$$\frac{dT_e}{dx} + \frac{T_e - T_0}{\lambda_w} = -\frac{q}{2k} E_x(x)$$

$$\lambda_w \approx 2 v_{sat} \tau_w$$

τ_w: energy relaxation time

$$T_e(x) = T_0 + \frac{q}{2k} V(x) - \frac{q}{2k\lambda_w} \int_0^x V(\xi) e^{\frac{\xi - y}{\lambda_w}} d\xi$$

Using $E_x(x) = -dV(x)/dx$

Hydrodynamic model

- In contrast with classical drift-diffusion models, the saturated velocity in the saturation region due to non-stationary effects can achieve several times the stationary saturation velocity, v_{sat}.

- This phenomenon is known as velocity overshoot.

- In linear region, the carrier velocity can be obtained from the mobility:

$$v(x) = \mu_n(x) E_x(x) = \frac{\mu_{n0}}{1 + \alpha (T_e(x) - T_0)} E_x(x)$$

$$\alpha = \frac{2k\mu_{n0}}{q\lambda_w v_{sat}}$$

$$\mu_{n0}(t_{si}, E_{eff}) = \frac{U0}{1 + \frac{U0}{\mu_{ph(bulk)}}\left(\frac{\mu_{ph(bulk)}}{\mu_{ph(t_{si(eff)})}} - 1\right) + \theta\frac{UO}{\mu_{sr}}}$$

$$E_{eff} \approx \frac{Q + Q_{dep}}{4\varepsilon_{Si}}$$

Hydrodynamic model

- Using the charge control models previously presented and the velocity expression given above, the drain current in the linear channel region can be obtained:

$$I_{DS} = \frac{W \int_0^{V_{Dsat}} \mu_{n0} Q(V)\, dV}{\int_0^{L_e} \left(1 + \alpha(T_e(x) - T_0)\right) dx} = \frac{W \mu_{eff} \int_0^{V_{Dsat}} Q(V)\, dV}{\int_0^{L_e} \left(1 + \alpha(T_e(x) - T_0)\right) dx}$$
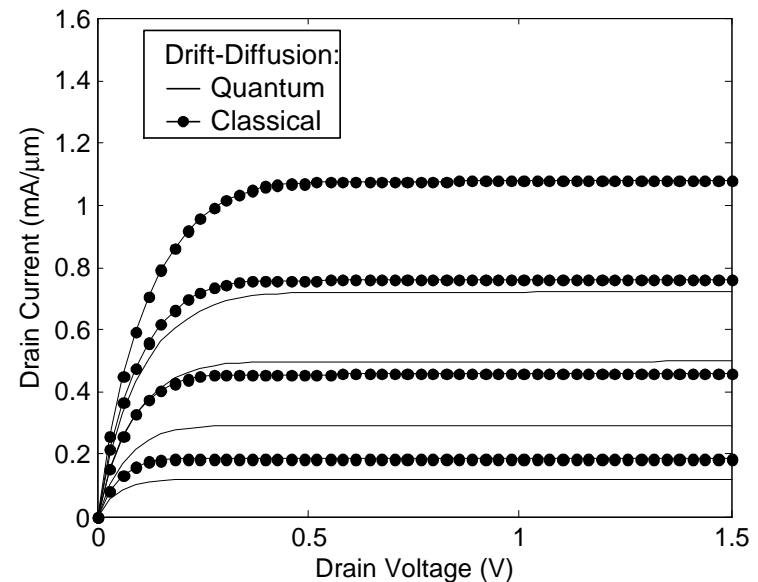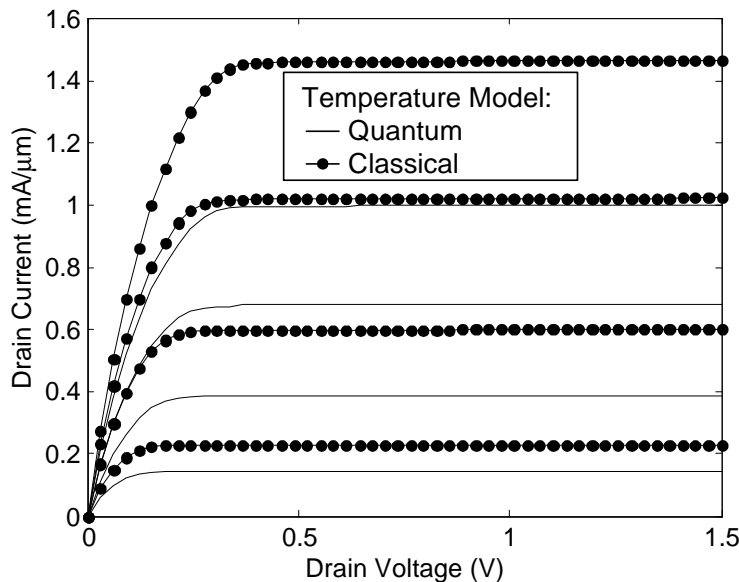
- As a first approximation, in the linear region we can suppose that the lateral field is linear from a small value at the source end to the saturation field at $x = L_e$ ($E_x = E_{sat \cdot x}/L_e$).

$$I_{DS} = \frac{W \mu_{eff} f(V_{gs}, V_{DSS})}{L_e + \dfrac{q\alpha}{2k} \int_0^{L_e} V(\xi) e^{\frac{\xi - L_e}{\lambda_w}} d\xi} = \frac{W}{L_e} \frac{\mu_{eff} f(V_{gs}, V_{DSS})}{1 + \gamma_n V_{DSS}}$$

$$\gamma_n = \frac{\mu_{eff}}{v_{sat} L_e} \frac{1}{(1 + 2\lambda_w/L_e)}$$

V_{DSS}: effective drain-source voltage

Hydrodynamic model

A comparison of drain current for FinFET (Wfin=10 nm, Hfin=30 nm, tox=1.5 nm, tbox=50 nm)), L=100 nm, for classical charge control (•) and quantum charge (-) using a) Temperature model b) Drift-Diffusion model. The gate voltages are Vgs-VTH=0.5, 0.75, 1 and 1.25 V.

Charge modelling

- The total channel charge is obtained by integrating the mobile charge density over the channel length.

- In doped DG MOSFETs, using the charge control model above explained:

$$Q_{Tot} = -2W \int_0^L Q\,dx = -(2W)^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2\,dV$$

$$Q_{Tot} = -(2W)^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{C_{ox}} + \frac{kT}{q} Q + \frac{kT}{q} \frac{Q^2}{Q + Q_{Dep}} \right) dQ$$

$$Q_{Tot} = -(2w)^2 \frac{\mu}{I_{DS}} \left(\frac{Q^3}{3C_{ox}} + \frac{kT}{q} \frac{Q^2}{2} + \frac{kT}{q} \left(-Q_{Dep} Q + \frac{Q^2}{2} + Q_{Dep}^2 \log[Q_{Dep} + Q] \right) \right) \Big|_{Q_s}^{Q_d}$$

- The total gate charge is: $Q_G = -Q_{Tot} - Q_{ox} + WLQ_{Dep}$, where Q_{ox} is the total oxide fixed charge at both front and back interfaces.

Charge modelling

- The total drain and source charges are obtained as:

$$Q_D = -2W \int_0^L \frac{x}{L} Q dx = \frac{(2w)^3 \mu^2}{LI^2{}_{DS}} \int_{Q_s}^{Q_d} Q^2 \left(\left(\frac{Q^2 - Q_s{}^2}{2C_{ox}} \right) + \frac{kT}{q} \left(2(Q - Q_s) - Q_{Dep} \log \left[\frac{Q + Q_{Dep}}{Q_s + Q_{Dep}} \right] \right) \right) \cdot$$

$$\cdot \left(\frac{1}{C_{ox}} + \frac{kT}{q} \left(\frac{1}{Q} + \frac{1}{Q + Q_{Dep}} \right) \right) dQ$$

$$Q_S = Q_{Tot} - Q_D$$

- The transcapacitances are necessary to develop the small-signal model. They are obtained by differentiating the total charges with respect to the applied voltages.

- There are 6 transcapacitances. 4 of them are independent.

Charge modelling

♦ In independently-biased DG MOSFETs we should consider a front gate charge and a back gate charge

$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{C_{ox}(1+\alpha)} + \frac{kT}{q} \left(Q + \frac{2Q^2}{2Q+Q_0} \right) \right) dQ$$

$$Q_F = \frac{Q_G}{1+\alpha} + \frac{W}{1+\alpha} 2\alpha \cdot V_{GS} L$$

$$Q_D = W \int_0^L \frac{x}{L} Q dx = -\frac{W^3 \mu^2}{L(I_{DS})^2} \int_{Q_s}^{Q_d} Q^2 \left(\left(\frac{Q^2 - Q_s^2}{2C_{ox}(1+\alpha)} \right) + \frac{kT}{q} \left(2(Q - Q_s) - \frac{1}{2} Q_0 \log \left[\frac{2Q + Q_0}{2Q_s + Q_0} \right] \right) \right) \cdot$$
$$\cdot \left(\frac{1}{C_{ox}(1+\alpha)} + \frac{kT}{q} \left(\frac{1}{Q} + \frac{2}{2Q+Q_0} \right) \right) dQ$$

Charge modelling

- The intrinsic capacitances, C_{gd} and C_{gs}, are obtained as:

$$C_{gi} = -\frac{dQ_G}{dVi}$$

- where $i=d,s$

- The non-reciprocal capacitances C_{dg} and C_{sg} are obtained as:

$$C_{ig} = \frac{dQ_i}{dV_G}$$

- The capacitances C_{sd} and C_{ds} are computed as follows

$$C_{ds} = -\frac{dQ_D}{dV_S} \qquad C_{sd} = -\frac{dQ_S}{dV_D}$$

Charge modelling

Normalized gate to drain capacitance (a, b) and gate to source capacitance (c, d) with respect to the gate voltage, for V_{DS}=1V (a, d) and V_{DS}=0.05V (b,c). Solid line: Atlas simulations; Symbol line: our

model. Doped DG MOSFET with N_A=6·10^{17} cm^{-3}

Normalized drain to gate capacitance (a, c) and source to gate capacitance (b, d) with respect to the gate voltage, for V_{DS}=1V (a, b) and V_{DS}=0.05V (c,d). Solid line: Atlas simulations; Symbol line: our model. Doped DG MOSFET with N_A=6·10^{17} cm^{-3}

Charge modelling

♦ In undoped cylindrical GAA MOSFETs:

$$Q_{Tot} = -2\pi R \int_0^L Q \, dx = -(2\pi R)^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 \, dV$$

$$Q_{Tot} = -(2\pi R)^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{C_{ox}} + \frac{kT}{q} Q + \frac{kT}{q} \frac{Q^2}{Q + Q_0} \right) dQ$$

$$Q_{Tot} = -(2\pi R)^2 \frac{\mu}{I_{DS}} \left(\frac{Q^3}{3C_{ox}} + \frac{kT}{q} \frac{Q^2}{2} + \frac{kT}{q} \left(-Q_0 Q + \frac{Q^2}{2} + Q_0^2 \log[Q_0 + Q] \right) \right) \Big|_{Q_s}^{Q_d}$$

$$Q_D = -2\pi R \int_0^L \frac{x}{L} Q \, dx = \frac{(2\pi R)^3 \mu^2}{L(I_{DS})^2} \int_{Q_s}^{Q_d} Q^2 \left(\left(\frac{Q^2 - Q_s^2}{2C_{ox}} \right) + \frac{kT}{q} \left(2(Q - Q_s) - Q_0 \log\left[\frac{Q + Q_0}{Q_s + Q_0} \right] \right) \right) \cdot$$

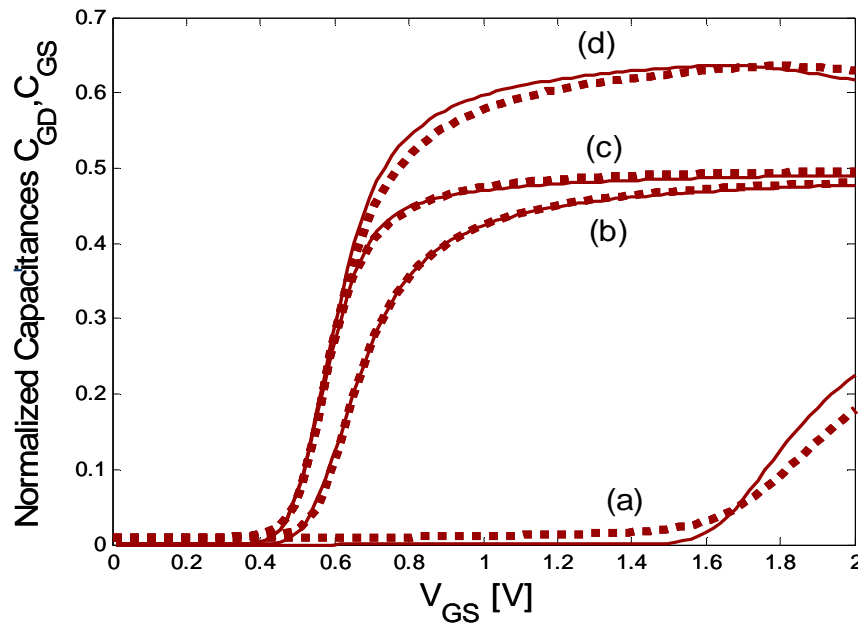$$\cdot \left(\frac{1}{C_{ox}} + \frac{kT}{q} \left(\frac{1}{Q} + \frac{1}{Q + Q_0} \right) \right) dQ$$
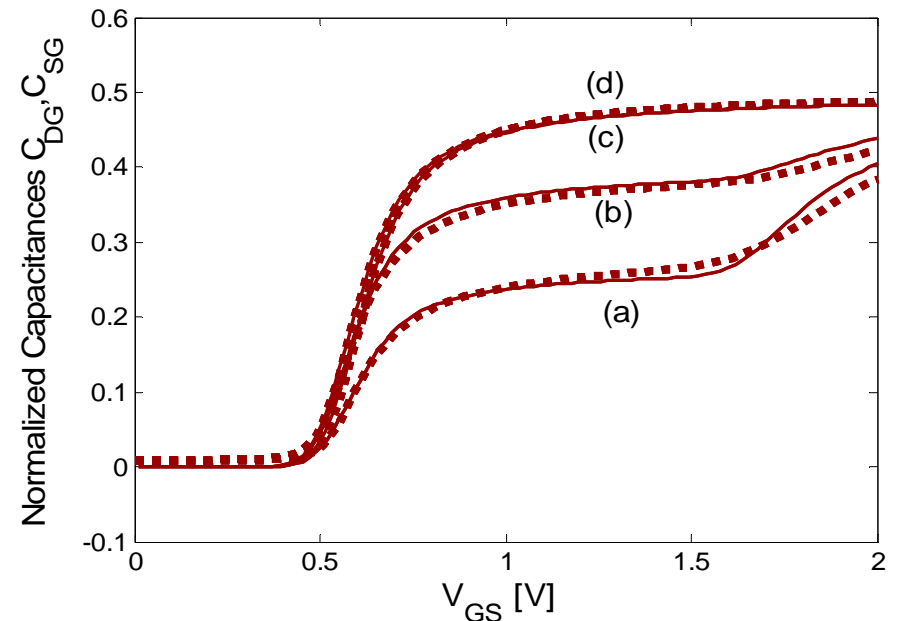
Charge modelling

Normalized drain to gate capacitance (a, c) and source to gate capacitance (b, d) with respect to the gate voltage, for $V_{DS}=1V$ (a, b) and $V_{DS}=0.1V$ (c, d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model

Normalized drain to source capacitance (c,d) and source to drain capacitance (a, b) with respect to the gate voltage, for $V_{DS}=1V$ (a, d) and $V_{DS}=0.1V$ (b, c). Solid line: DESSIS-ISE simulations; Symbol line: analytical model

Charge modelling

- In undoped DG MOSFETs:

$$Q_{Tot} = -W\int_0^L Qdx = -W^2\frac{\mu}{I_{DS}}\int_0^{V_{DS}}Q^2 dV$$

$$Q_{Tot} = -W^2\frac{\mu}{I_{DS}}\int_{Q_s}^{Q_d}\left(\frac{Q^2}{2C_{ox}}+\frac{kT}{q}Q+\frac{kT}{q}\frac{Q^2}{Q+2Q_0}\right)dQ$$

$$Q_{Tot} = -W^2\frac{\mu}{I_{DS}}\left(\frac{Q^3}{6C_{ox}}+\frac{kT}{q}\frac{Q^2}{2}+2\frac{kT}{q}\left(-Q_0 Q+\frac{Q^2}{4}+2Q_0^2\log[2Q_0+Q]\right)\right)\Bigg|_{Q_s}^{Q_d}$$

$$Q_D = -W\int_0^L\frac{x}{L}Qdx = -\frac{W^3\mu^2}{L(I_{DS})^2}\int_{Q_s}^{Q_d}Q^2\left(\left(\frac{Q^2-Q_s^2}{4C_{ox}}\right)+\frac{kT}{q}\left(2(Q-Q_s)-2Q_0\log\left[\frac{Q+2Q_0}{Q_s+2Q_0}\right]\right)\right)\cdot$$
$$\cdot\left(\frac{1}{2C_{ox}}+\frac{kT}{q}\left(\frac{1}{Q}+\frac{1}{Q+2Q_0}\right)\right)dQ$$
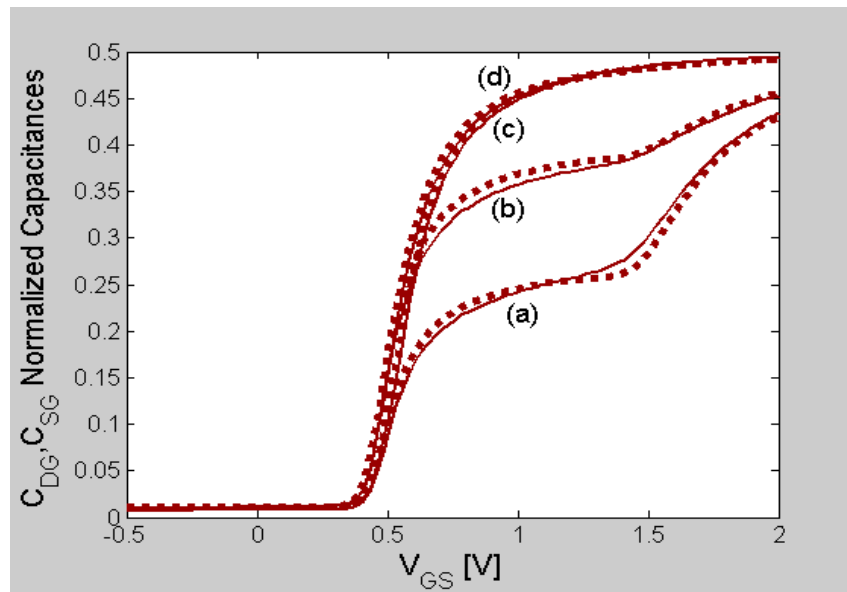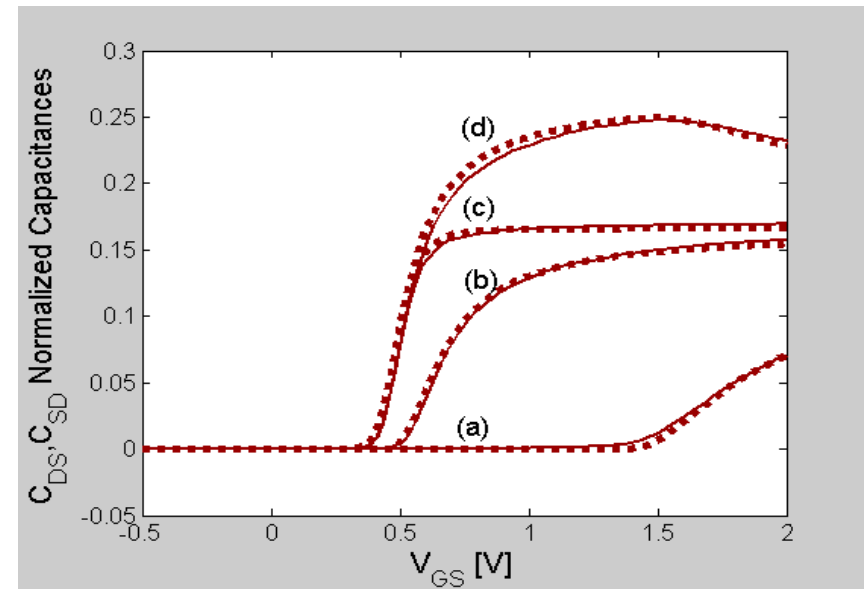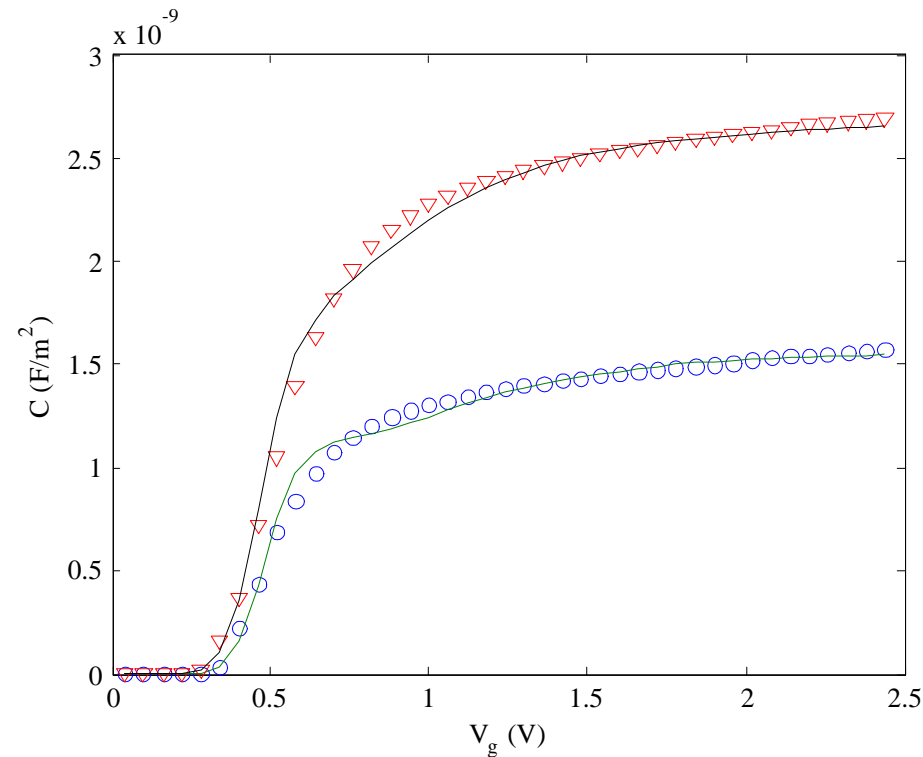
Charge modelling
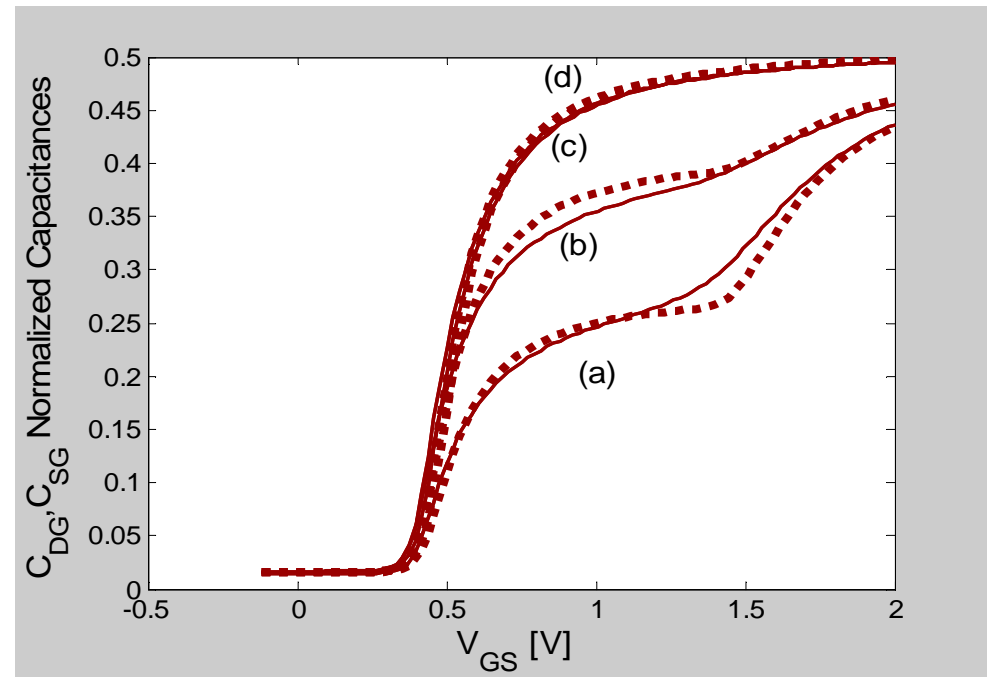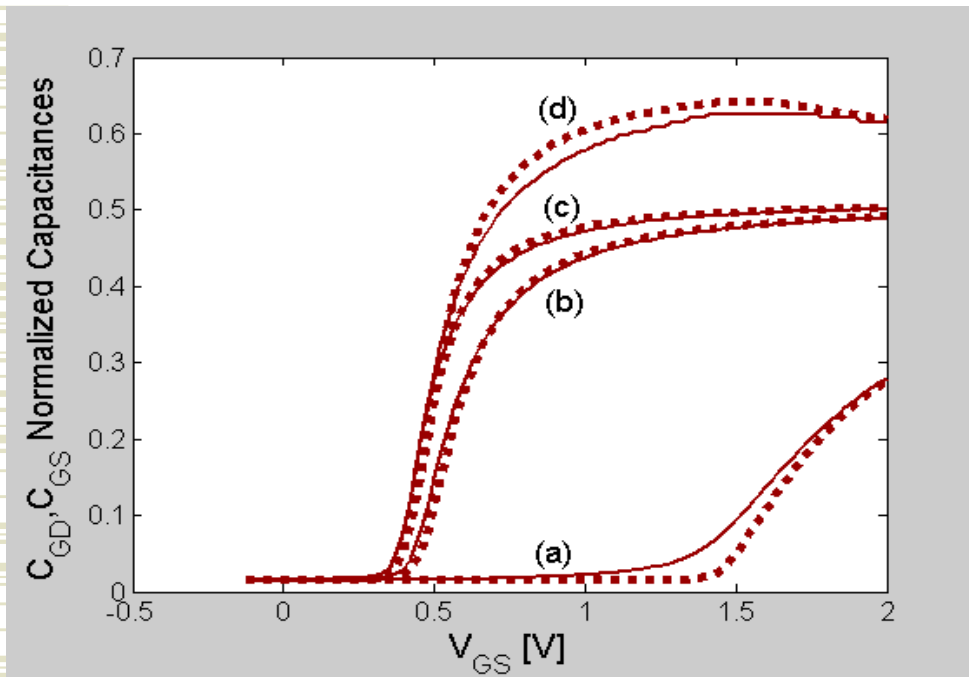
Normalized gate to drain capacitance (a, b) and gate to source capacitance (c, d) with respect to the gate voltage, for V_{DS}=0.05V (b,c) and V_{DS}=1V (a,d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model

Normalized drain to gate capacitance (a, c) and source to gate capacitance (b, d) with respect to the gate voltage, for V_{DS}=1V (a, b) and V_{DS}=0.05V (c, d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model

Charge modelling: Independently Biased DG MOSFET

Normalized gate-to-drain capacitance (a, b) and gate-to-source capacitance (c, d) with respect to the gate voltage, for V_{DS}=0.05V (b,c) and V_{DS}=1V (a,d); t_{si}=31nm. Solid line: analytical model; Symbol line: DESSIS-ISE simulation

Normalized drain-to-gate capacitance (a, c) and source-to-gate capacitance (b, d) with respect to the gate voltage, for V_{DS}=1V (a, b) and V_{DS}=0.05V (c, d); t_{si}=31nm Solid line: analytical model; Symbol line: DESSIS-ISE simulation

Capacitance modelling: quantum effects

Gate-to-Channel numerically calculated (∇ classic and o quantum) and the charge control model (solid-line) for a FinFET with (Wfin=10 nm, Hfin=30 nm, tox=1.5 nm, tbox=50 nm).

High frequency and noise modelling

- The active line approach, used to extend the model to high frequency operation, is based on splitting the channel into a number of elementary sections

- Our quasi-static small-signal equivalent circuit, to which we add additional microscopic diffusion and gate shot noise sources, is applied to each section

- Our charge control model allows to obtain analytical expressions of the local small-signal parameters in each segment
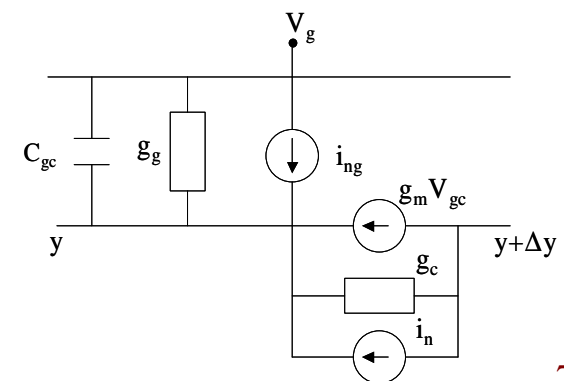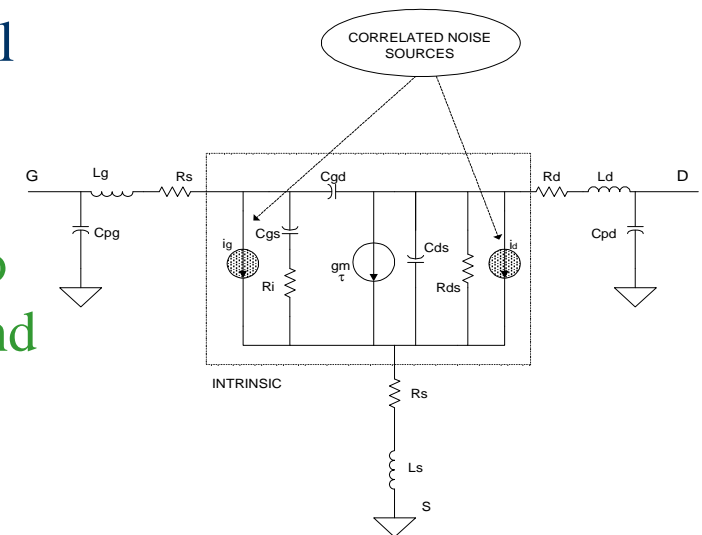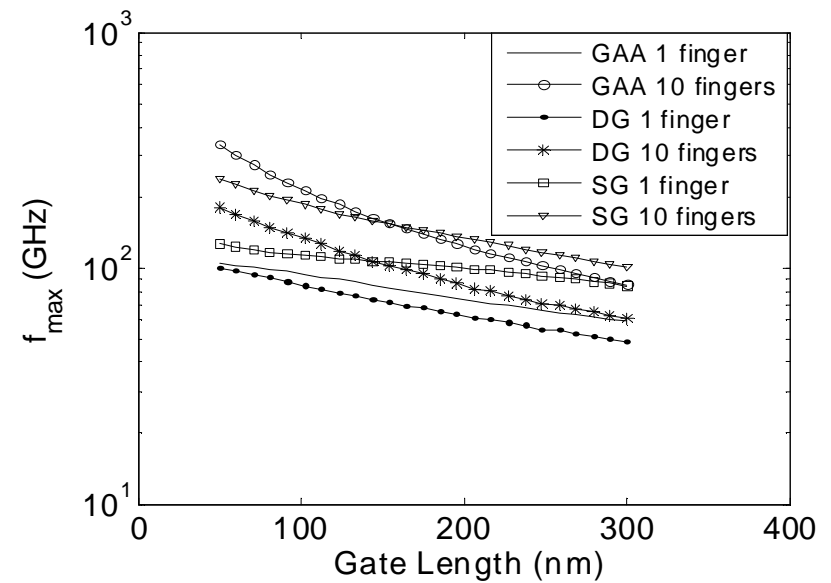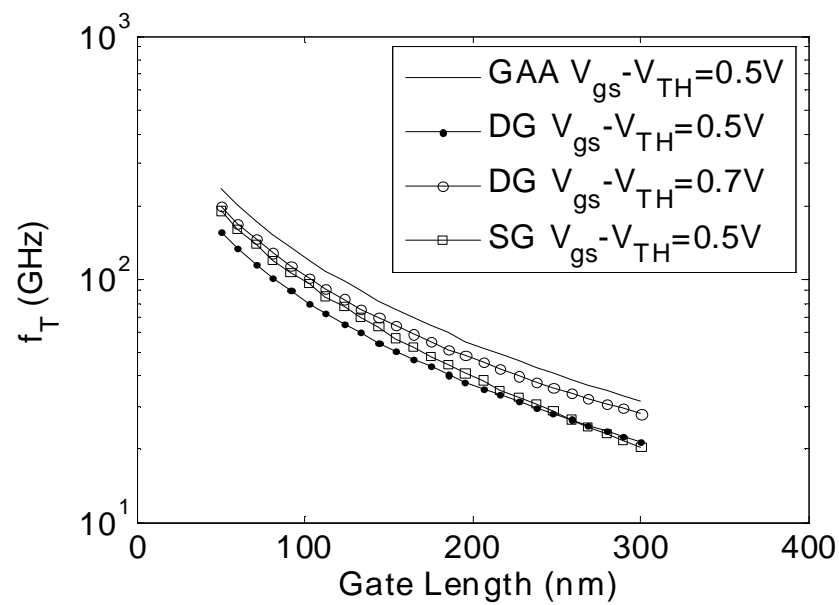
High frequency and noise modelling

◆ In order to model noise using this technique, several approaches have been considered:

- The contribution to noise of the length where carriers travel at the saturation velocity must not neglected.

- A Diffusion Coefficient is used to define the microscopic noise current sources, in order to consider the short channel effect. The expression of the diffusion coefficient is valid from low to high fields

- Mobility reduction should be considered along the channel.
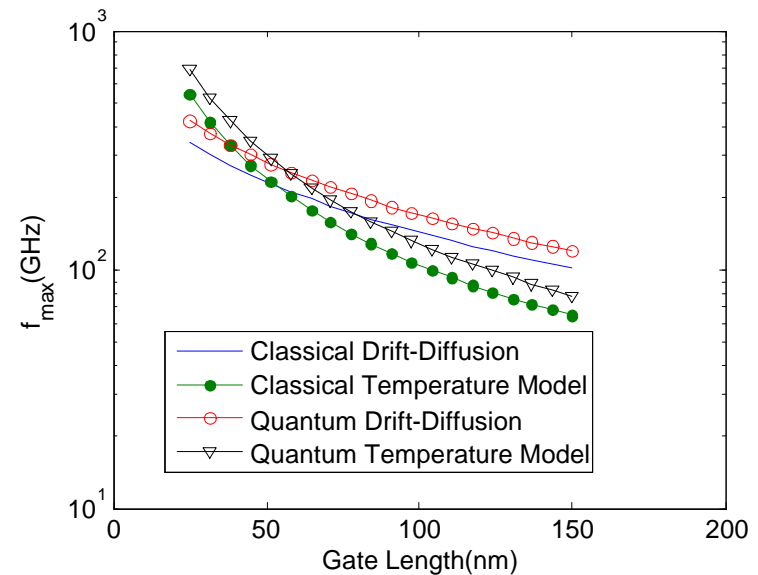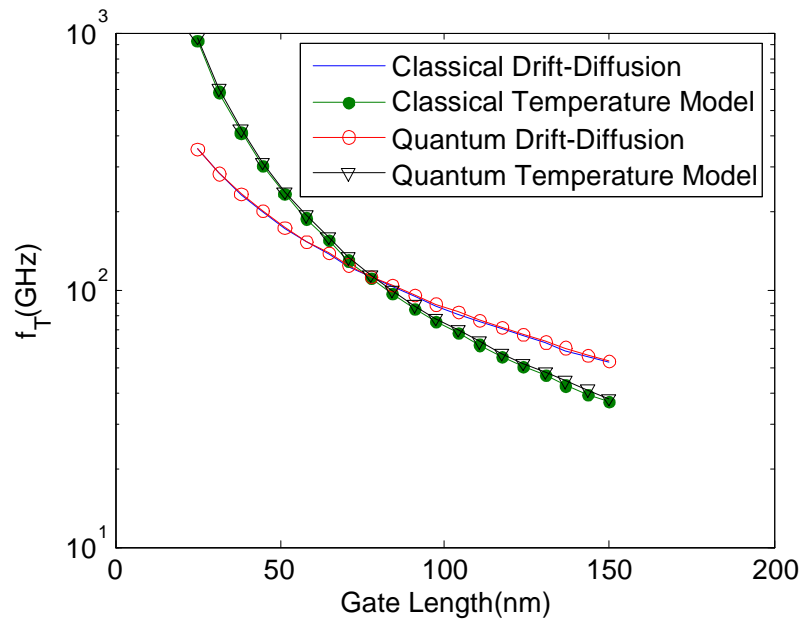
High frequency and noise modelling

- The active transmission line is analysed using the nodal admittance method
- Once the intrinsic admittance matrix, Y_i, and admittance correlation matrix, C_{Yi}, are obtained, extrinsic elements are included
- Thermal noise is considered for access resistances
- Gate tunnelling current, and its associated shot noise source are added

- Using the model, we calculate the S-parameters and the usual noise parameters: F_{min}, R_n (equivalent noise resistance) and G_{opt} (optimum reflection coefficient)
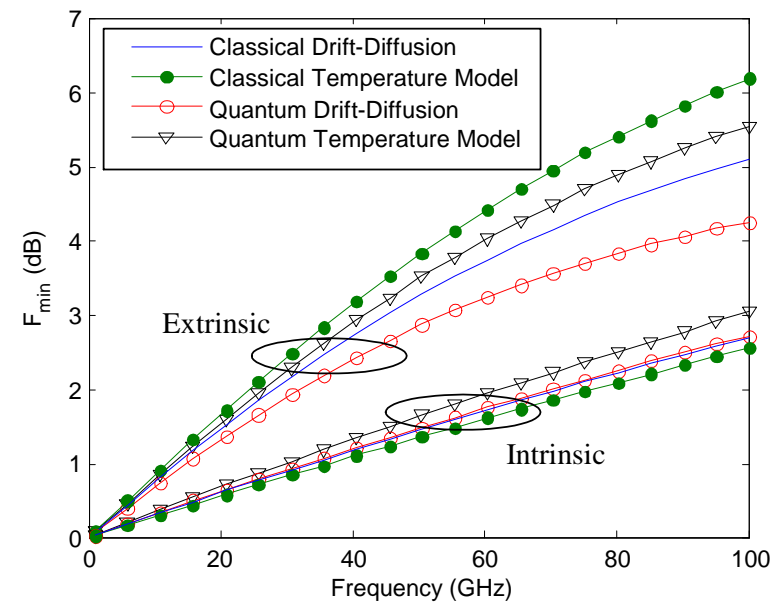- ◆
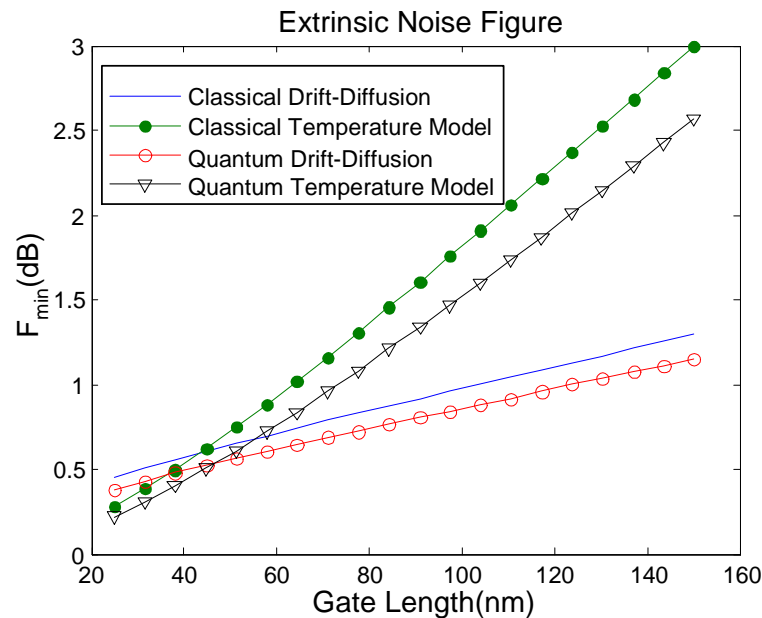
High frequency and noise modelling

High frequency and noise modelling

FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, V_{ds}=1 V, V_{gs}-V_{TH}=0.5V).

High frequency and noise modelling

FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, 100 fingers, V_{gs}-V_{TH}=0.5V, V_{ds}=1V)

Conclusions

- We have discussed techniques to develop compact models in Thin-Film SOI MOSFETs (FD SOI MOSFDETs, AM SOI MOSFETs, DG MOSFETs, GAA MOSFETs, FinFETs)
- Very few models are currently available for FD SOI MOSFETs in circuit simulators
- No models available for AM SOI MOSFETs
- Compact models for Multi-Gate MOSFETs are still under development
  - They face important challenges for nanoscale devices: scaling with volume inversion/accumulation, quantum confinement, hydrodinamic transport
  - These effects, although considered by UFDG, are hard to take into account in a full compact analytical way

Conclusions

- **We have also reviewed our approaches:**
  - A core model, developed from a unified charge control model obtained from the 1D Poisson's equation (using some approximations in the case of DG MOSFETs)
  - 2D or 3D scalable models of the short-channel effects (threshold voltage roll-off, DIBL, subthreshold swing degradation and channel length modulation), developed by solving the 2D or 3D Poisson's equation using appropriate techniques
- **Quantum effects have been including by using an effective oxide thickness which accounts for the position of the inversion centroid**
- The active transmission line approach extends the models to the high frequency and noise analysis