



Simulation of CMOS inverters based on the novel Surrounding Gate Transistors. A Verilog-A implementation.

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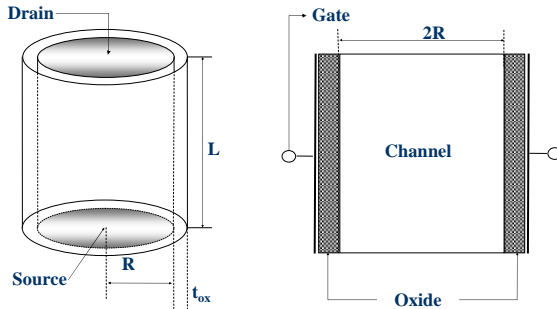
Introduction

A Verilog-A compact model for Surrounding Gate Transistors (SGTs) has been implemented to study basic digital circuits.

The main features of CMOS inverters based on the novel SGTs have been analyzed.

The initial classical drain current model has been enhanced to account for quantum effects. Both the electron and hole layers are known to be highly confined in these structures due to structural as well as electrical confinement. The influence of confinement effects in several circuits based on these quantum nanowires are characterized in depth. In particular, CMOS inverter gate delays, CMOS inverter ring oscillator frequencies, etc., have been obtained in order to explore the relations between the most representative technological parameters of the transistors and the inverters performance.

Classical charge and current model for SGTs [1]



$$C_{Oxide} = \frac{\epsilon_{ox}}{R \cdot \ln\left(1 + \frac{t_{ox}}{R}\right)}$$

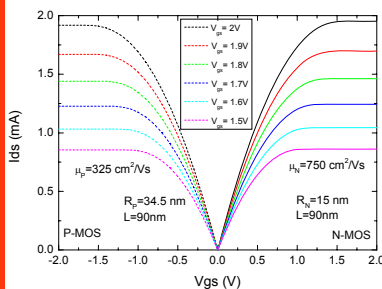
$$Q_0 = \frac{4\epsilon_{Si} kT}{R q}$$

$$V_T = V_0 + 2V_{th} \ln\left(1 + \frac{Q_0'}{Q_0}\right) + \Delta V_{TQM}$$

$$V_0 = \phi_{MS} + \frac{kT}{q} \ln\left(\frac{8}{\delta R^2}\right) \quad \delta = \frac{q^2 n_i}{kT \epsilon_{Si}}$$

$$\Delta V_T = \frac{\left(\frac{2C_{TOTAL} V_{th}^2}{Q_0}\right) Q_0'}{(Q_0 + Q_0')}$$

$$I_{ds} = \frac{2\pi R}{L} \mu \left[\frac{2kT}{q} (Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kTQ_0}{q} \ln\left(\frac{Q_d - Q_0}{Q_s - Q_0}\right) \right]$$



The capacitances of the structure are obtained following reference [2].

Finally, the models for both N-type and P-type SGTs are implemented in Verilog-A [3].

Output curves of matched N- and P- SGTs at room temperature (classical model).

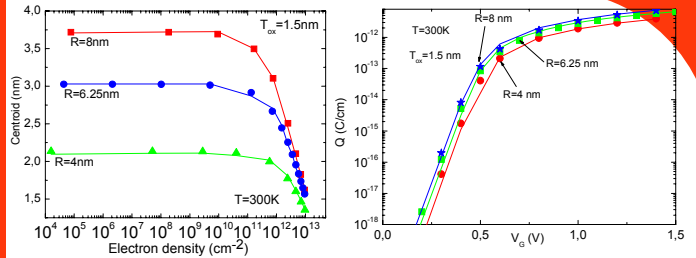
Quantum effects in SGTs

The inversion charge centroid z_i is modelled to account for the realistic charge distribution [4]. A new gate-channel capacitance model is used, corresponding to a higher oxide thickness, which is corrected to include the inversion charge centroid in the channel.

$$\frac{1}{z_i} = \frac{1}{a + b \times 2 \times R} + \frac{1}{z_{i0} \left(\frac{N_I}{8.26 \times 10^{12} \text{ cm}^{-2} - 4.9 \times 10^{18} \text{ cm}^{-3} \cdot R(\text{cm})} \right)^n}$$

$$C_{Semiconductor} = \frac{\epsilon_{Si}}{(R - z_i) \ln\left(1 + \frac{z_i}{R - z_i}\right)}$$

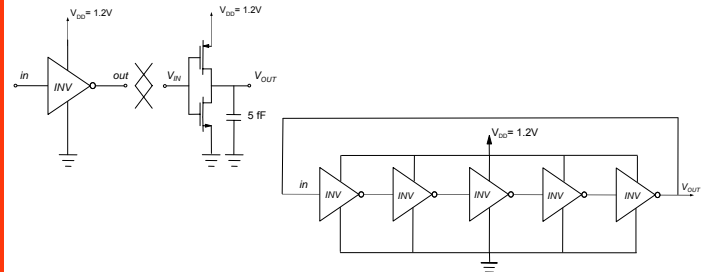
$$\frac{1}{C_{TOTAL}} = \frac{1}{C_{Oxide}} + \frac{1}{C_{Semiconductor}}$$



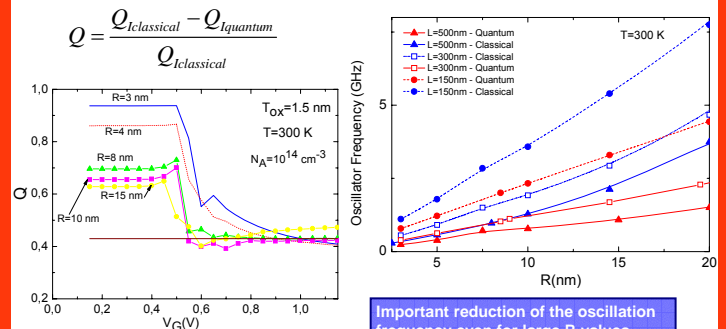
Inversion charge centroid for a SGT at room temperature with $R=4, 6.25, 8$ nm. The simulation results (lines), the model data (solid squares)

Channel charge at the source for SGTs at room temperature ($R=4, 6.25, 8$ nm). Simulation results, obtained taking quantum effects into account, (solid lines), Modeled data (symbols).

CMOS inverters and Oscillator rings



Technological data for the SGTs used in these circuits: oxide thickness was $T_{ox}=1.5$ nm, the electron and hole effective mobilities were $750 \text{ cm}^2/\text{Vs}$ and $325 \text{ cm}^2/\text{Vs}$ respectively, following the experimental data obtained by Singh et al. [5]. For these enhancement transistors, we have $V_{TN} \approx |V_{TP}| \approx 0.5$ V. The average ratio of the inversion charge centroid for P-type/N-type devices is $z \approx 1.77/1.12$ [6]; in this respect, the same empirical model has been used in both cases.



Important reduction of the oscillation frequency even for large R values. Structural and electrical confinement influence the result.

CONCLUSIONS

A CMOS inverter based on SGTs has been studied. To do so, a new model for the SGT was implemented (using Verilog-A) in a circuit simulator (ELDO, Mentor Graphics). The sizing of the transistors has been done by equating the transconductance parameter adapted to the particular geometry of the SGTs. The CMOS inverter propagation delay and the oscillation frequency of a five stage ring oscillator have been calculated.

The influence of quantum effects in a SGTs in the oscillation frequency of a five stage oscillator ring has been studied. It can be seen that the reduction of the oscillation frequency when quantum effects are included is very important, both the structural and electrical confinement makes this reduction noticeable even for high values of the radius.

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ACKNOWLEDGMENTS

This work was partially carried out within the framework of Research Project TEC-2005-01948 supported by the Spanish Government, and TIC-2005-831 supported by the Junta de Andalucía.