



# VERTICAL PNP TRANSISTOR TCAD SIMULATION

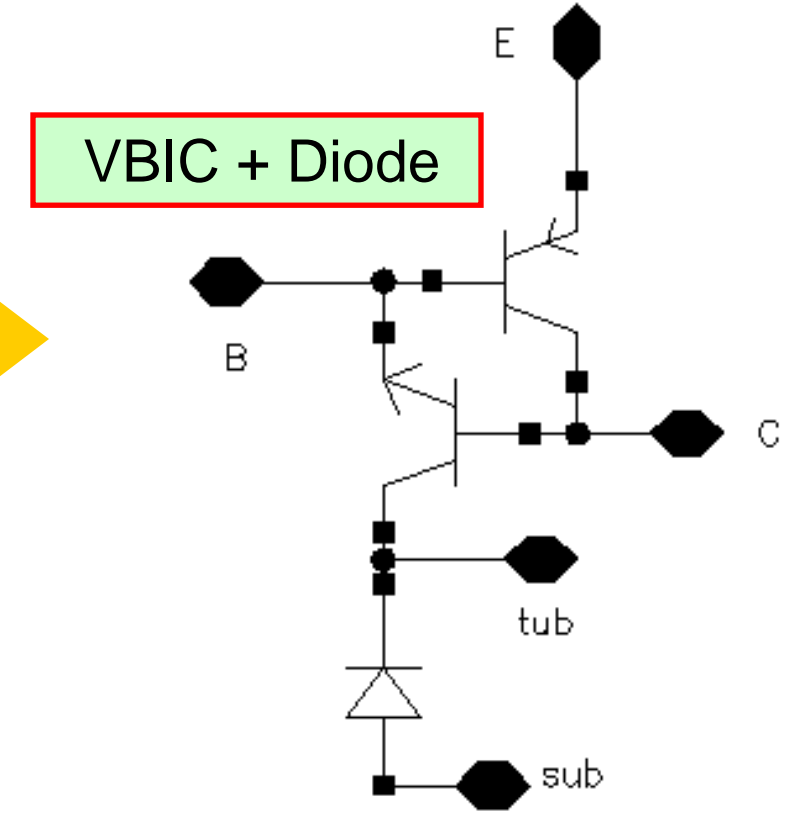
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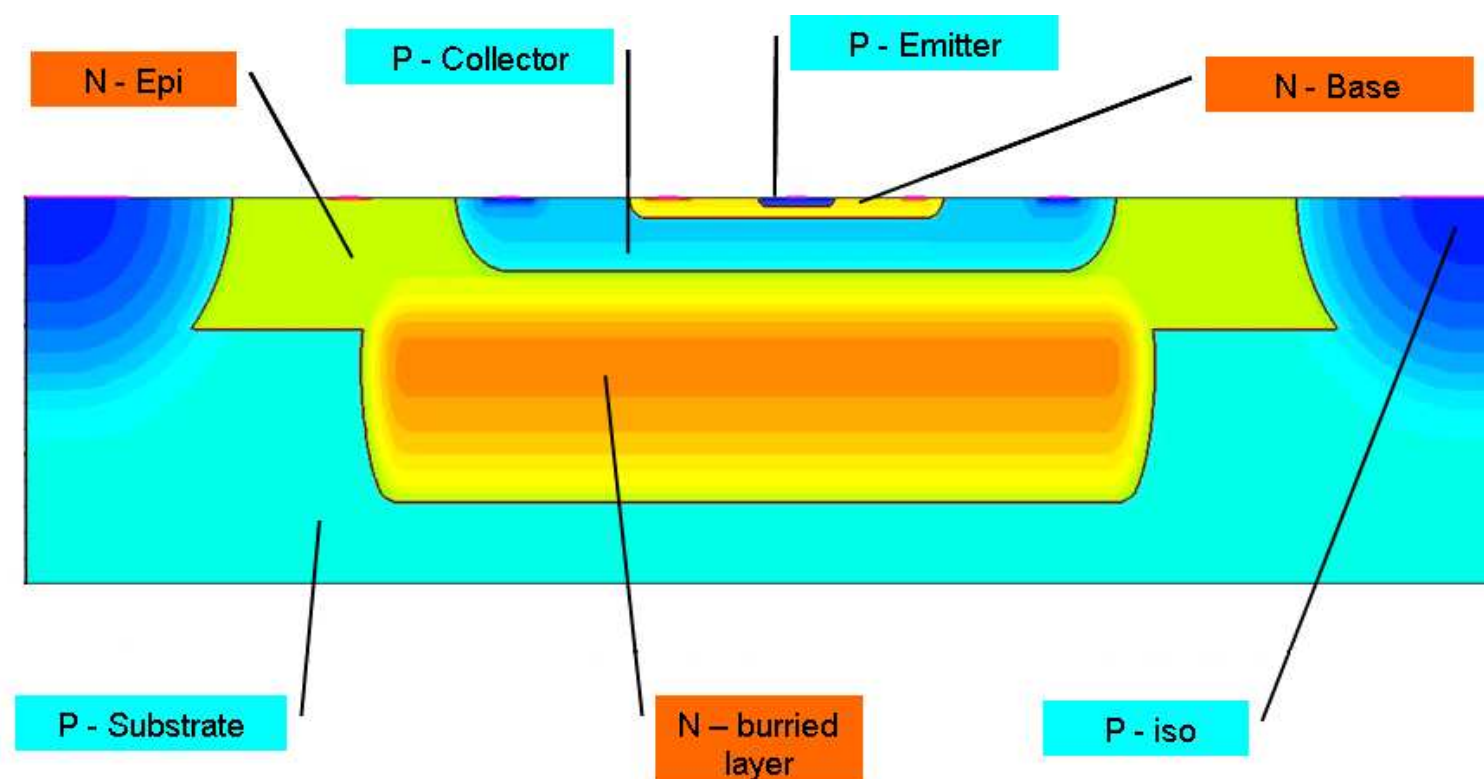
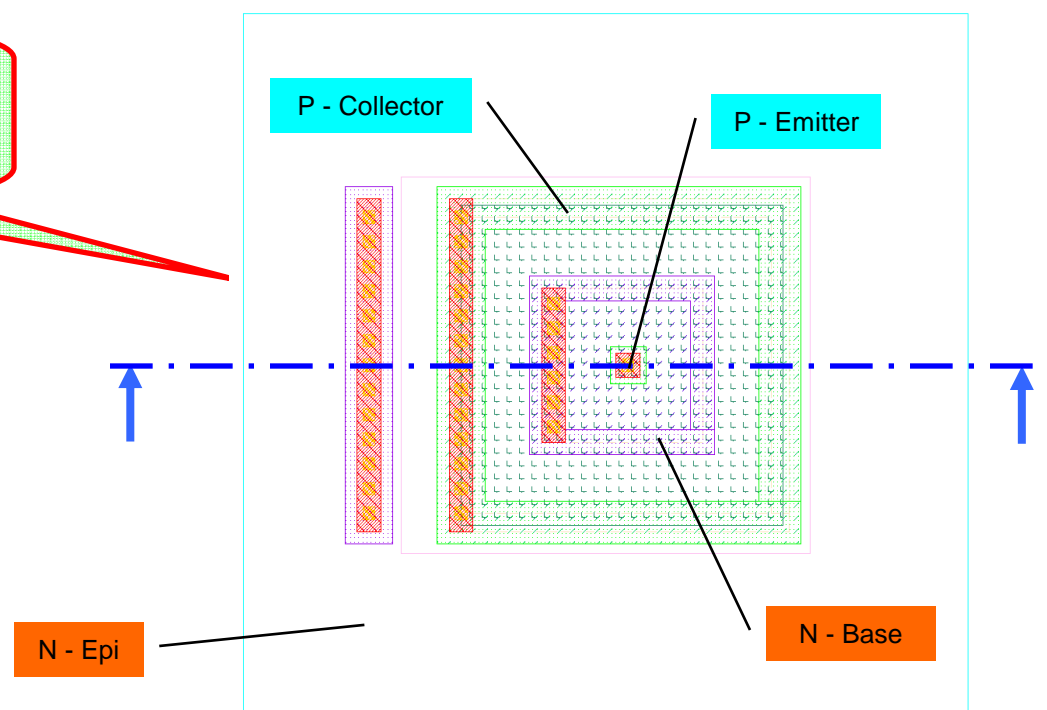
## Goal of the contribution

Vertical PNP transistors (PNPV) are mostly modeled by a macro model using the VBIC model and a parasitic diode between the substrate and the N-type well, which isolates the collector. However, the PNPV is a 5-layer vertical structure with 2 parasitic transistors. The substrate current can be significant when the device is in saturation and this phenomenon is not covered by the VBIC model with the parasitic diode. This paper deals with TCAD simulations of vertical PNP transistor in saturation. It describes electrical behavior inside the complex structure focusing on the substrate current. The presentation suggests modifications in the transistor layout to reduce the parasitic substrate current.



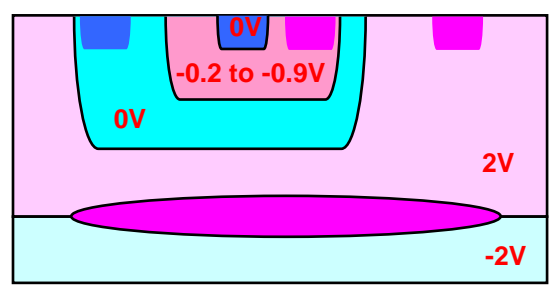
## The tested PNPV transistor

PNPV layout from Cadence

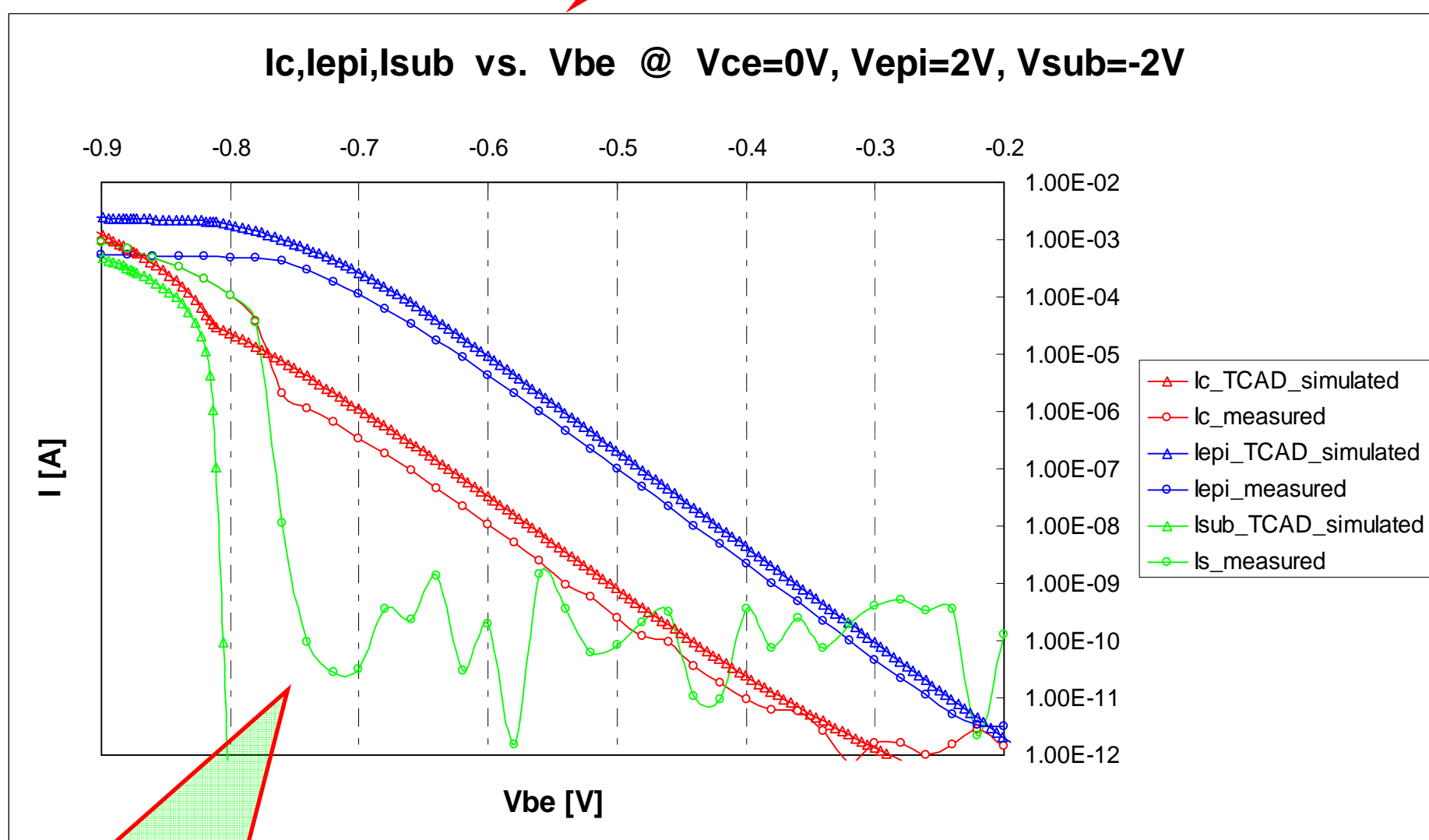


Slice of transistor used for TCAD simulation

## TCAD Simulation of the PNPV in saturation

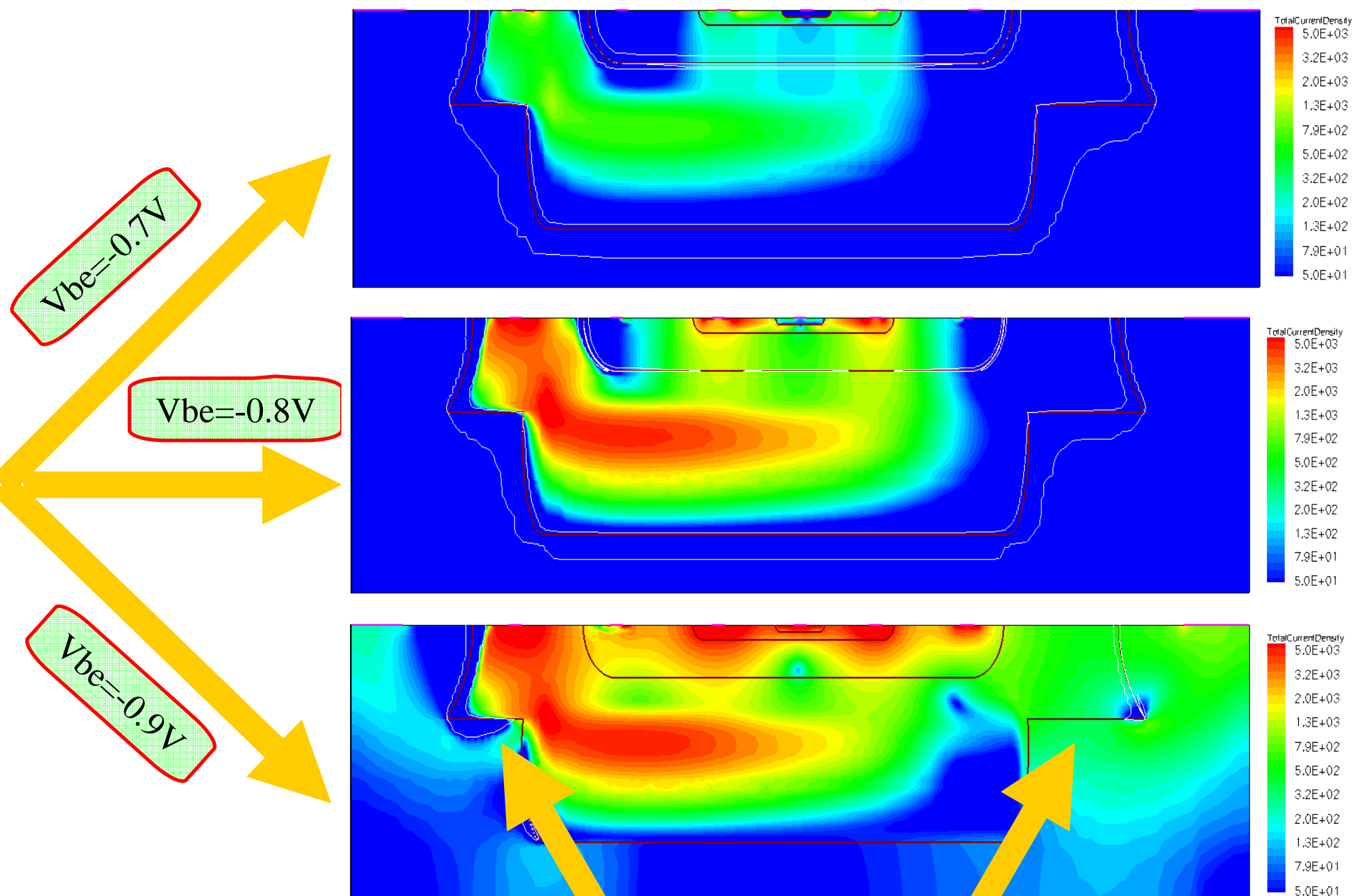


TCAD simulation versus measured data from silicon



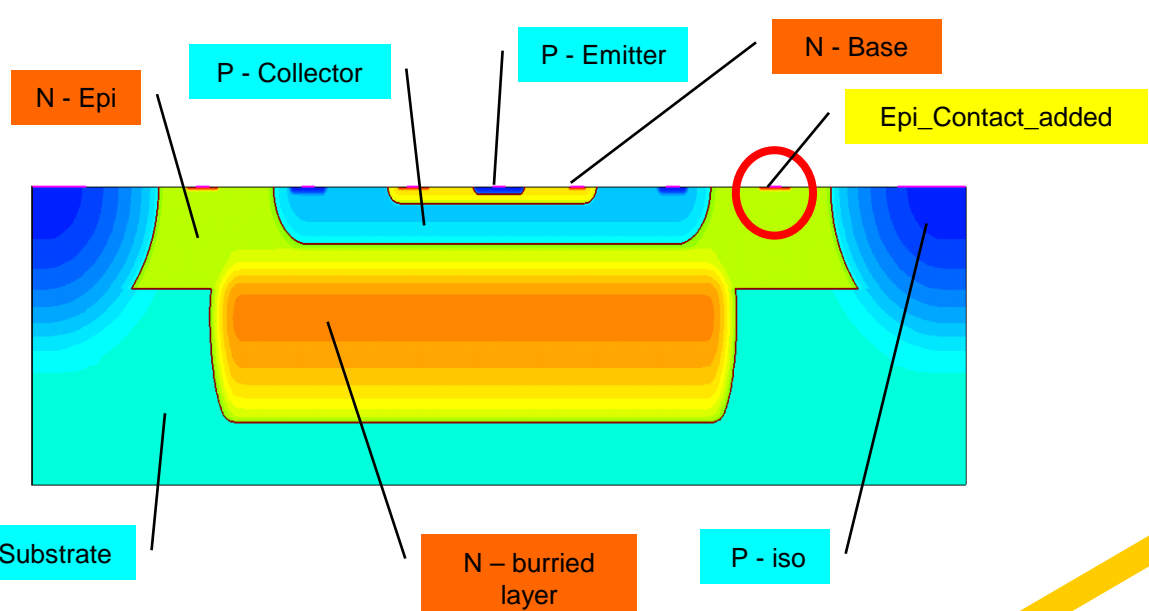
The same trends for both curves  
GOOD FIT

Total current densities [ $Acm^{-2}$ ] in transistor for different bias points during TCAD simulation.

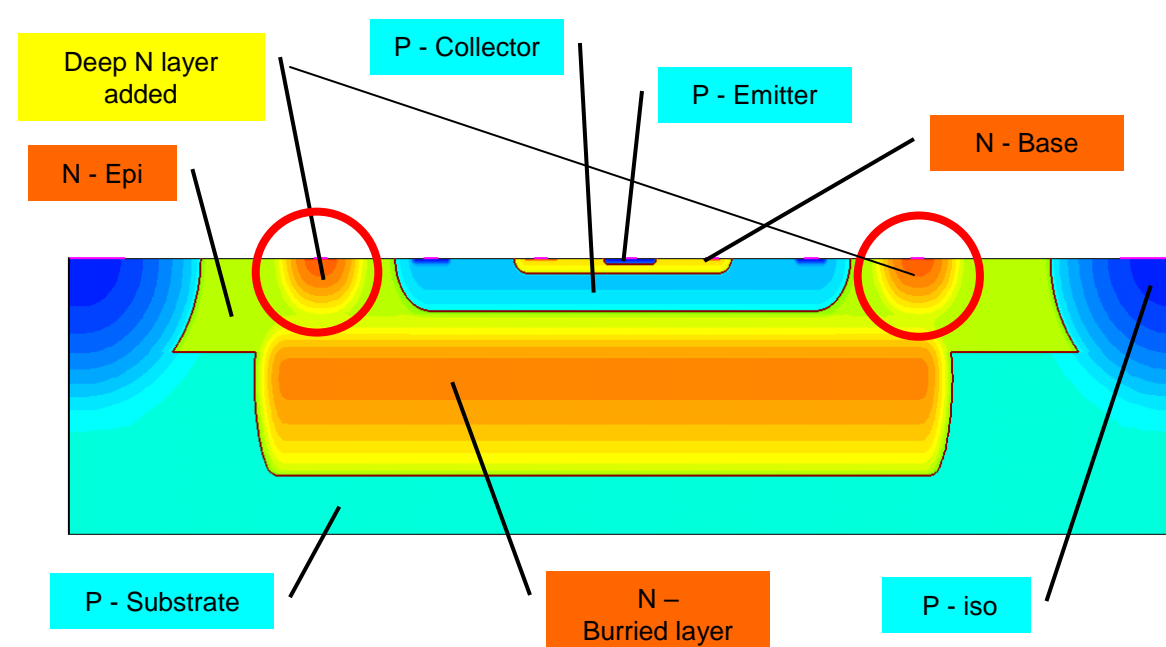


At the bias points @  $V_{be} < -0.8V$  there is so strong injection of holes from emitter that these injected holes are not caught in collector. They drift to N-type well (the epitaxial layer) and majority recombine in high doped N-buried layer. However some of them don't recombine in the epitaxial layer and flow to substrate. This current of holes flow especially in areas where is no N-buried layer.

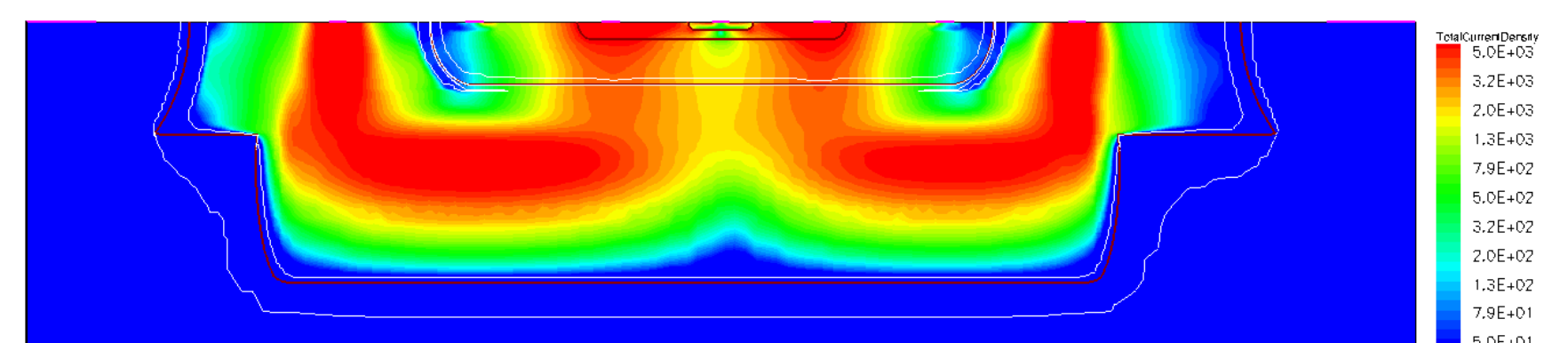
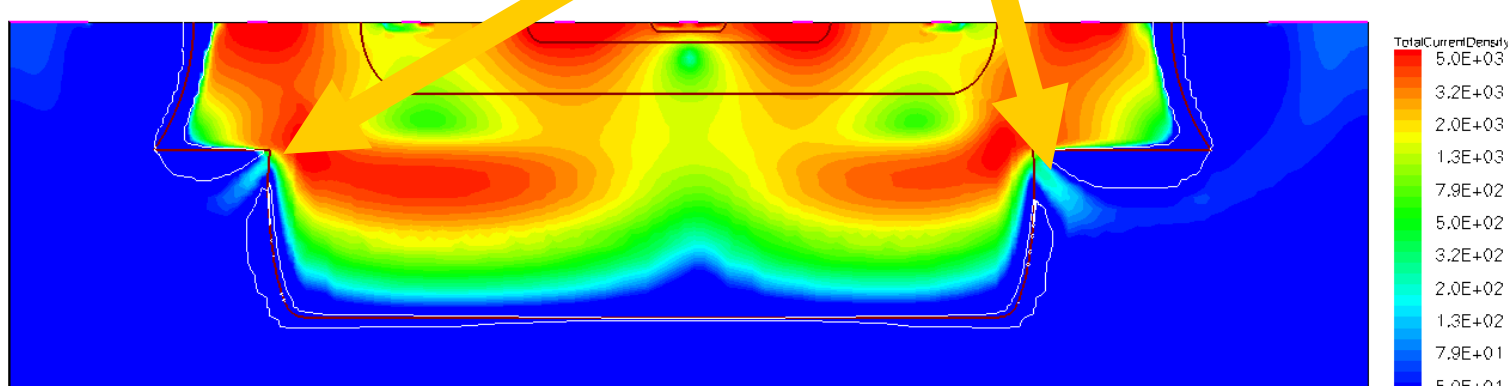
## Modifications in the transistor layout



In the modified layout there is contact to the epitaxial layer on the both side. The current flows symmetric in the device. The substrate current is much smaller than in original one.



The addition of deep N-layer improve recombination of the injected holes in the N-type well. The current to substrate is reduced dramatically. The increase of transistor area is drawback of this modification.



## REFERENCES

[1] Synopsys, Sentaurus Structure Editor User Guide Version A-2007.12, December 2007