



# The PSP compact MOSFET model

## An update

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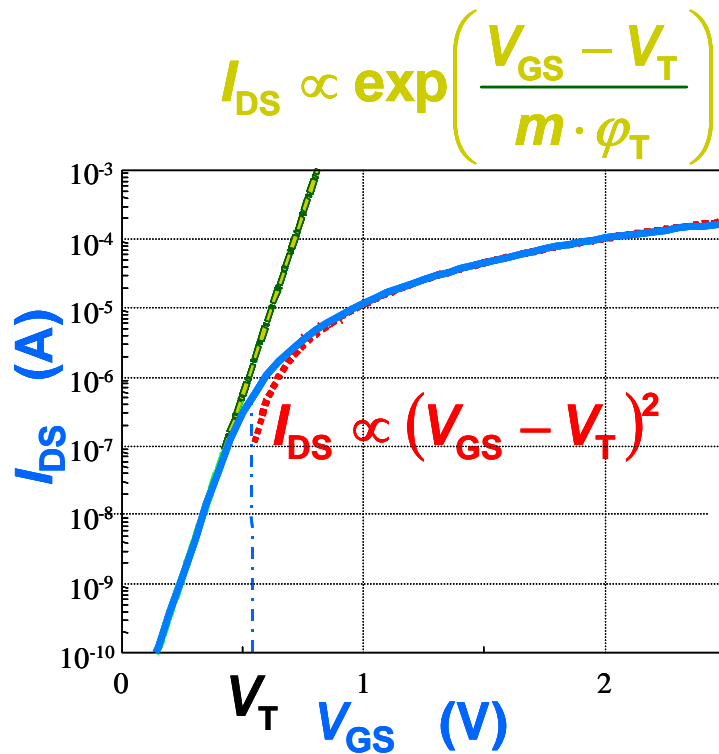
# contents

- ▶ why PSP? (recap)
- ▶ recent model additions
- ▶ simulation time & JUNCAP Express
- ▶ upcoming model updates

# why PSP: overview

- ▶ transition from subthreshold region to strong inversion
- ▶ output conductance
- ▶ Gummel symmetry
- ▶ capacitances
- ▶ thermal noise and induced gate noise
- ▶ ...

# from subthreshold region to strong inversion



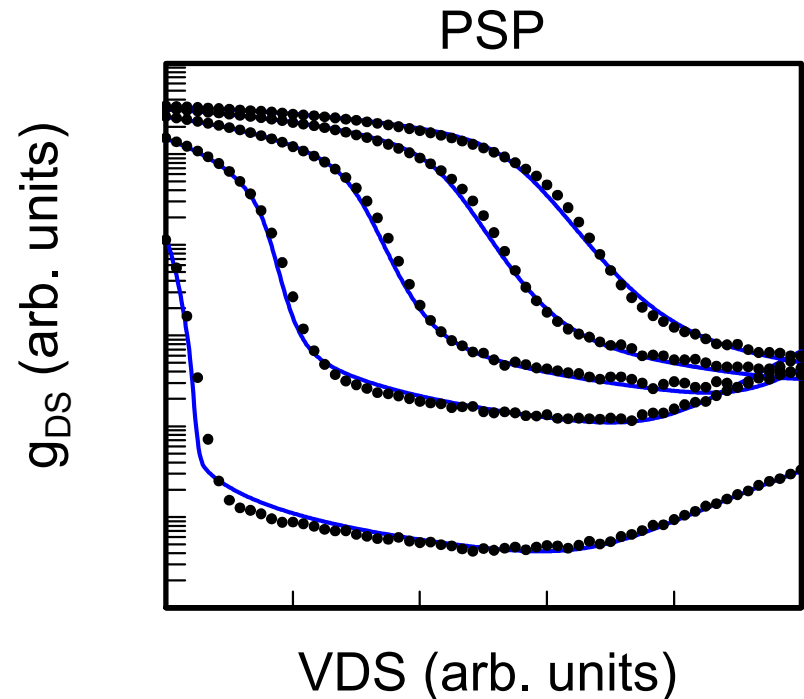
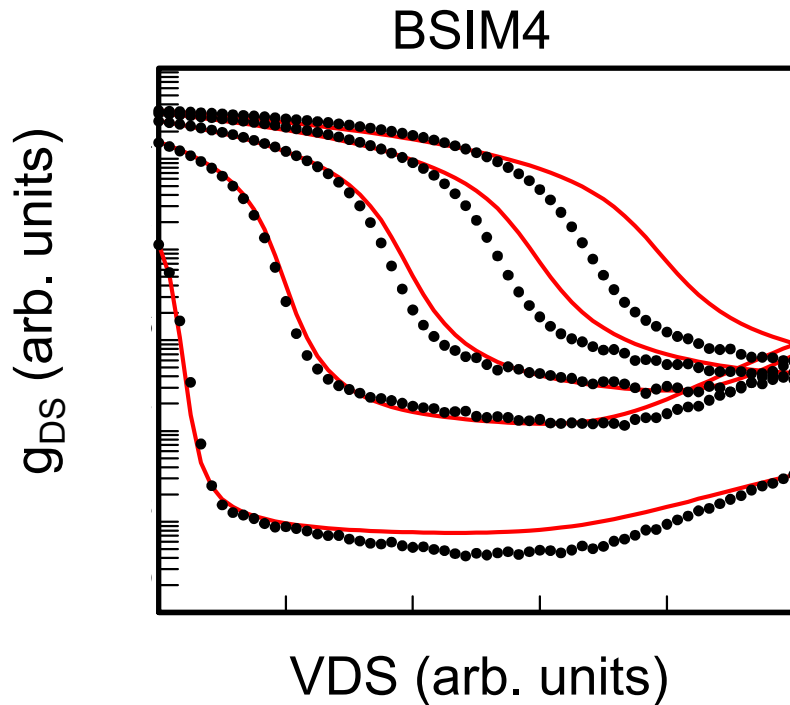
## ▶ BSIM4

- threshold-voltage based
- gluing function

## ▶ PSP

- surface potential based
- one well-behaved physics-based expression
- leads, e.g., to better  $g_{m3}$  modelling

# long-channel output conductance



- systematic long-standing problem in BSIM4
- problem gets progressively worse for higher-order derivatives
- analog designers are using these devices!
- also short-channel  $g_{DS}$  form PSP superior (not shown here)

# Gummel symmetry

- ▶ MOSFET models describe currents for  $V_{DS} > 0$ :  $I = I_+(V_D, V_G, V_S, V_B)$
- ▶ MOSFET is symmetric device  
(layout extractor doesn't which terminal is source and which is drain)

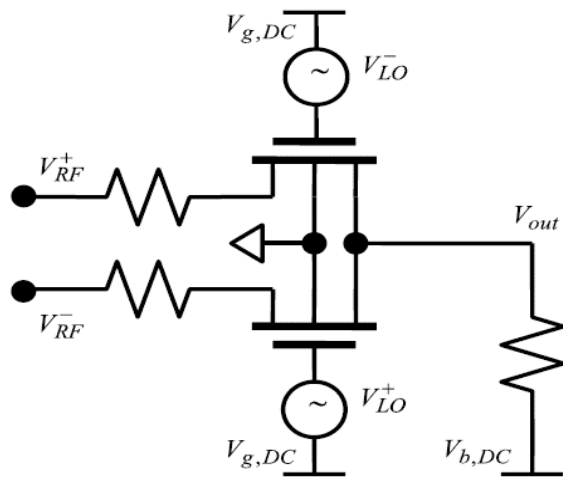
- ▶ for negative VDS source-drain exchange is applied:

$$I_-(V_D, V_G, V_S, V_B) = -I_+(V_S, V_G, V_D, V_B)$$

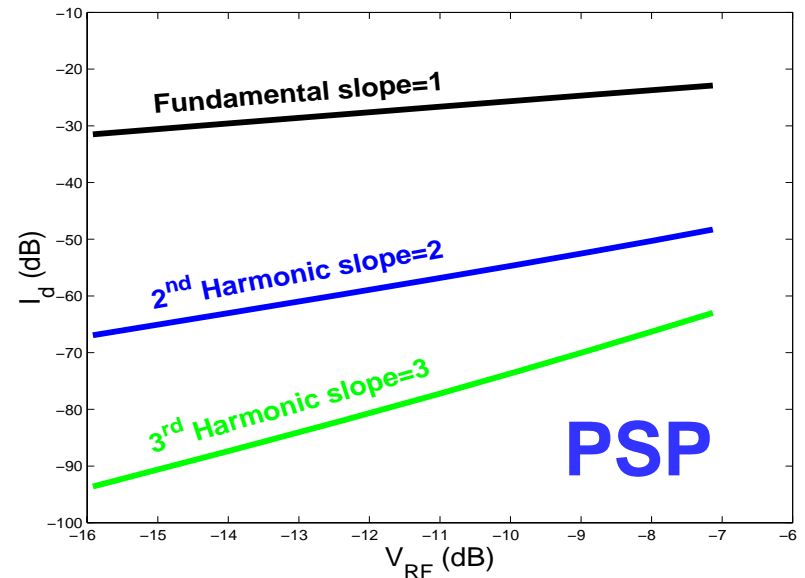
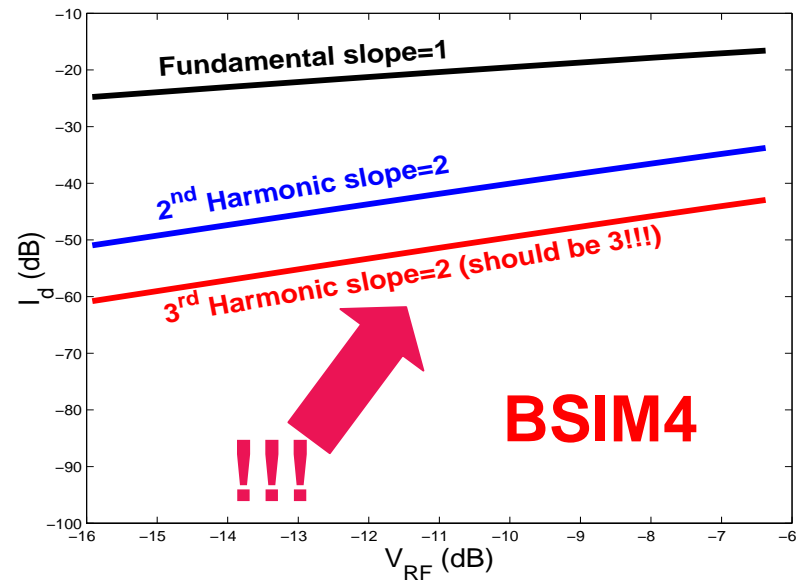
- ▶ continuity of current and derivatives is not trivial!
- ▶ if fulfilled the model is called “Gummel symmetric”
- ▶ similar considerations apply to
  - gate current
  - capacitances
- ▶ lack of Gummel symmetry one of the long-standing problems in BSIM4
- ▶ relevant in RF circuit design:
  - passive mixers
  - variable gm circuits
  - continuous time integrators

# circuit example: passive mixer

passive RF mixer



from: P. Bendix et al., CICC 2004



# capacitances

$$C_{ij} = (2 \cdot \delta_{ij} - 1) \cdot \frac{\partial Q_i}{\partial V_j}$$

symmetry at  $V_{DS}=0V$

$$C_{iD} = C_{iS} \quad \text{and} \quad C_{Dj} = C_{Sj}$$

reciprocity at  $V_{DS}=0V$

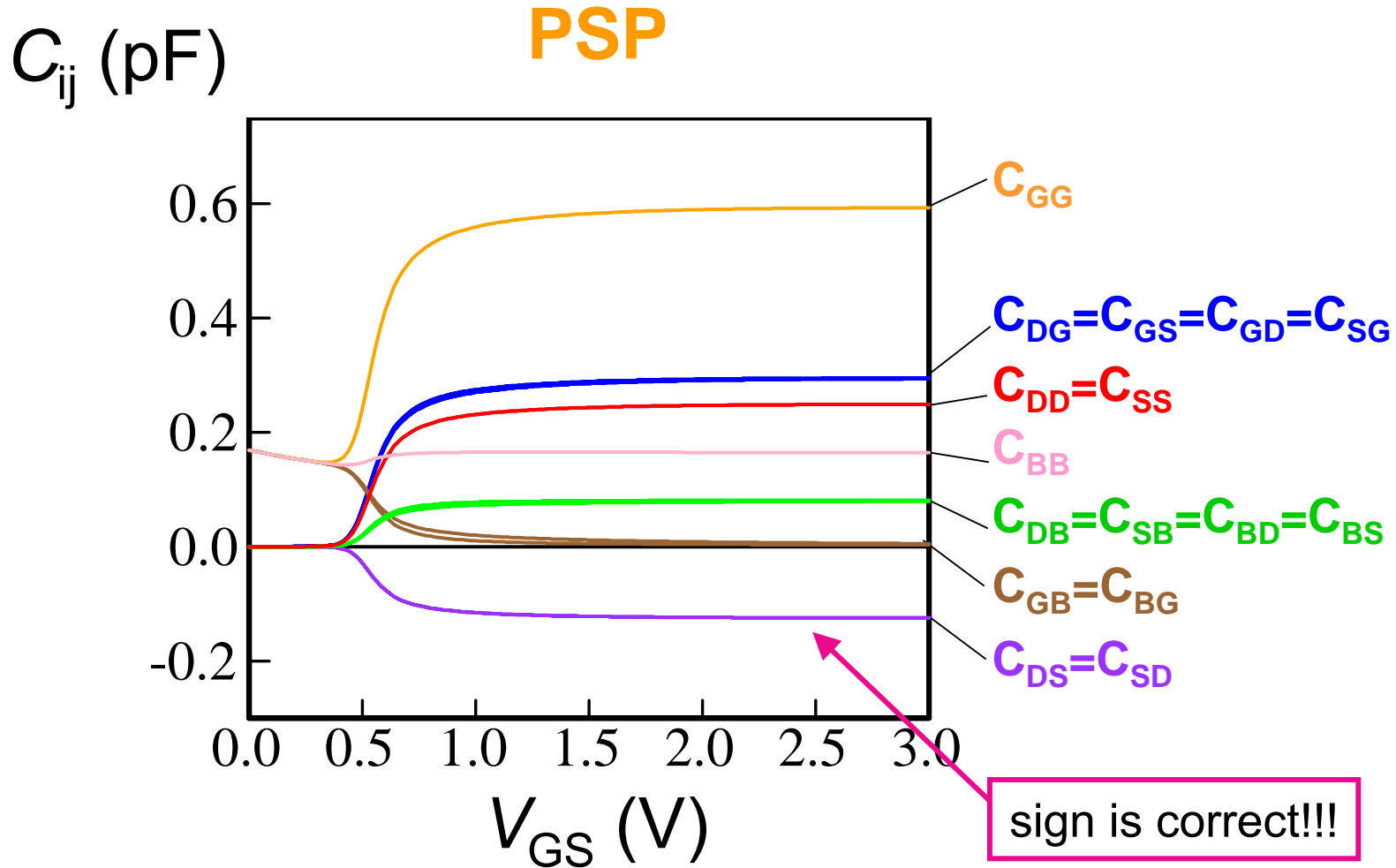
$$C_{ij} = C_{ji}$$

physics: 7 different  
capacitance values  
at  $V_{DS}=0V$

$C_{DD}$	$C_{DG}$	$C_{DS}$	$C_{DB}$
$C_{GD}$	$C_{GG}$	$C_{GS}$	$C_{GB}$
$C_{SD}$	$C_{SG}$	$C_{SS}$	$C_{SB}$
$C_{BD}$	$C_{BG}$	$C_{BS}$	$C_{BB}$

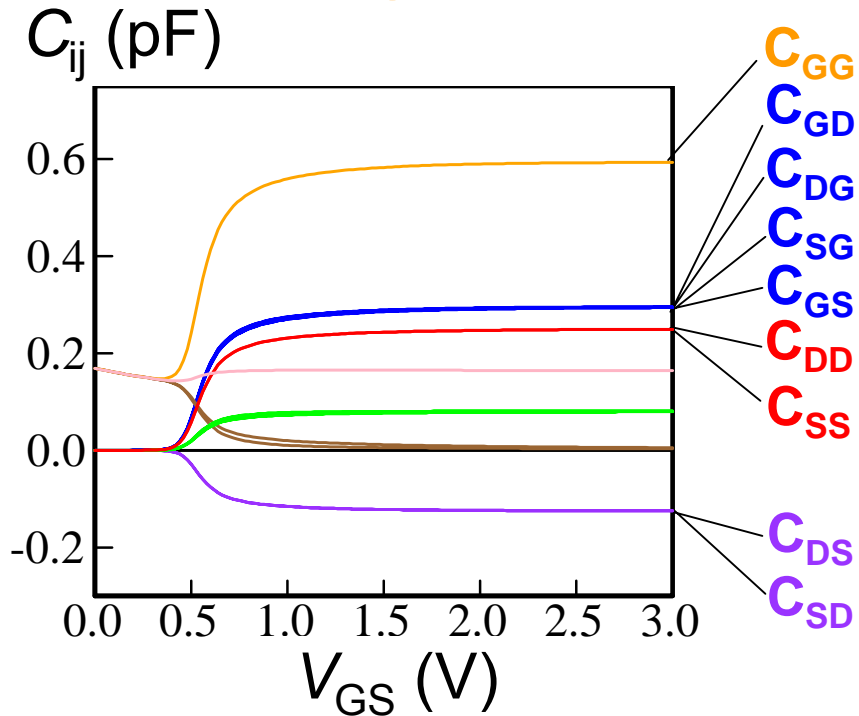


# capacitances at $V_{DS}=0V$

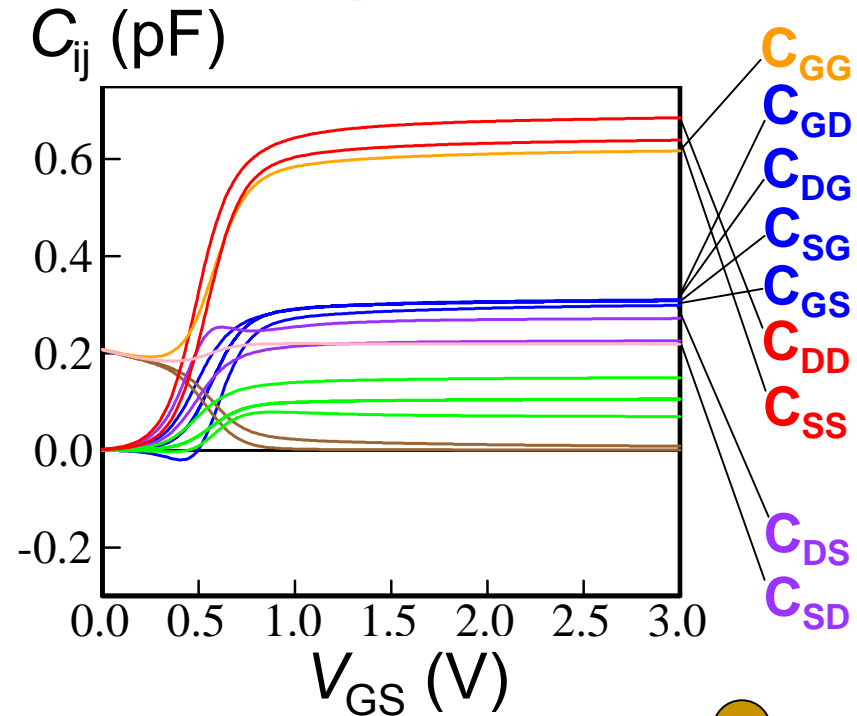


# capacitances at $V_{DS}=0V$

## PSP



## BSIM4

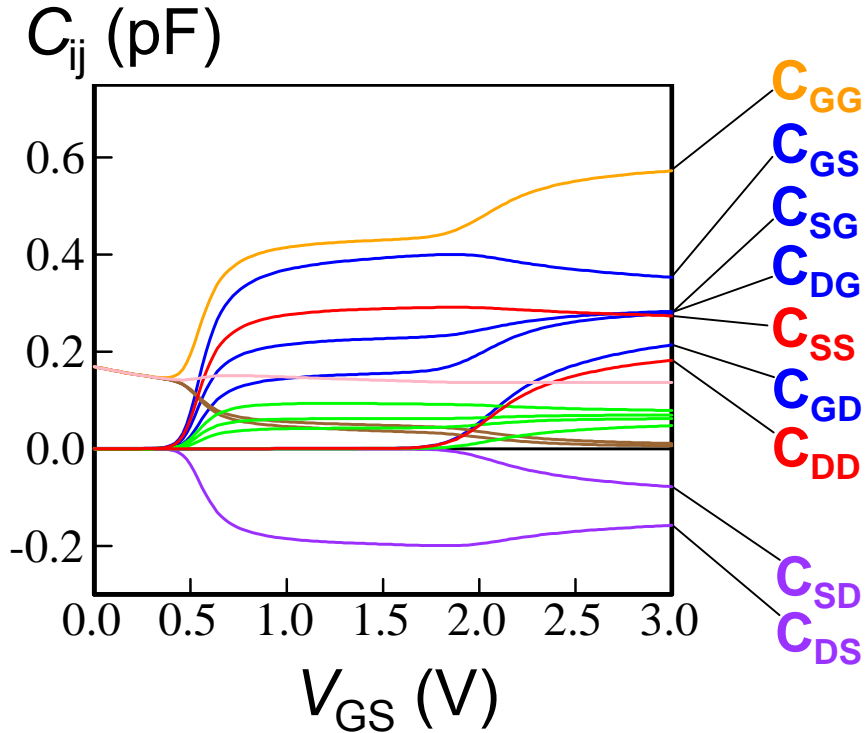


### BSIM4:

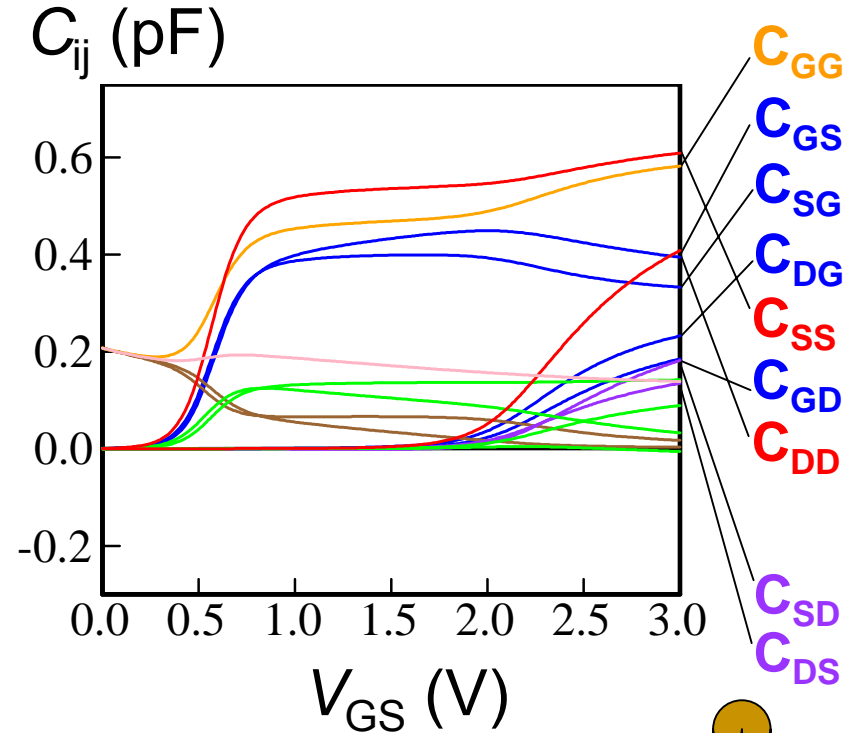
- symmetry and reciprocity are not satisfied
- sign of  $C_{SD}$  and  $C_{DS}$  incorrect
- $C_{DD}$  and  $C_{SS}$  exceeding  $C_{GG}$

# capacitances at $V_{DS}=1V$

## PSP



## BSIM4



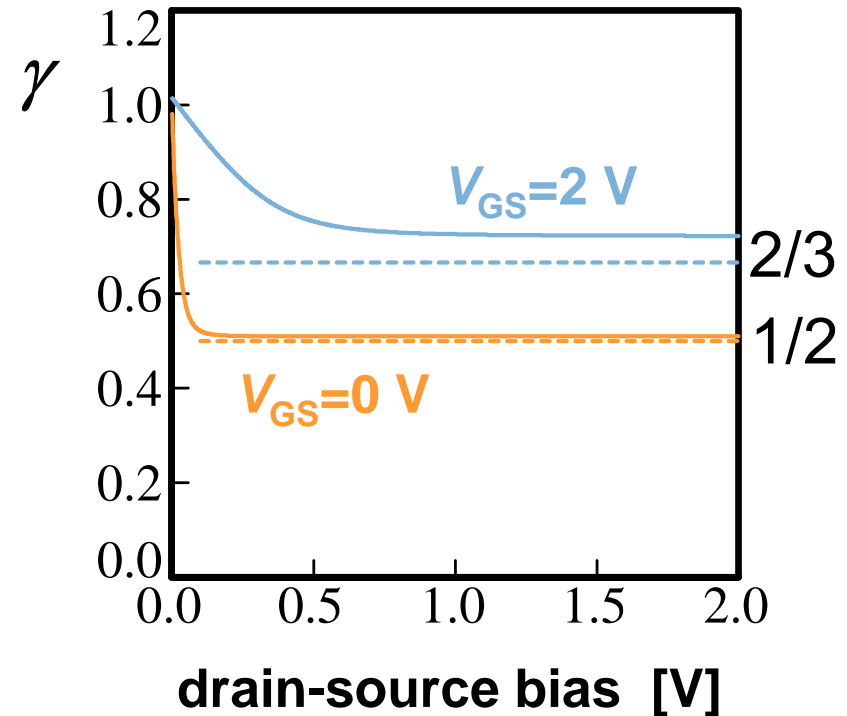
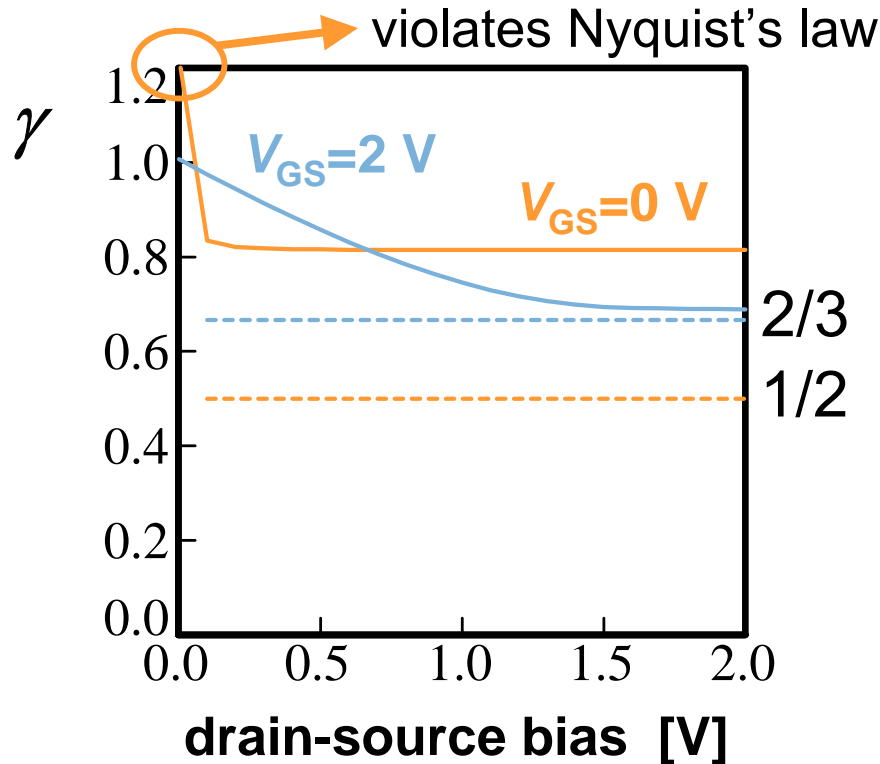
### BSIM4:

- sign of  $C_{SD}$  and  $C_{DS}$  incorrect
- $C_{SS}$  exceeding  $C_{GG}$
- $C_{DD}$  too large

# thermal noise and induced gate noise

white – noise gamma factor :  $\gamma = \frac{S_{id}}{4 \cdot k_B \cdot T \cdot g_{DS0}}$

$\gamma$	$V_{DS}=0V$	saturation
strong inversion	1	$\sim 2/3$
subthreshold	1	1/2



**BSIM4: incorrect**

**PSP: correct behavior**

# contents

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- ▶ recent model additions
- ▶ simulation time & JUNCAP Express
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# new in PSP102.2.0 w.r.t. PSP102.1.1:

- ▶ JUNCAP Express: see next part of this presentation
- ▶ WPE model added: CMC standard model
- ▶ dielectric constant now a parameter:  
leads to more physical modelling of capacitance and tunneling current in high-k dielectric
- ▶ addition of DELVTO (threshold voltage shift) and FACTUO (zero-field mobility factor): useful for user-defined additions
  - matching
  - corner modelling
  - layout dependent effects
  - ...
- ▶ NF support: number of fingers, including stress effect

# new in PSP102.2.0 w.r.t. PSP102.1.1:

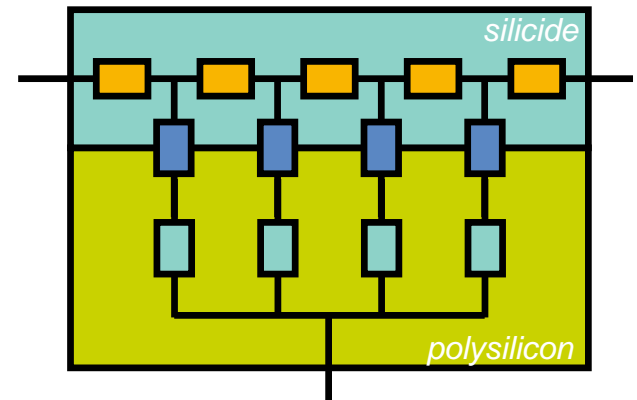
## ▶ gate resistance model added:

### – several components

- distributed silicide resistance 
- silicide-to-polysilicon interface resistance 
- vertical poly resistance 

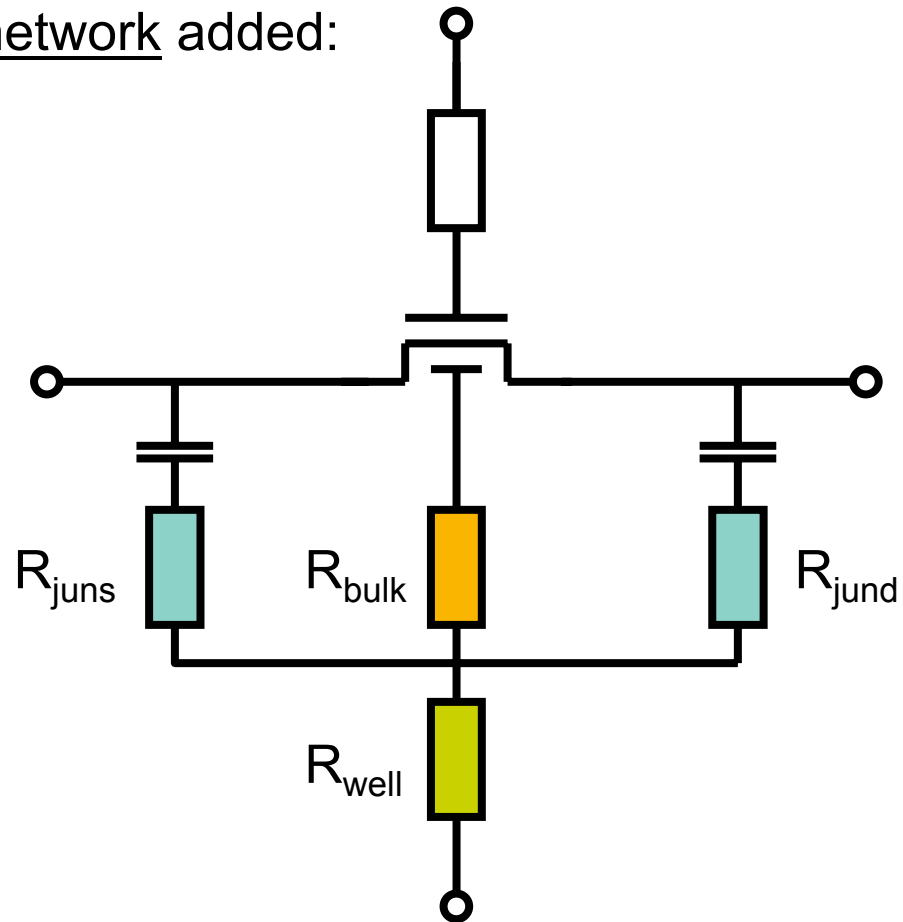
### – implementation in C-code with optional internal node

- can be switched off for, e.g., digital design → no additional internal node
- provides easy way to satisfy the needs of both RF and digital circuit designers



# new in PSP102.2.0 w.r.t. PSP102.1.1:

- ▶ optional bulk resistance network added:





# source code PSP102.2.0

- ▶ VA-code available at [http://pspmodel.asu.edu/psp\\_code.htm](http://pspmodel.asu.edu/psp_code.htm)
- ▶ C-code (SiMKit 3.0.3) available at [http://www.nxp.com/models/mos\\_models/psp/](http://www.nxp.com/models/mos_models/psp/)

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- ▶ why PSP? (recap)
- ▶ recent model additions
- ▶ **simulation time & JUNCAP Express**
- ▶ upcoming model updates

# background and general idea

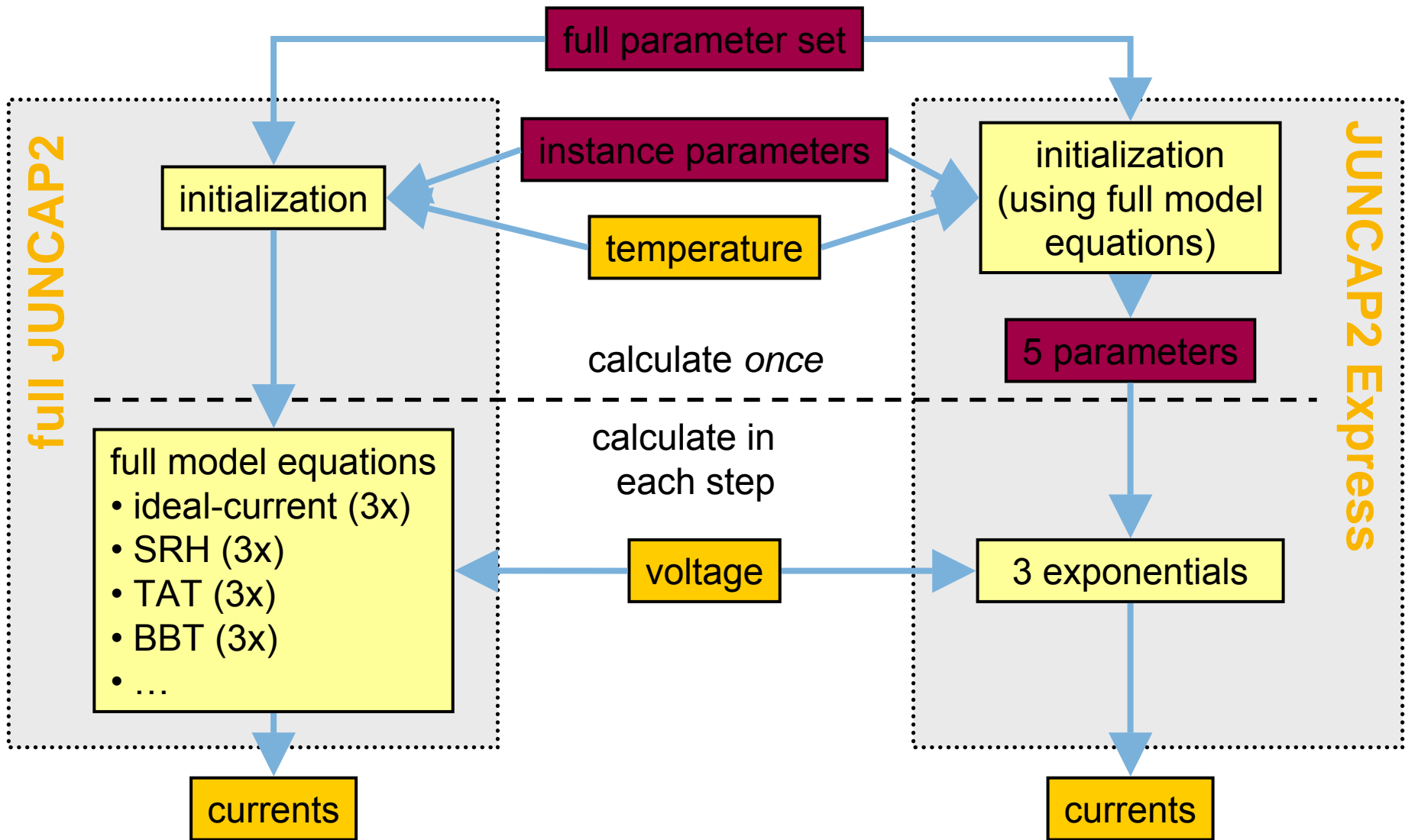
## ▶ background

- JUNCAP2 gives a very accurate description of junction currents and capacitances
- well-defined and physics-based extraction strategy
- model evaluation time is significant, while full accuracy is not always required

## ▶ general idea

- generic method to reduce simulation time for less demanding applications
- no additional characterization/parameter extraction needed (full model parameter set is used)
- can be invoked by simple switch
- requires no insight in which components of junction current are important

# flow chart



# special function count

for *currents* (voltage-dependent section of model)

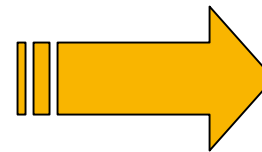
## JUNCAP2

	exp	sqrt	ln	pow
ideal	1			
SRH		4	2	1
TAT	1	4		1
BBT	1			1
breakdown		1		1
subtotal	3	9	2	4
total (3 comp)	9	27	6	12

Note:

- these numbers are *maxima*
- actual numbers depend on parameter set
- typical parameter set: less than 50%

## JUNCAP2 Express



	exp
total	3

Note:

- these numbers are independent of parameter set

# model equations

- ▶ model for currents is replaced by very simple equation (sum of three exponentials)
- ▶ **only five parameters**
  - automatically computed during model initialization
  - from full parameter set, using full JUNCAP2 model

$$I(V) = \underbrace{I_{for,1} \cdot [\exp(V / \varphi_T) - 1]}_{\text{ideal forward current}} + \underbrace{I_{for,2} \cdot [\exp(V \cdot m_{for,2} / \varphi_T) - 1]}_{\text{non-ideal forward current}} - \underbrace{I_{rev} \cdot [\exp(-V \cdot m_{rev} / \varphi_T) - 1]}_{\text{non-ideal reverse current}}$$

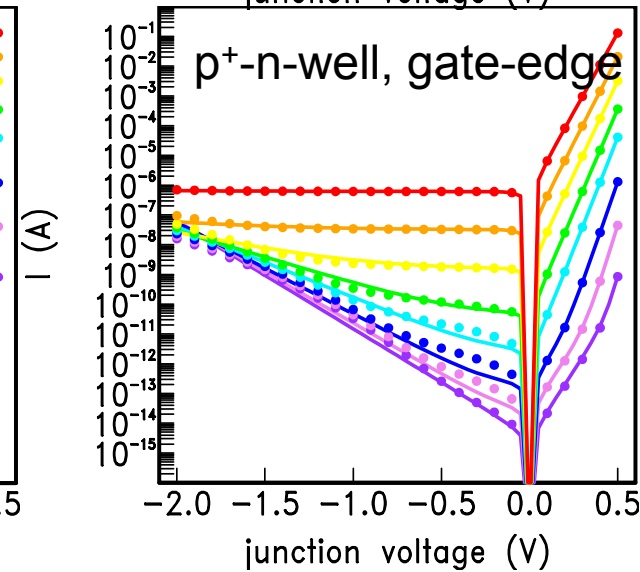
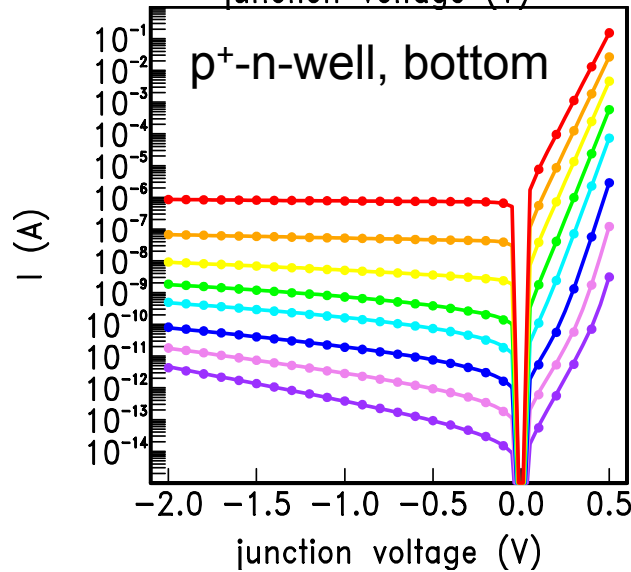
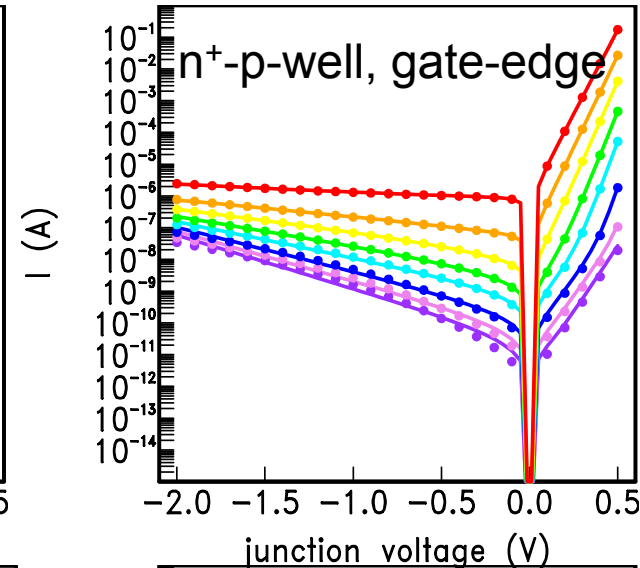
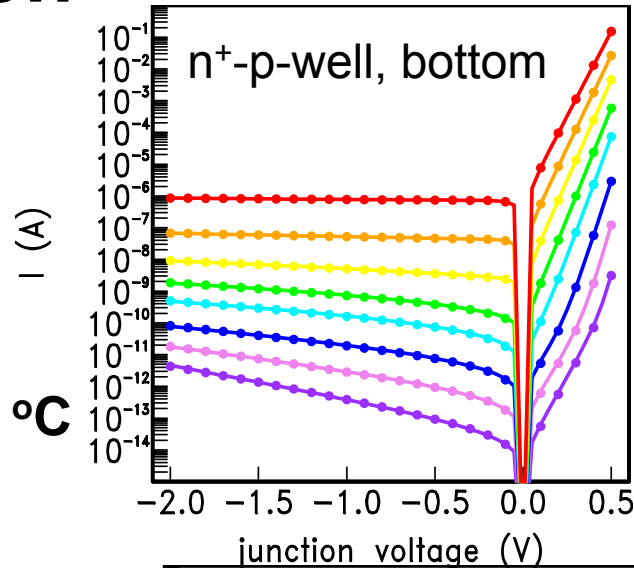
- ▶ guaranteed to be continuous and smooth

# model validation

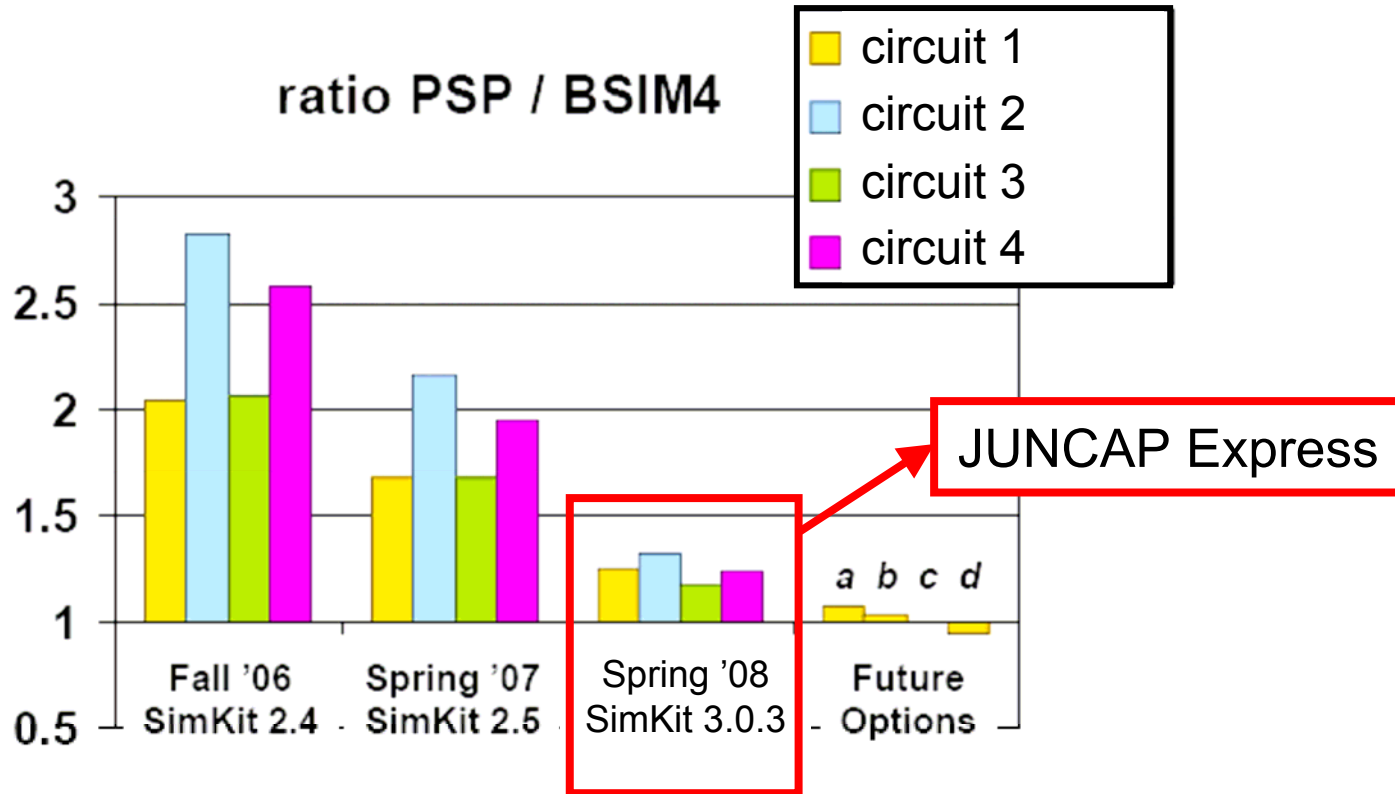
- ▶ Process 1
- ▶  $V_{JUNREF} = 2V$
- ▶  $T = -40, -10, 21, 60, 90, 125, 160, 200$  °C

symbols:  
full JUNCAP2

lines:  
JUNCAP2 Express



# simulation speed improvement



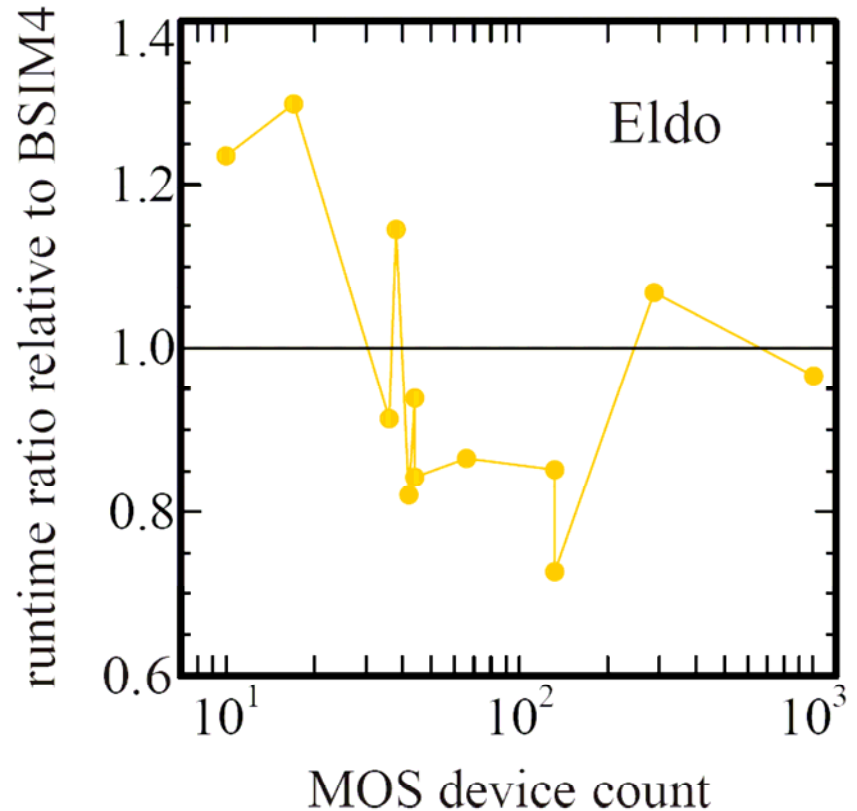
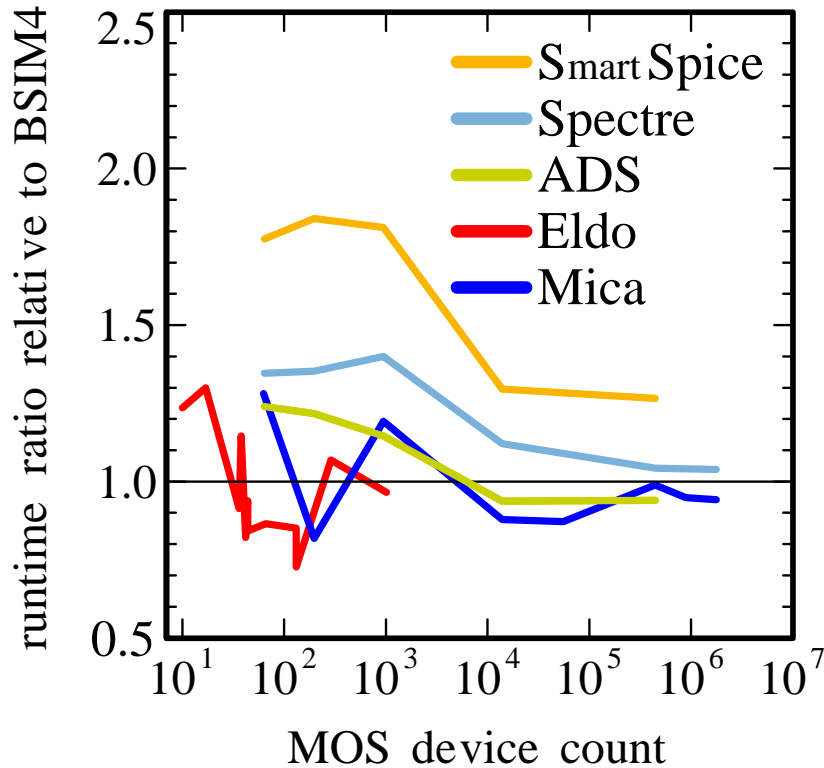


# a note on large circuits (i)

- ▶ there have been claims that the simulation time ratio PSP vs. BSIM4 would become progressively worse when going to large circuits
  - Simucad, on their website
  - Simucad, WCM publication (not peer reviewed!)
  - HiSIM team, at the MOS-AK 2007
- ▶ all experts on circuit simulation know that evaluation time differences become *less* important for larger transistor count
- ▶ claims like this originate from comparing circuit simulations with randomly chosen parameter sets for different models
- ▶ instead, one should use parameter sets that match well
- ▶ for details:  
[http://www.geia.org/GEIA/files/ccLibraryFiles/Filename/000000003516/NXP\\_runtimes.pdf](http://www.geia.org/GEIA/files/ccLibraryFiles/Filename/000000003516/NXP_runtimes.pdf)

# a note on large circuits (ii)

- ▶ when investigation is carried out properly, the results make sense:



# contents

- ▶ why PSP? (recap)
- ▶ recent model additions
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- ▶ **upcoming model updates**

# new in PSP102.3.0 w.r.t. PSP102.2.0:

- ▶ asymmetric MOS: separate source/drain parameters for
  - junctions
  - GIDL
  - overlap capacitance
  - overlap gate current
- ▶ non-unity slope EF in flicker noise
- ▶ will be available in SiMKit 3.1 (May '08)

