

MOS-AK

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Scalable high-frequency modelling with EKV3



Matthias Bucher

Technical University of Crete, Chania, Greece



Antonios Bazigos

National Technical University of Athens, Athens, Greece

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- ❖ EKV3 model Team:
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- ❖ EDA support:
 - Mentor Graphics, Dolphin Integration, Cadence

Outline

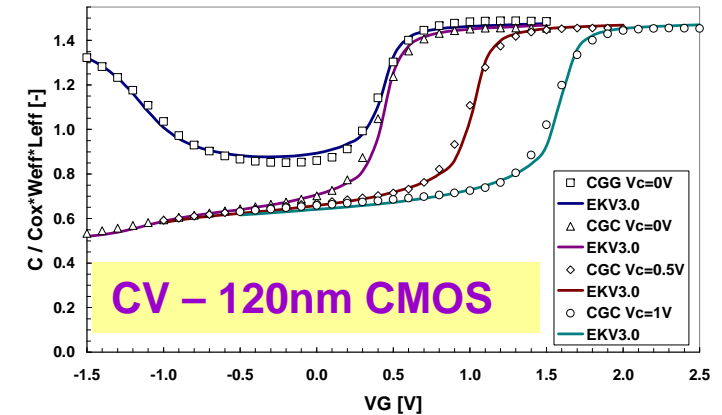
- ❖ Introduction
- ❖ EKV3 compact MOSFET model
- ❖ RF measurements in advanced RFCMOS
 - 180nm RF CMOS
 - 110nm RF CMOS
 - 90nm RF CMOS
- ❖ Conclusions

Introduction

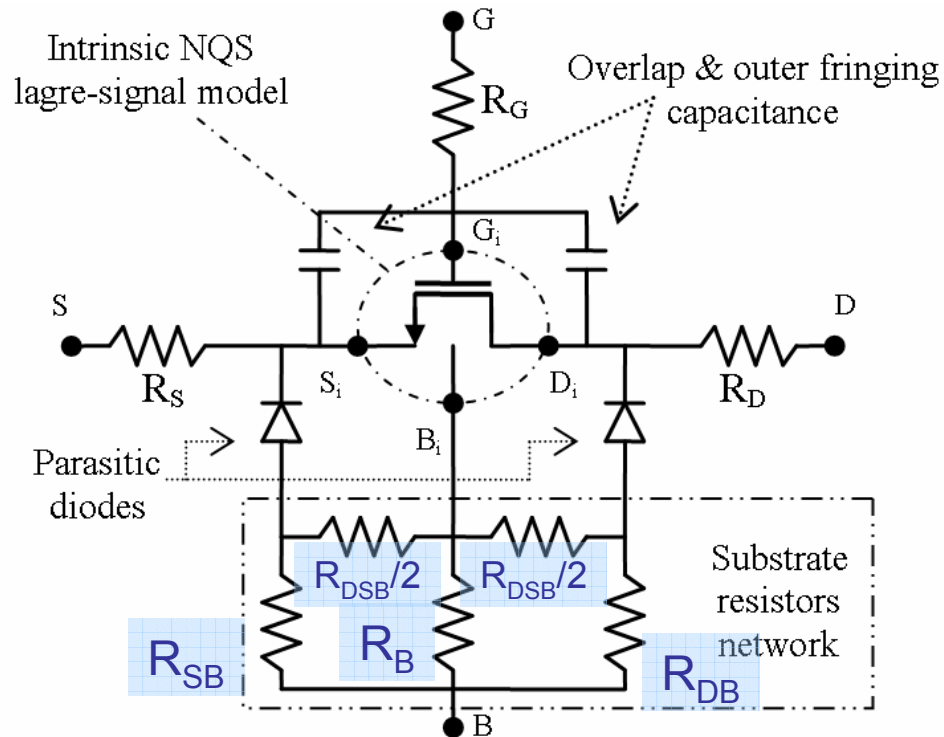
- ❖ Si CMOS is mainstream technology
 - Low-cost, “Best nano-scale technology!” (S. Cristoloveanu)
 - RF front ends compatible with large-scale digital circuits (SoC)
- ❖ Many RF applications in multi-GHz range
 - Efficient design demands efficient compact models in circuit simulators
 - High requirements in terms of RF characterization
- ❖ Analog RF design relies on compact, scalable MOSFET models
 - Physics based model
 - Covering all effects to 65nm CMOS
 - Model should cover all high-frequency aspects (RF Noise!)
 - L, W, Temperature, frequency, statistics.....
 - Multi-finger RF MOSFETs – Layout dependence
- ❖ EKV3 Compact MOSFET model for Analog/RF IC Design

EKV3 MOSFET compact model

- ❖ **Physics Based Charges Model**
 - ❑ Inversion charge linearization
 - ❑ Same parameters as surface potential model
 - ❑ Preserves the essence of a surface potential model.
- ❖ **Extensions for CV:**
 - ❑ Polydepletion, Quantum effects
 - ❑ Bias-dependent Overlap & fringing capacitance
- ❖ **Extensions of IV:**
 - ❑ DIBL, Charge sharing, RSCE, Halo doping
 - ❑ Charge-based vertical field mobility
 - ❑ Charge-based velocity saturation, CLM
 - ❑ Gate tunnelling
- ❖ **Non-quasi-static (NQS) modelling**
- ❖ **Noise modelling:**
 - ❑ 1/f noise, Induced Gate Noise, enh. Short-channel thermal noise
- ❖ **Parameter count: ca. 140**
- ❖ **Implementation: Verilog-AMS Code**
 - ❑ Available in: ELDO (Mentor) , Smash (Dolphin), Spectre (Cadence)



EKV3 model for RF

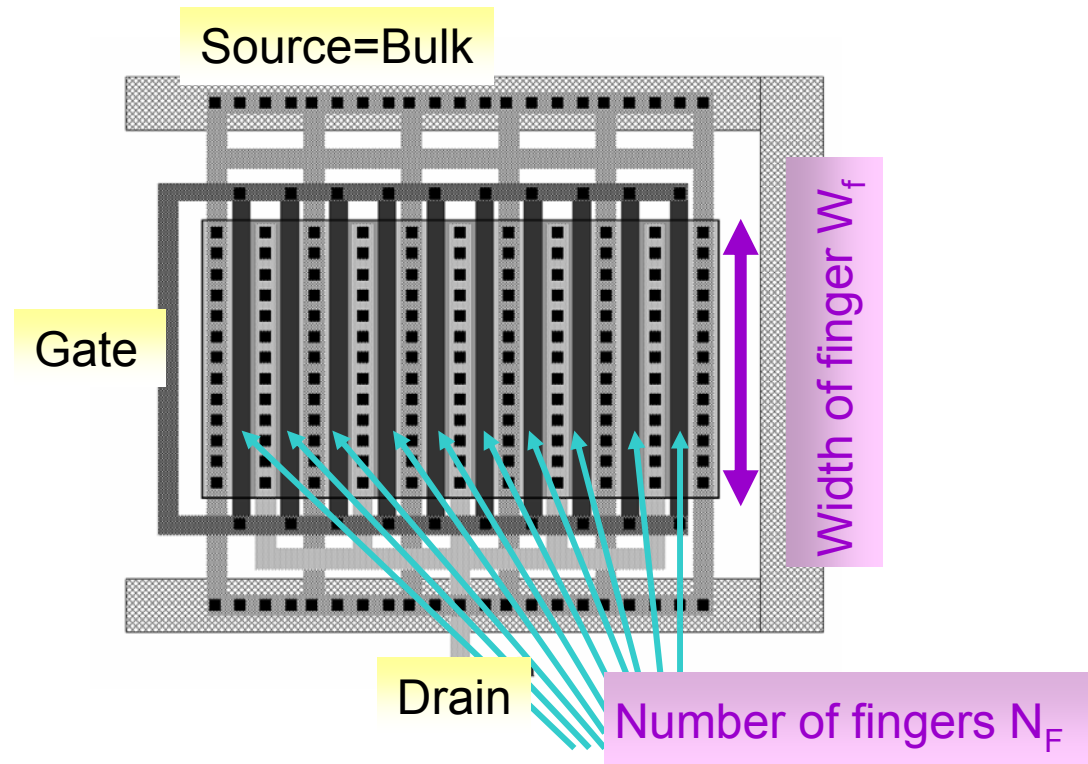


- ❖ Non quasi-static model (NQS)
 - ❑ channel segmentation
 - ❑ consistent AC/transient

- ❖ Gate- and substrate- parasitics scale with multi-finger layout

R_G	$\sim W_f / (L * N_F)$
R_{SB}, R_{DB}	$\sim 1 / W_f$
R_B	$\sim 1 / W_f$
R_{DSB}	$\sim L / (W_f * N_F)$

Multi-finger RF MOSFETs

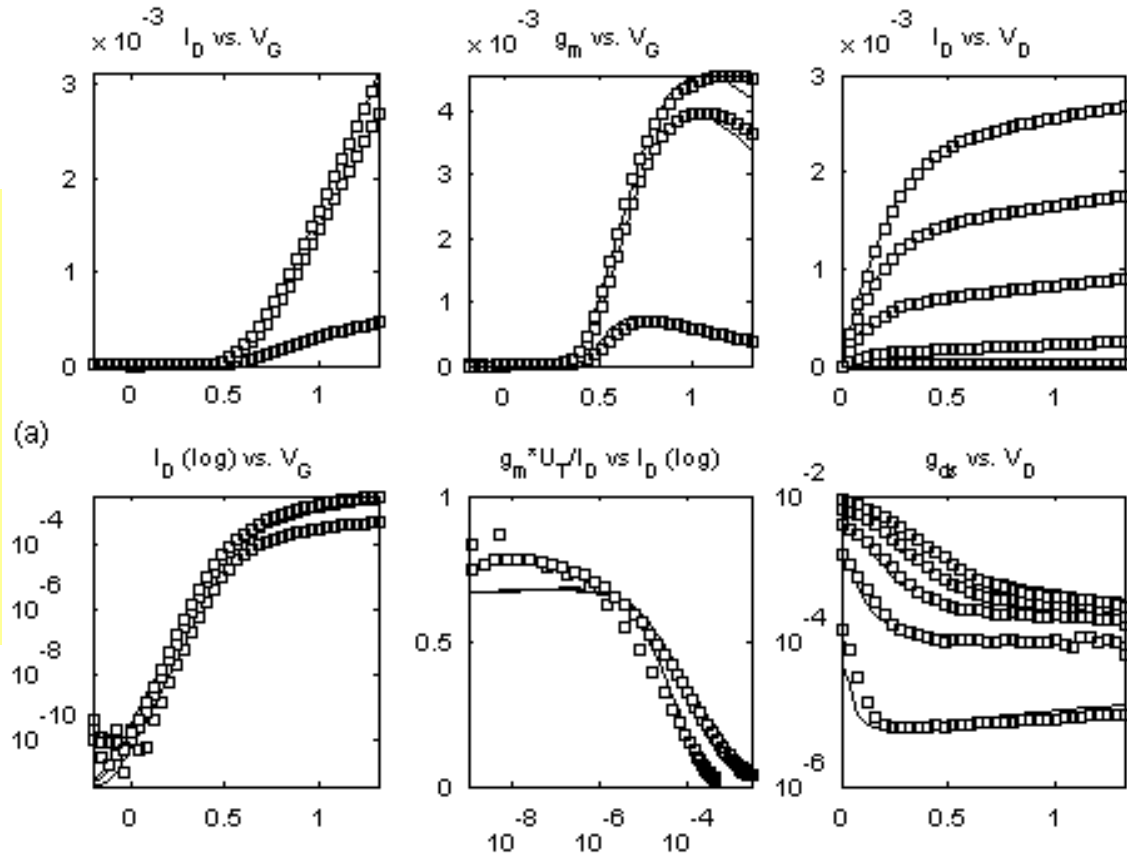


- ❖ Layout of RF multi-finger MOSFET
 - ❑ Number of fingers – N_F (1-50), can be odd or even
 - ❑ Finger Width – W_f (0.5-5 μ m)
 - ❑ Gate Length – L
 - ❑ Single- or both-sided gate contacts
 - ❑ Layout-dependent stress: Active area to shallow trench isolation (STI)

Static characteristics – 180nm CMOS

$V_{DS}=50m, 0.5, 1V$

$V_{GS}=0.4, 0.6, 0.8, 1, 1.2V$



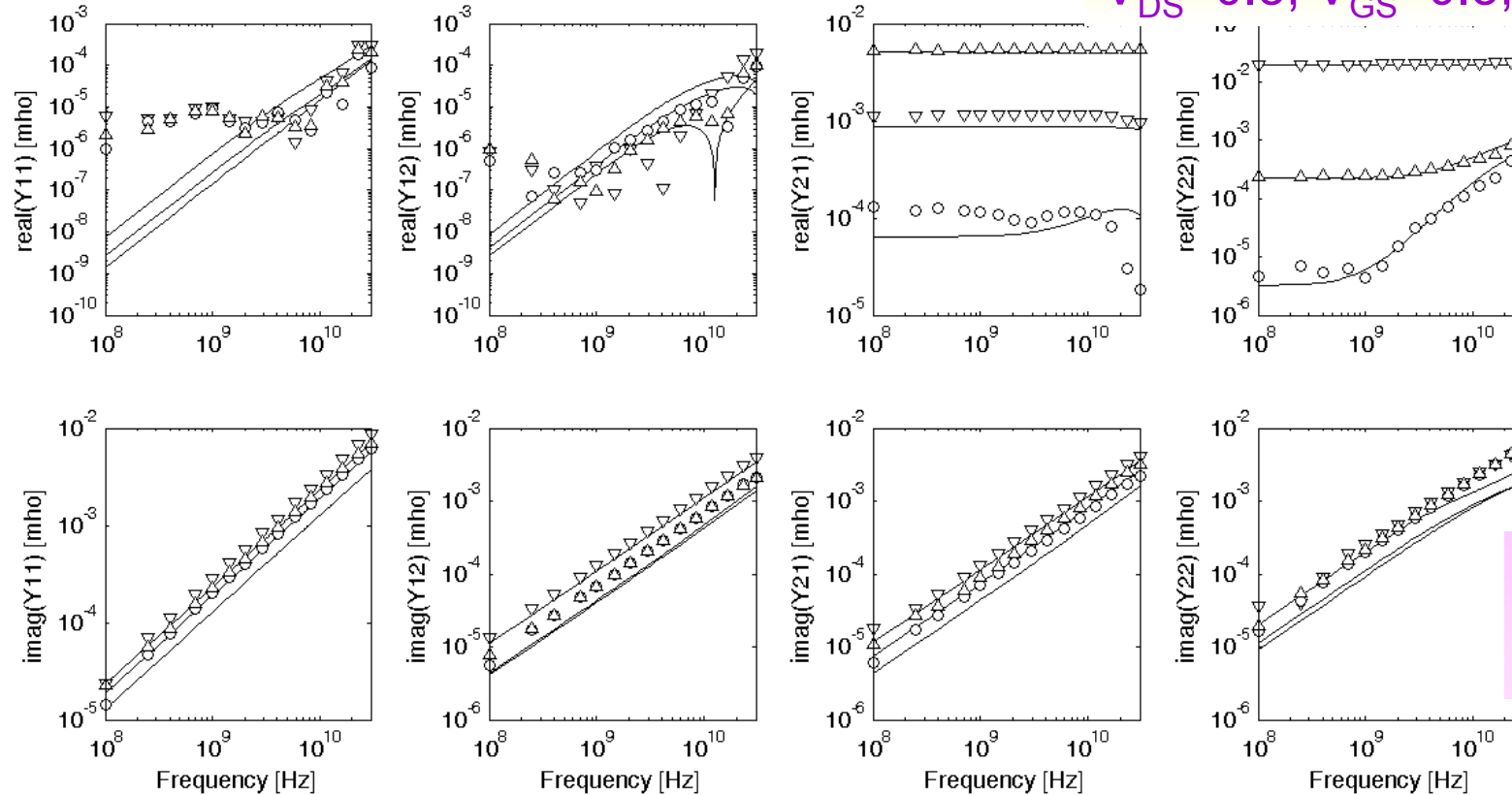
— EKV3
□ meas.

Bazigos e.a., Micro&Nano 2007

- ❖ NMOS, $L=180nm$, $W_f=2\mu m$, $N_F=4$
- ❖ I_D-V_G , g_m-V_G , $g_m \cdot U_T / I_D - I_D$
- ❖ I_D-V_D , $g_{ds}-V_D$

Y-parameters – 180nm CMOS

$V_{DS}=0.3, V_{GS}=0.3, 0.6, 1.2V$



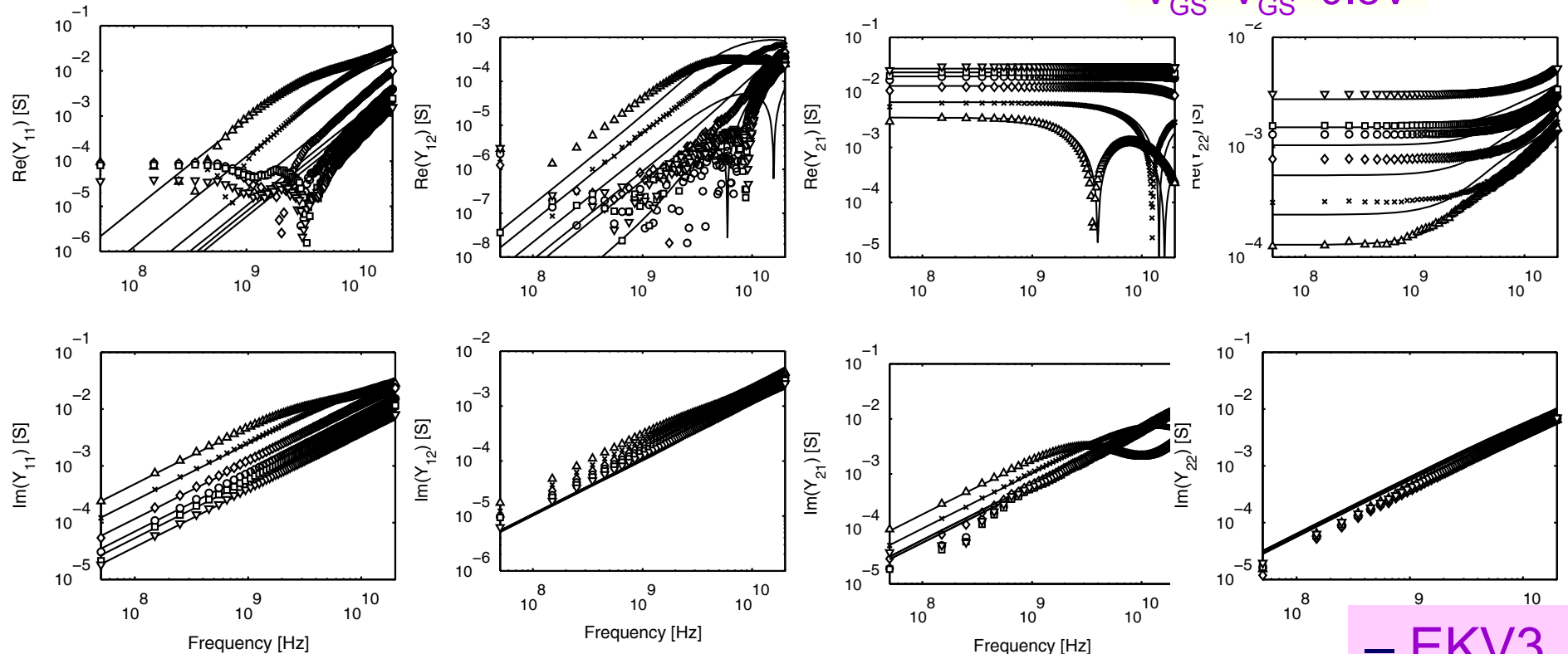
— EKV3
□ meas.

- ❖ Real & Imaginary 2-port Y-parameters up to 30GHz
- ❖ NMOS, $L=180\text{nm}$, $W_f=2\mu\text{m}$, $N_F=9$

Bazigos e.a., Micro&Nano 2007

Scaling of Y parameters vs. L – 110nm CMOS

$V_{GS} = V_{DS} = 0.8V$



— EKV3
 □ meas.

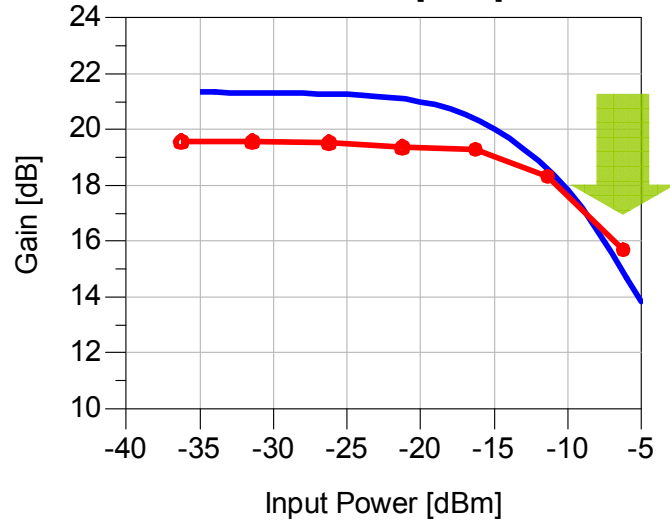
❖ NMOS, L=110nm ... 2μm, $W_f=2\mu m$, $N_F=40$

Bucher e.a., RFMiCAE 2008

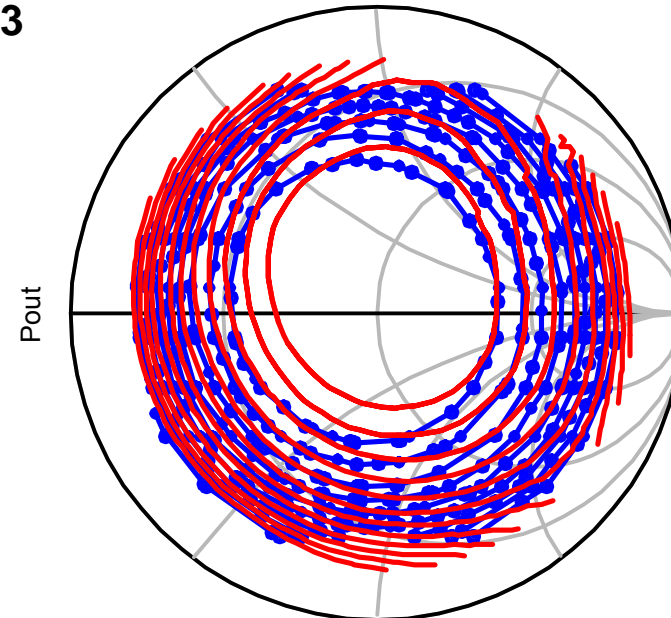
Large signal verification at RF – 110nm CMOS

Yoshitomi, MIXDES 2005

Gain at 50Ω load vs Input power



— Measured
— EKV3



$L_g=110\text{nm}$, $W_f=5.2\mu\text{m}$, $N_F=12$

freq = 2.45 GHz

$V_{GS}=0.9\text{V}$, $V_{DS}=1\text{V}$

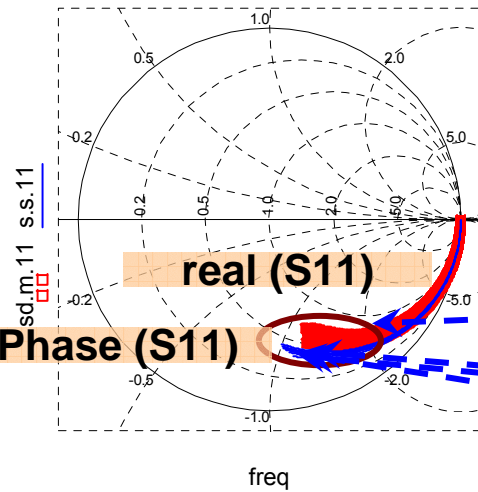
indep(Pdel_contours_p) (0.000 to 60.000)
IndexPoutdBm (1.000 to 234.000)

Gain range 3dB...8.5dB
Gain contour @ Pin = -6dBm

- ❖ Gain compression & gain contour plots at given bias & geometry

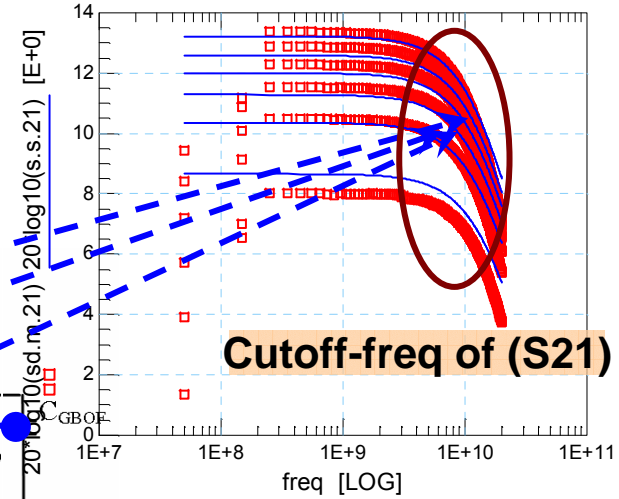
S parameters – 90nm CMOS

Plot H_NVS_Lp07W2N40/RF_dut/spar_vg0p4/s11

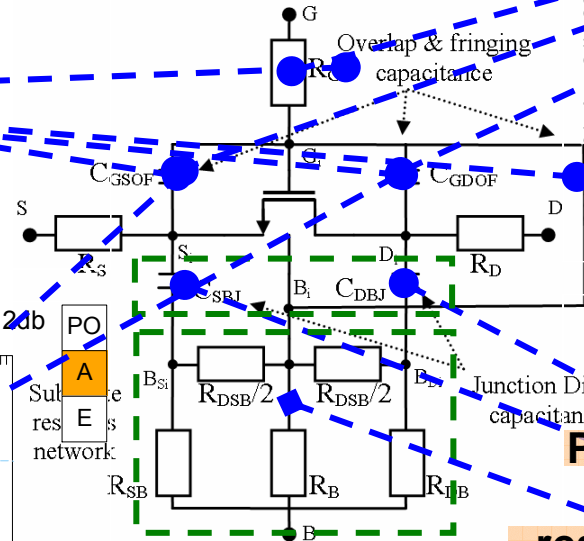


A
E

Plot H_NVS_Lp07W2N40/RF_dut/spar_vg0p4/s21db

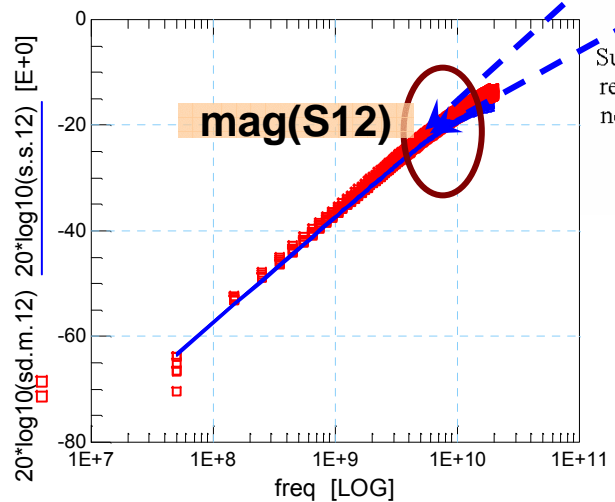


PO
A
E



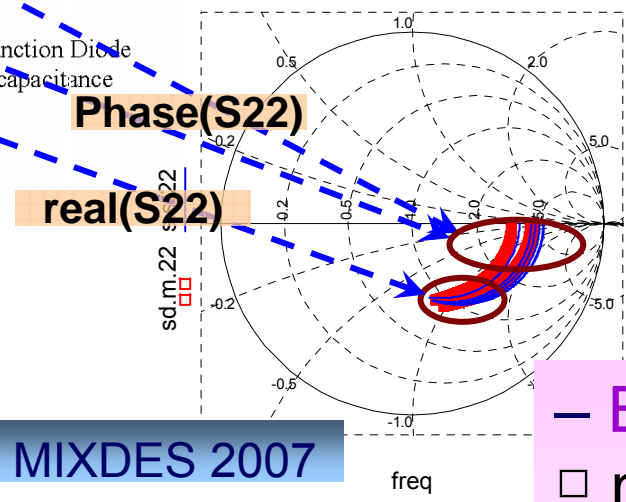
X
Y

Plot H_NVS_Lp07W2N40/RF_dut/spar_vg0p4/s12db



PO
A
E

Plot H_NVS_Lp07W2N40/RF_dut/spar_vg0p4/s22



A
E

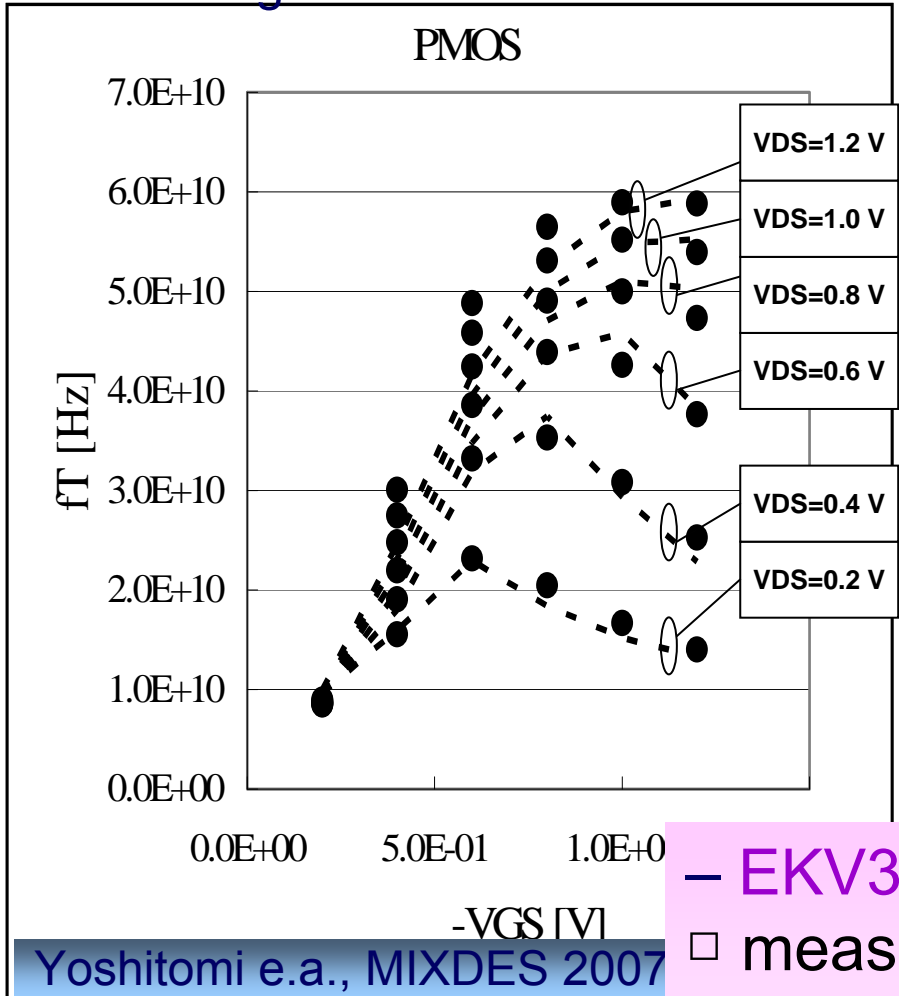
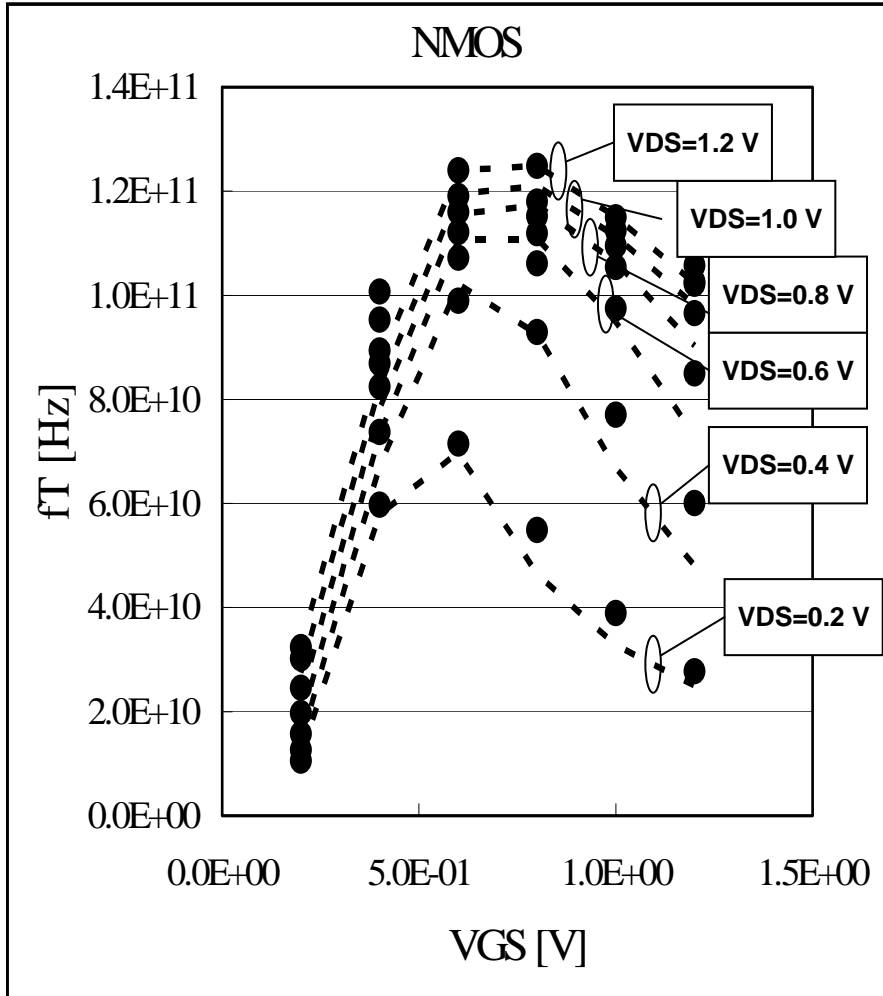
Yoshitomi e.a., MIXDES 2007

– EKV3
□ meas.

Transit frequency f_T vs. V_{GS} , V_{DS} – 90nm CMOS

● Measurement
 - - - - EKV3

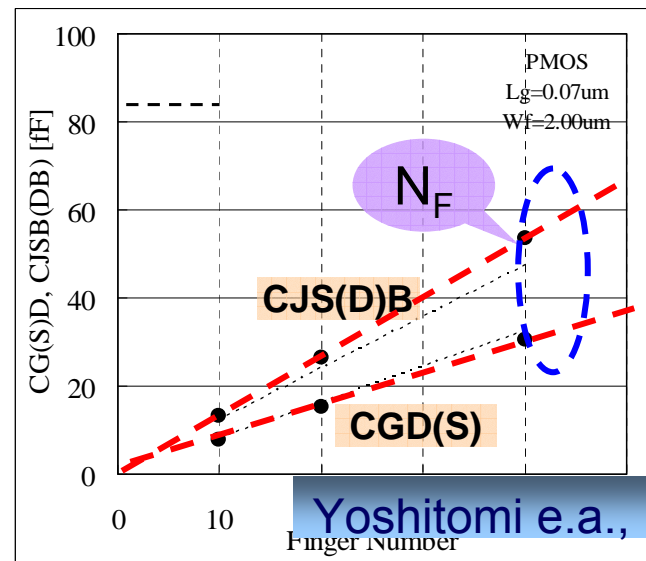
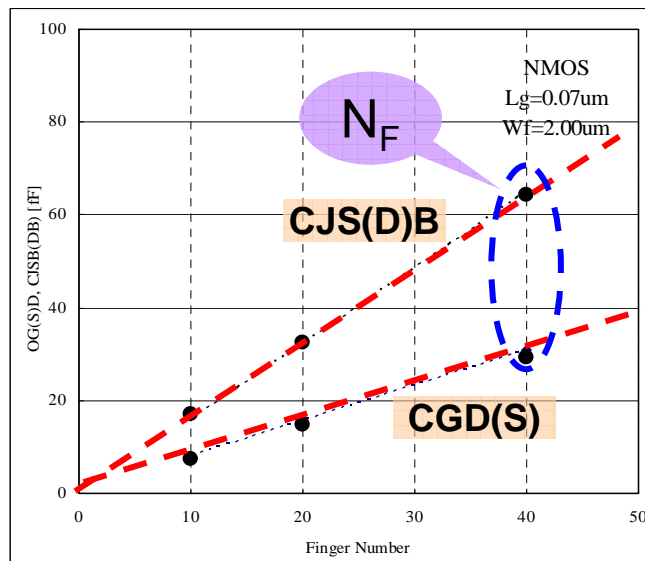
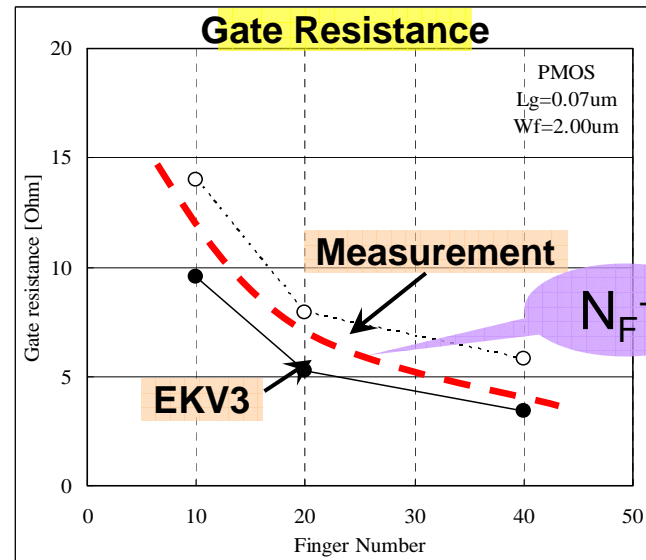
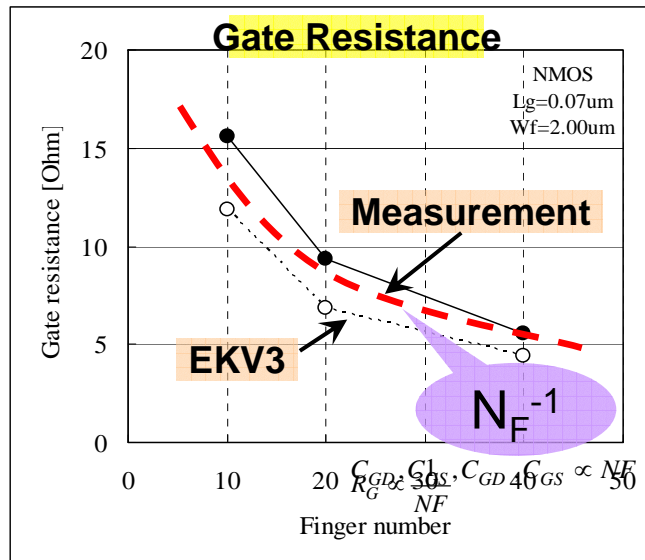
$L_g=70\text{nm}$ $W_f=2\mu\text{m}$ $N_F=10$



Yoshitomi e.a., MIXDES 2007

— EKV3
 □ meas.

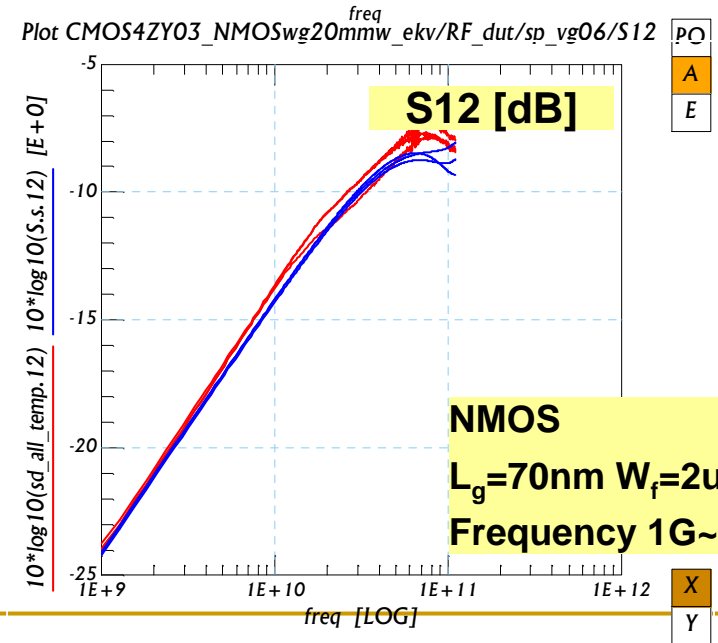
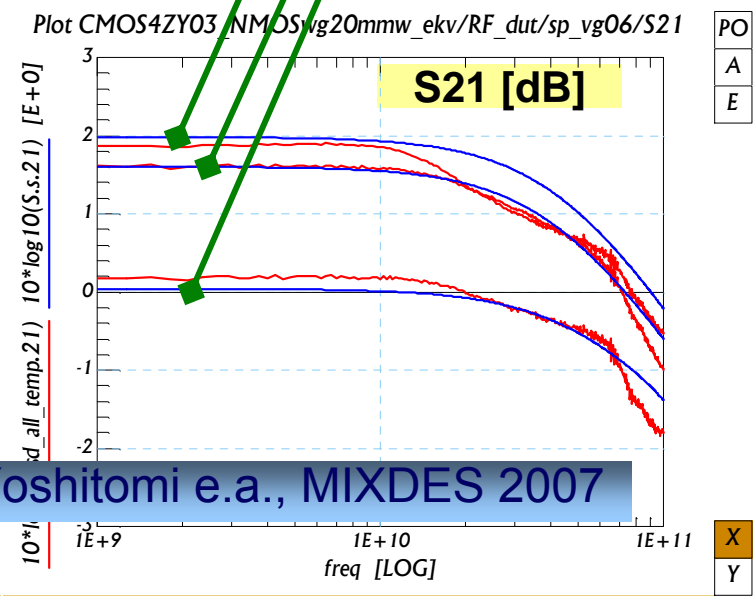
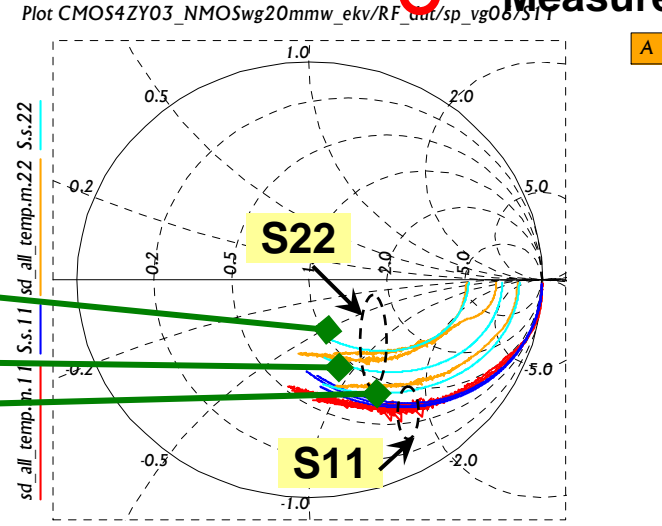
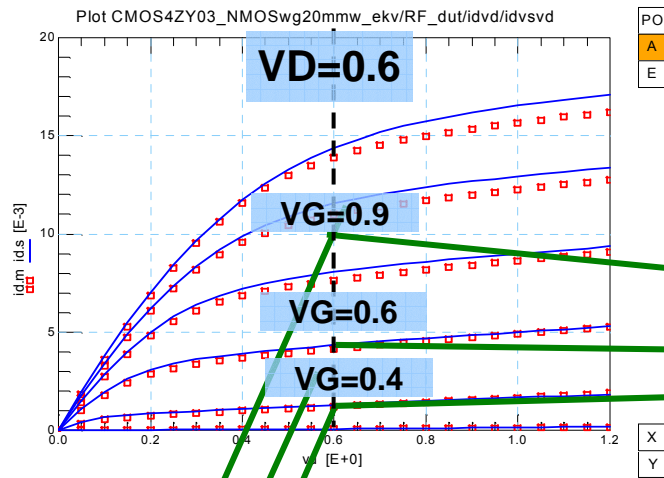
RF-Scalability vs. Number of fingers



Yoshitomi e.a., MIXDES 2007

EKV3 for mm-Wave design

— EKV3 NQS Mode
 ○ Measurement



Yoshitomi e.a., MIXDES 2007

NMOS
 $L_g=70\text{nm}$ $W_f=2\mu\text{m}$ $N_F=10$
 Frequency 1G~110GHz

Conclusions

- ❖ EKV3 RF scalable model has been extensively validated
 - 180nm CMOS
 - 110nm CMOS
 - 90nm CMOS

- ❖ EKV3: a design-oriented, charge-based, compact model for analog/RF IC design.
 - EKV301.01 Verilog-AMS code released 23 November, 2007.
 - Standard model implementations
 - ELDO (Mentor)
 - Smash (Dolphin)
 - Spectre (Cadence)
 - AdMOS EKV3 parameter extraction automated toolkit for IC-CAP.

- ❖ EKV3 ongoing developments:
 - Extended 1/f noise model
 - Extended model for short-channel effects in HF noise

Reference

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- ❖ Contact: Prof. Matthias Bucher
Dept. of Electronics and Computer Engineering
Technical University of Crete (TUC)
73100 Chania, GREECE
Phone/fax: +30 28210 37210 / 37542
Email: bucher@electronics.tuc.gr
web: <http://www.rfic.tuc.gr>