A CMOS technology and its characterization in ITE

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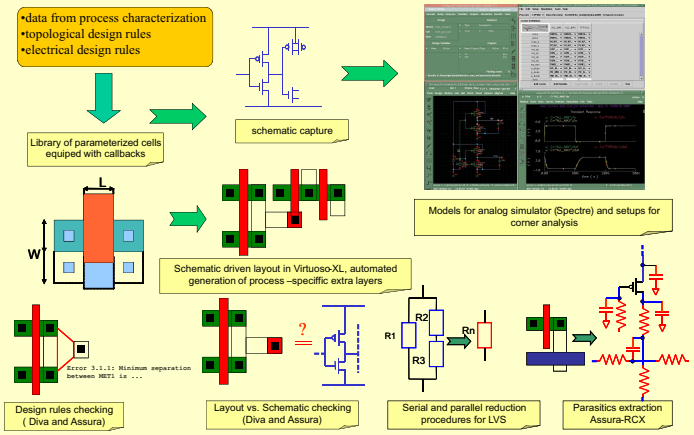
CMOS technology; design kit development

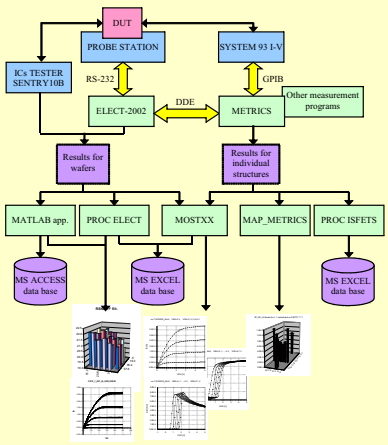
The main features of the CMOS technology available at ITE are as follows: 3μm feature size, single p-well, single poly-Si level, two metal levels.

The technology is offered to the academic laboratories within a multi-project-wafer (MPW) service. For this purpose a design kit for the CADENCE design system has been developed. At present it offers the following main functionalities, e.g. DRC, extraction and LVS for Diva and Assura, Assura-RCX, Virtuoso-XL support, analog environment for Spectre with corners, and GDSII and CIF import / export.



Characterization system

MATLAB application for processing of the measurement data generated by the 93 I-V system. Simple models implemented. On-wafer distributions of basic parameters, simple statistics



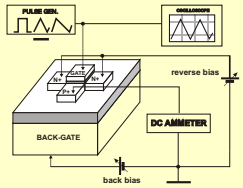
PROC_ELECT for processing of data measured on CMOS test structures or ISFET-type test elements using the ELECT-2002/METRICS system (on-wafer distributions of basic parameters, their simple statistics)

MOSTXX for extraction of MOSFETs and P-N junctions models parameters (a number of models, based on a number of linear and non-linear regression (optimization) methods, graphical visualization procedures)

MAP_METRICS for generation of maps and histograms of the electrical characteristics/parameters (useful in case of precise measurements of the individual devices (like p-n junctions), histograms of single data points of characteristics at the given bias can be plotted and compared)

The programs have been written in a MS EXCEL VBA environment

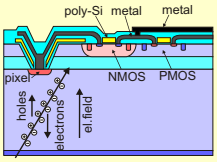
Charge-pumping method

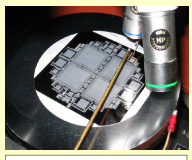


Charge-pumping (CP) is a very efficient tool for analyzing the quality of semiconductor-dielectric interface. IMiO has considerable experience in charge-pumping characterization of conventional and SOI MOSFETs, as well as other MOS structures (VMOS, SiGe channel, alternative gate dielectrics).

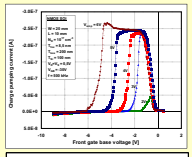
We have at our disposal a unique gate-signal generator for charge-pumping designed and built in IMiO. The generator allows for arbitrary shape of gate signal, which might come in useful if modification of standard CP measurements is required.

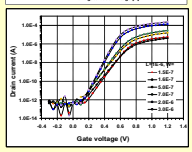
SOI activities





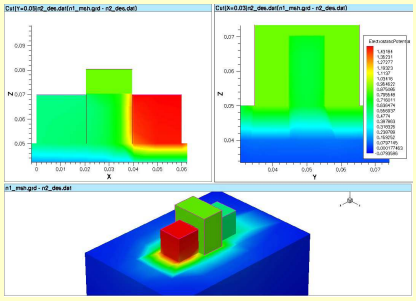
- Integration of SOI CMOS with fully depleted detectors of ionizing radiation (**SUCIMA** project - FP5)
- Implementation of a FD SOI CMOS technology developed in UCL (**TRIADE** project - FP7)
- Application of SOI substrates for MEMS, ISFETs manufacturing
- Measurements and characterization of SOI CMOS structures, MOSFETs SiGe, MOSFETs with SiON gate dielectric using the CP method
- Measurements of FinFETs (courtesy of dr. M.Jurczak - IMEC; within **SINANO** project); gathering experience in tha area of characterization
- Extensive numerical modelling of multi-gate MOSFETs and SiGe MOSFETs

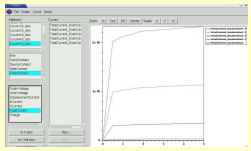


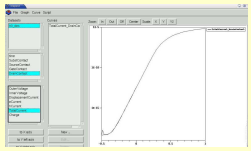


Numerical simulation of multi-gate MOSFETs

For the development of the processes and devices a set of simulation and characterization tools is used. The following packages are used: SILVACO, ISE-TCAD, COVENTOR, SEMulator3D, Matlab/Simulink. Particularly the DESSIS program (ISE-TCAD) seems to be a very powerful tool for the investigation of the dispersion in electrical characteristics of multi-gate MOS devices.



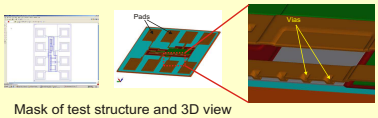




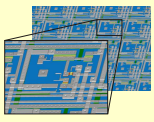
Emulation of CMOS fabrication processes

SEMulator3D tool includes procedures for emulation of the following processes:

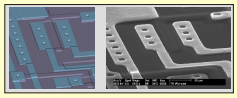
PVD, LPCVD, PECVD, Metal Lift-Off deposition, Epitaxial growth, Wafer bonding, Electrochemical deposition, RIE, Implantation etc.



Mask of test structure and 3D view



3D model of pixel detectors array



3D model of single pixel and SEM image of the structure

Conclusions

From the point of view of COMON needs ITE offers the facilities in the following areas:

- electrical measurements of multi-gate MOS SOI structures
- numerical simulations of complex processes and semiconductor devices
- development of MOS SOI device models and their use for characterization tasks
- development of characterization methods and methods for analysis of device characteristics variations
- design-kit development and implementation in the CADENCE environment

COMON "kick-off" meeting, Eindhoven, 3-4th April, 2008