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a leap ahead in analog

Quality of HiSIM_HV Model for Analog Circuit Design

MOS-AK Meeting, Frankfurt (Oder), Germany

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2-3 April 2009

a leap ahead
in Compact Modeling

Outline

- Introduction (HiSIM_HV 1.0.2)
- Model capabilities
- Geometry Scalability
- I-V results (Id-Vg, Id-Vd)
- Self-heating Modelling
- C-V results (Gate Oxide)
- HiSIM_HV benchmark results
- Comparison of benchmark circuit test
- Summary

Table of Model Capabilities (1/3)

Physical Effects	HiSIM_HV 1.0.2
Technology:	
Quasi-Saturation	☑
RON	☑
Mobility	☑
Carrier Velocity Saturation	☑
Channel Length Modulation (CLM)	☑
Impact Ionization current (Substrate Current)	☑
Poly-Silicon-Gate Depletion Effects	☑
Geometry Scaling:	
SCE (Short Channel Effects)	☑
Reverse Short Channel Effects	☑
Narrow Channel Effects	☑
DIBL (Drain Induced Barrier Lowering)	☑

Table of Model Capabilities (2/3)

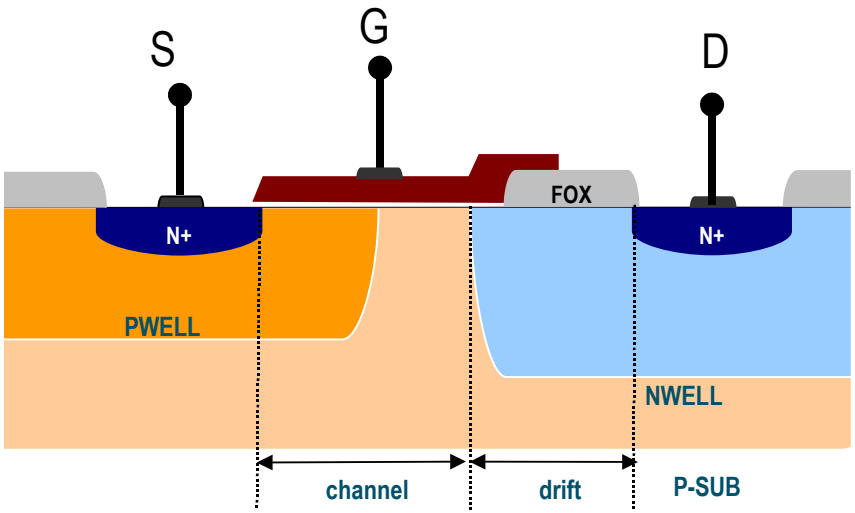
Physical Effects	HiSIM_HV 1.0.2
MOS Capacitance:	
Intrinsic Capacitance	☑
Overlap Capacitance	☑
Fringing Capacitance	☑
Bulk Diodes :	
Diode Current	☑ Only symmetrical
Diode Capacitance	☑ Only symmetrical
Temperature Modelling:	
Threshold Voltage	☑
Mobility	☑
Quasi-Saturation	☑
RON	☑
Impact Ionization (Bulk current)	☑
Self-heating	☑

Table of Model Capabilities (3/3)

Physical Effects	HiSIM_HV 1.0.2
Noise:	
SPICE2 Noise model	☒
Flicker Noise Model	☑
Short-Channel Thermal Noise Model	☑
Induced Noise in Gate and Substrate	☑
RF:	
Gate resistance model	☑
Substrate resistance model	☑
Multi-finger transistors	☑
Non-Quasi-Static (NQS):	
NQS	☑

⇒ HiSIM_HV has been selected for CMC standardization

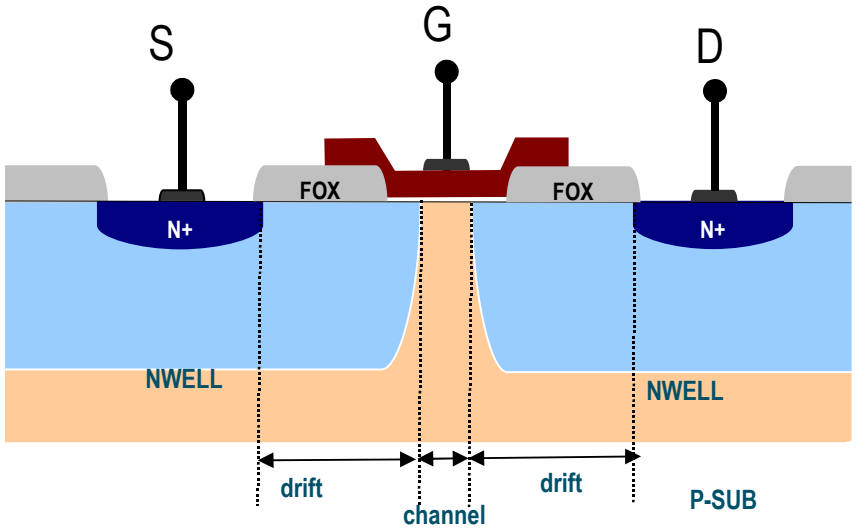
Cross-Section of LDMOS and HV-MOS



HiSIM_HV 1.0.2

Asymmetrical LDMOS

COSYM = 0

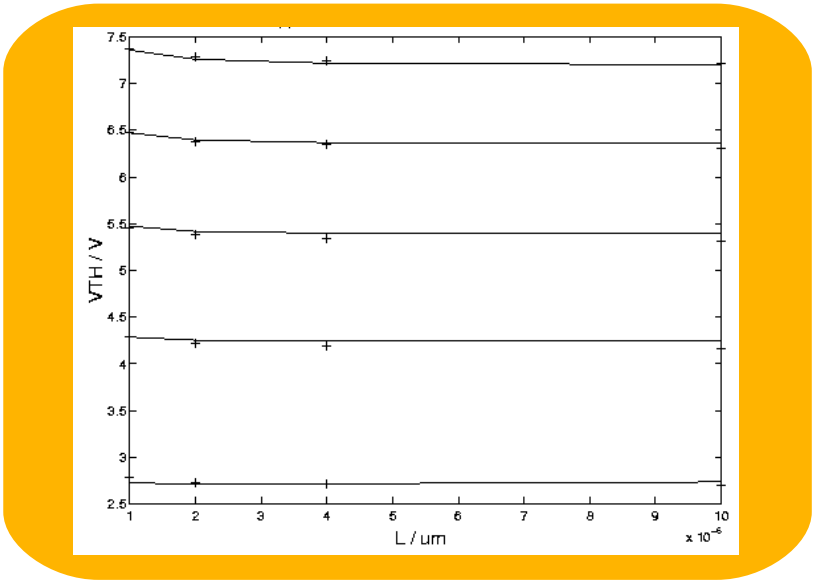


Symmetrical HV-MOS

COSYM = 1

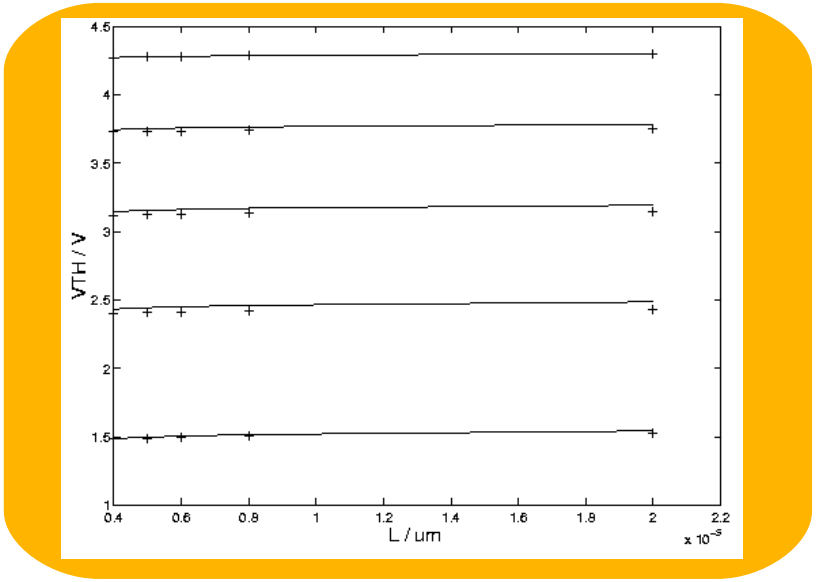
Geometry Scalable Modelling: Threshold Voltage

Asymmetrical NMOS



VTH vs. channel length

Symmetrical NMOS

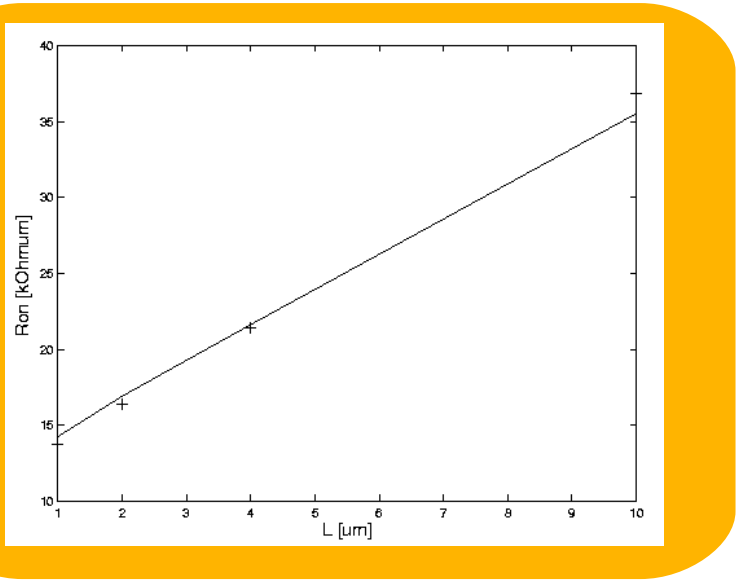


VTH vs. channel length

points: measurement; solid line: model

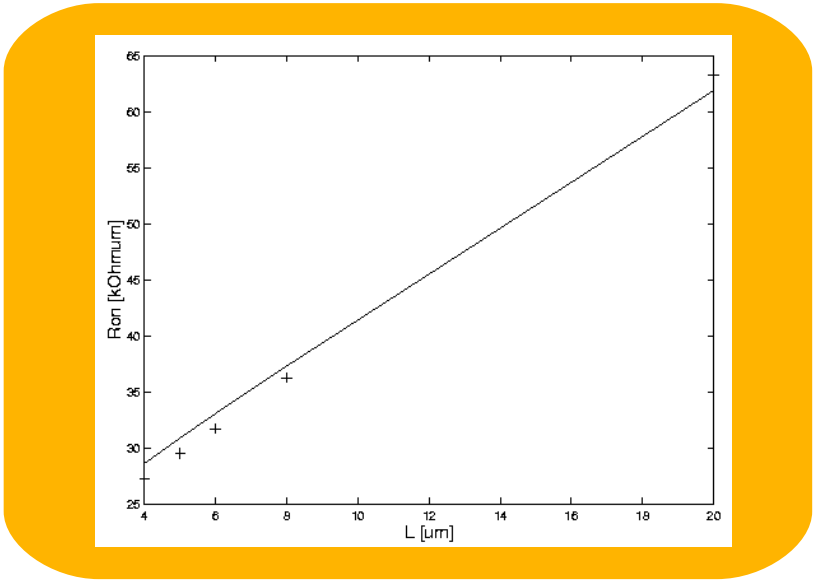
Geometry Scalable Modelling: on-resistance

Asymmetrical NMOS



On-resistance vs. channel length

Symmetrical NMOS

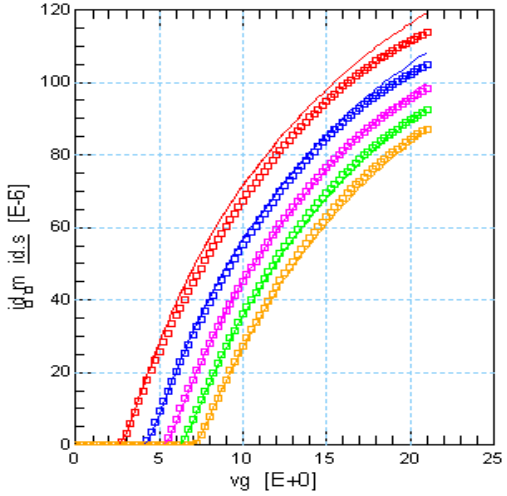


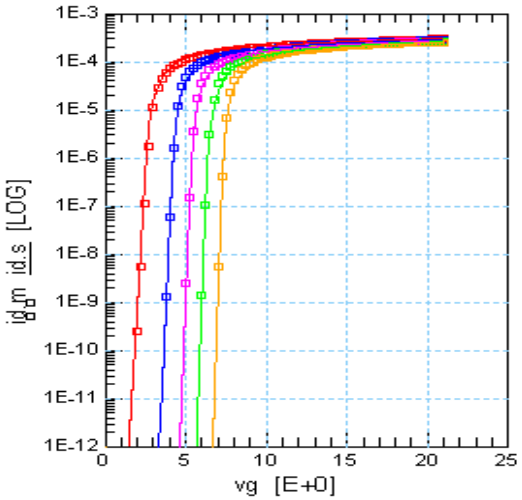
On-resistance vs. channel length

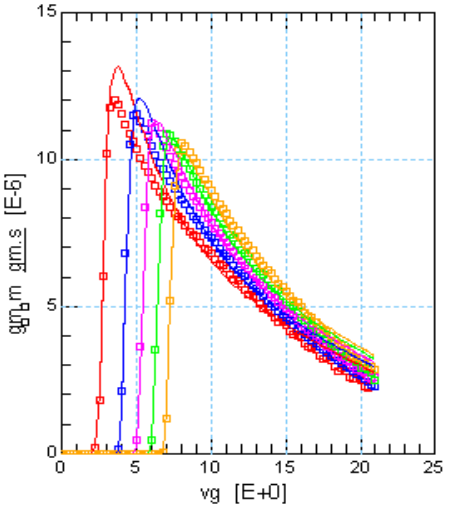
points: measurement; solid line: model

HiSIM_HV Modelling: Id-Vg Results (Large Device)

Asymmetrical NMOS

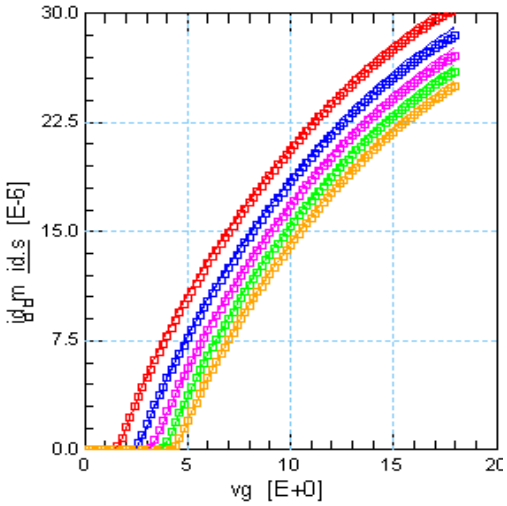


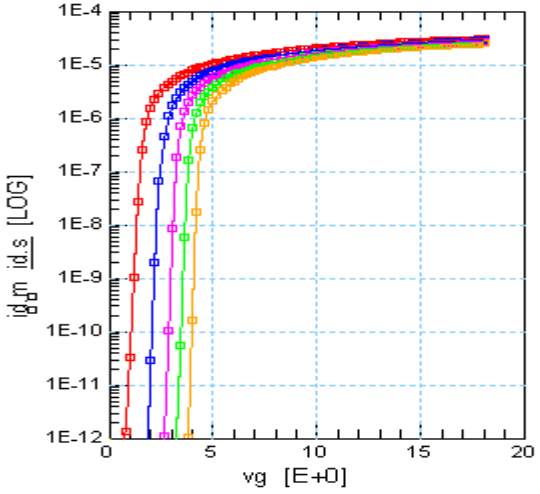


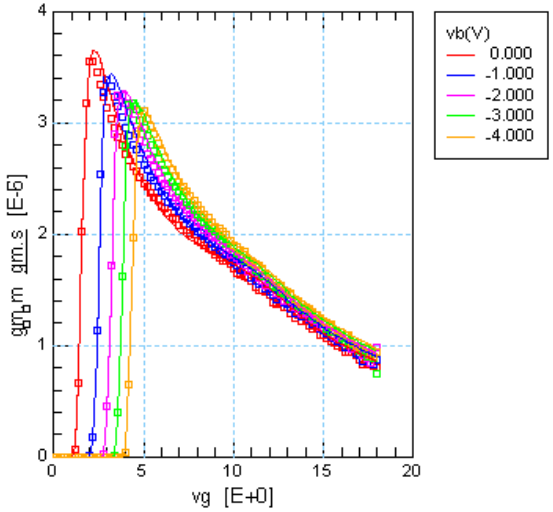


W/L: 40/10 um; points: measurement; solid line: model

Symmetrical NMOS



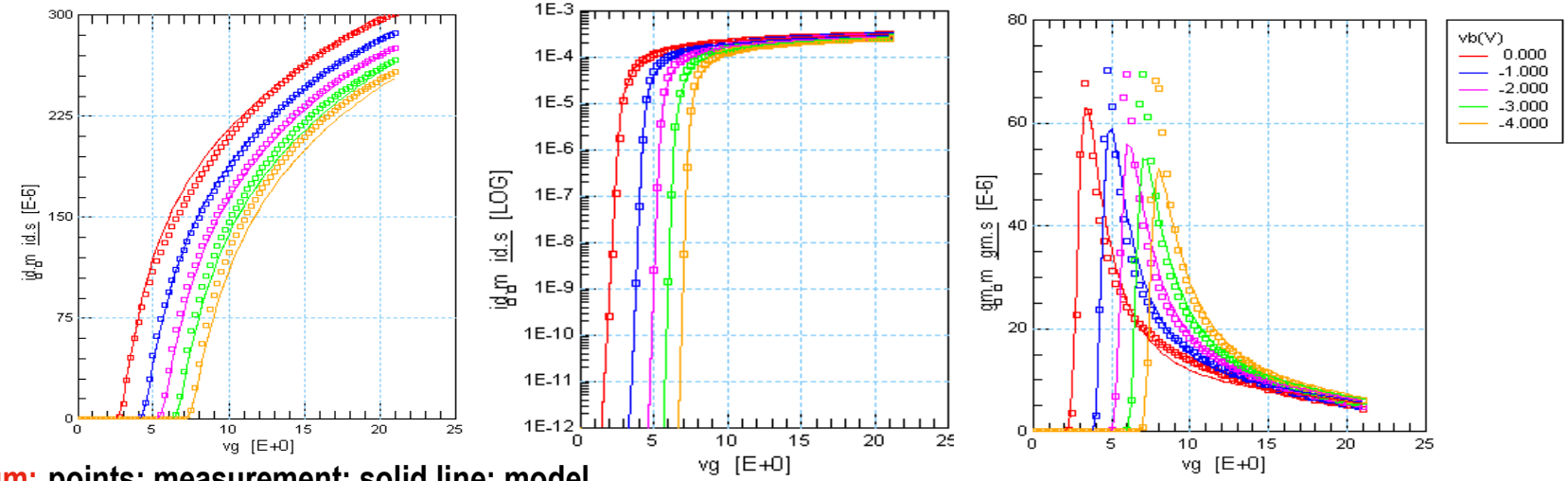




W/L: 20/20 um; points: measurement; solid line: model

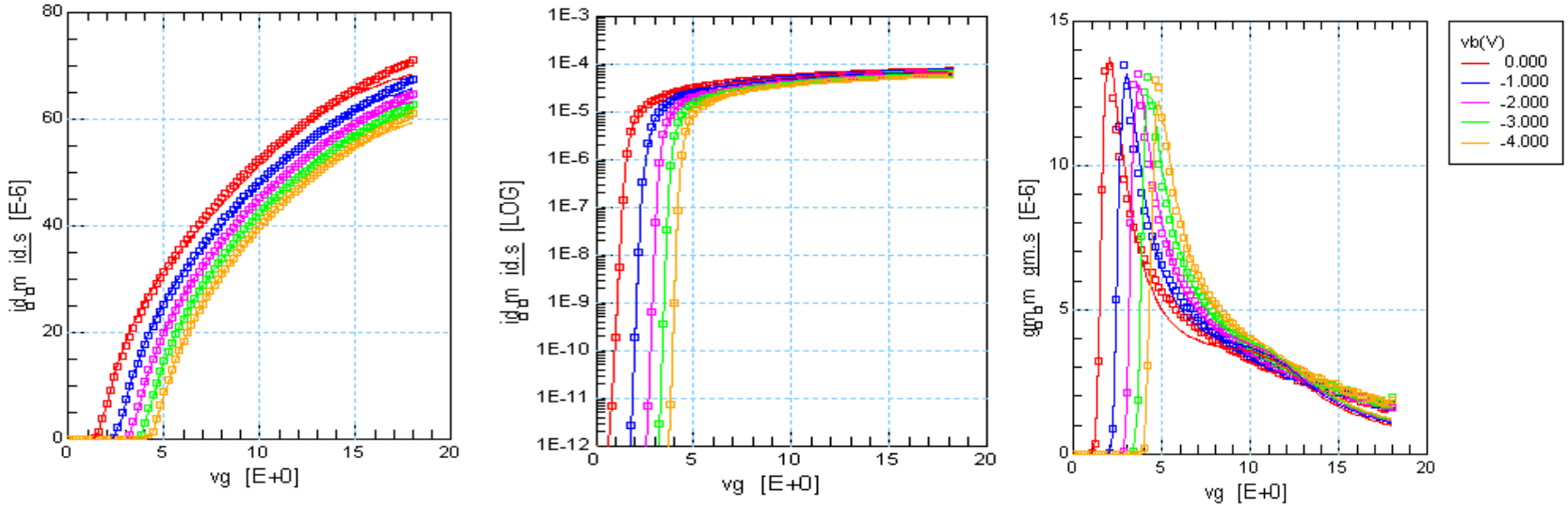
HiSIM_HV Modelling: Id-Vg Results (Short Device)

Asymmetrical NMOS



W/L: 40/1 um; points: measurement; solid line: model

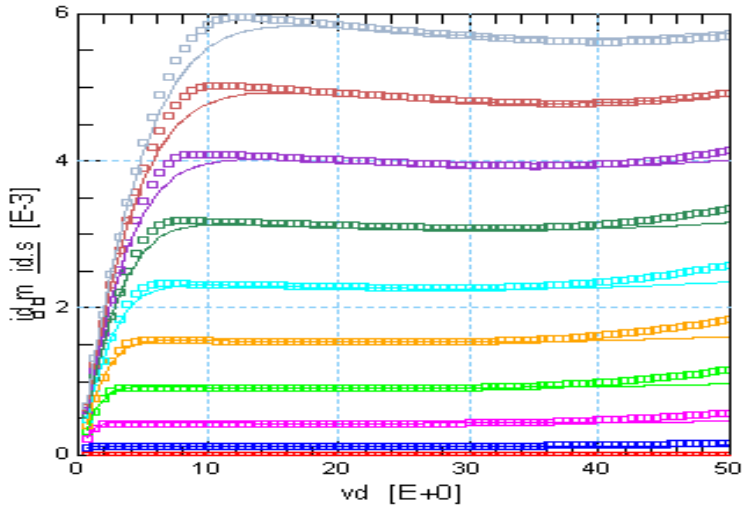
Symmetrical NMOS

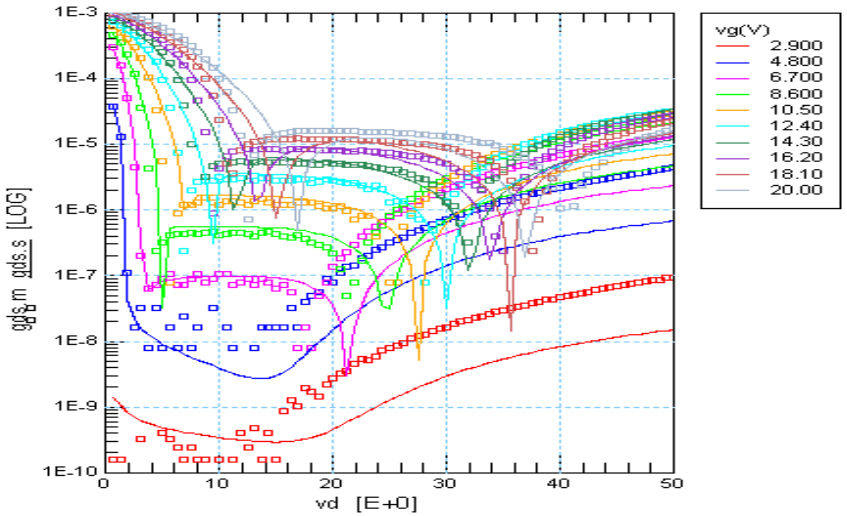


W/L: 20/4 um; points: measurement; solid line: model

HiSIM_HV Modelling: Id-Vd Results (Large Device)

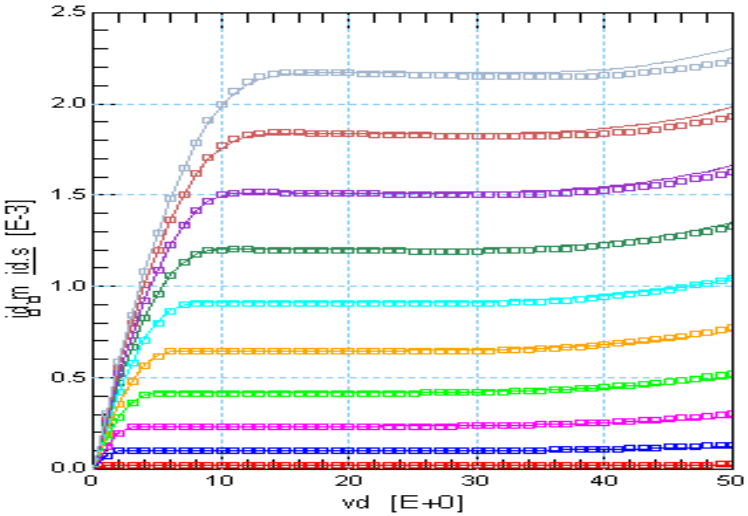
Asymmetrical NMOS

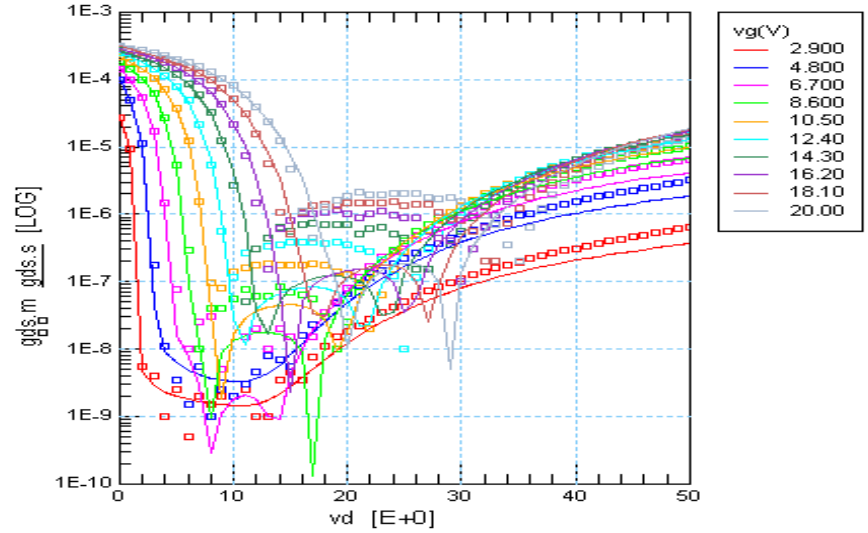




W/L: 40/10 um; points: measurement; solid line: model

Symmetrical NMOS

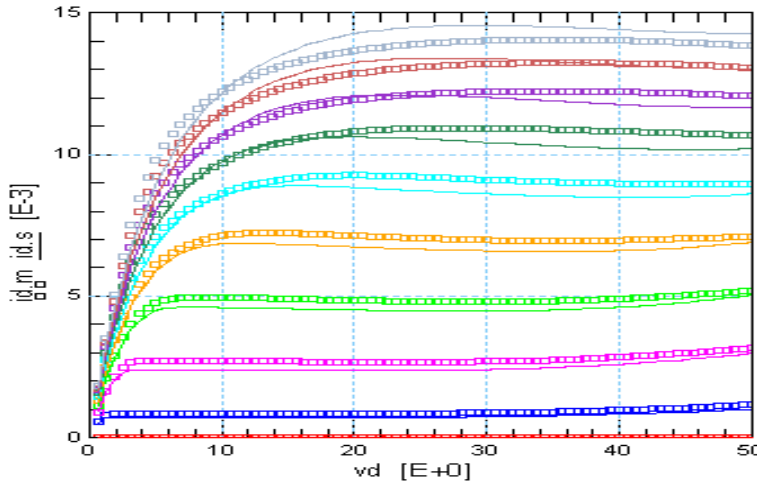


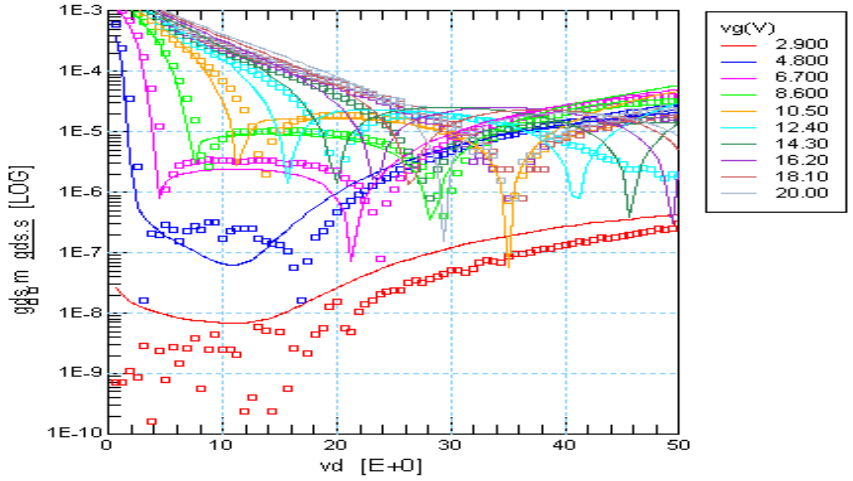


W/L: 20/20 um; points: measurement; solid line: model

HiSIM_HV Modelling: Id-Vd Results (Short Device)

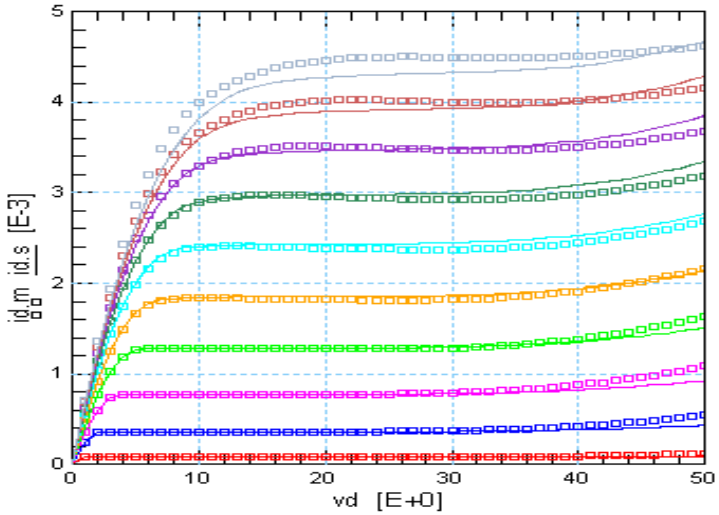
Asymmetrical NMOS

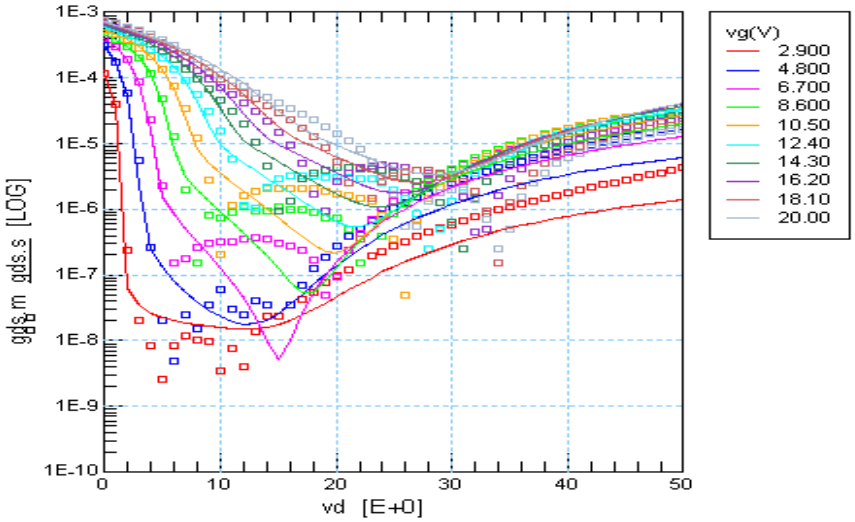




W/L: 40/1 um; points: measurement; solid line: model

Symmetrical NMOS



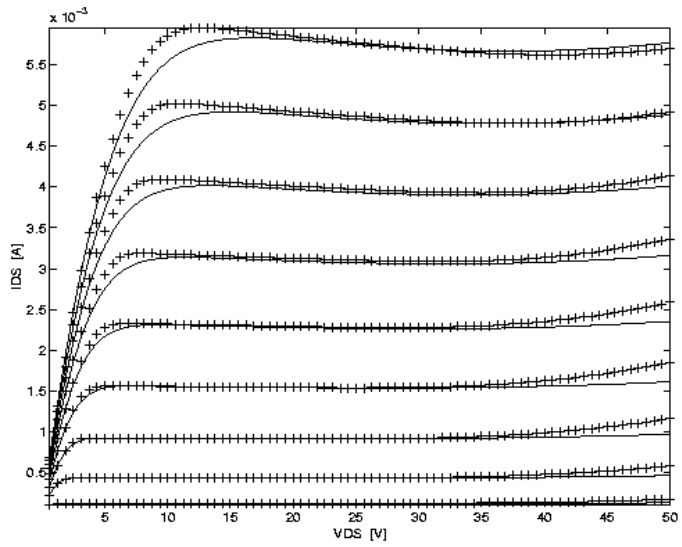


W/L: 20/4 um; points: measurement; solid line: model

Self-Heating Modelling (Asymmetry NMOS)

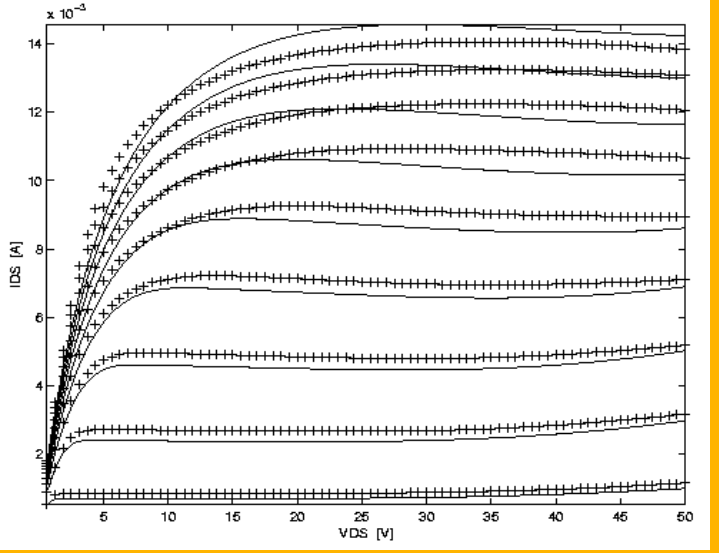
W/L=40/10 um; Vgs=6.7(1.9) 20V

Self-heating modelling flag on



W/L=40/1 um; Vgs=2.9(1.9) 20V

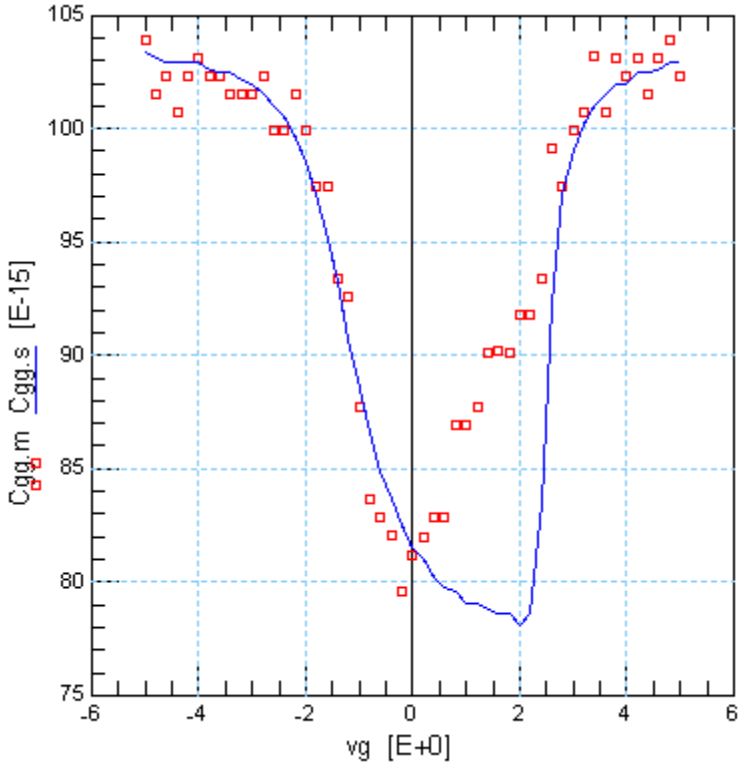
Self-heating modelling flag on



points: DC measurement with self-heating solid line: model

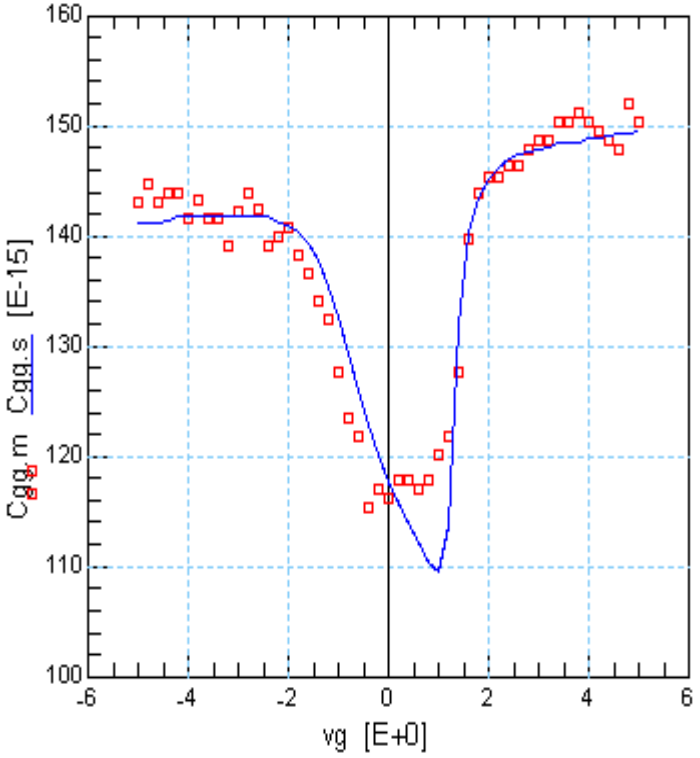
HiSIM_HV Modelling: C-V Results

Asymmetrical NMOS



W/L= 40/1 um; Vds=0V

Symmetrical NMOS



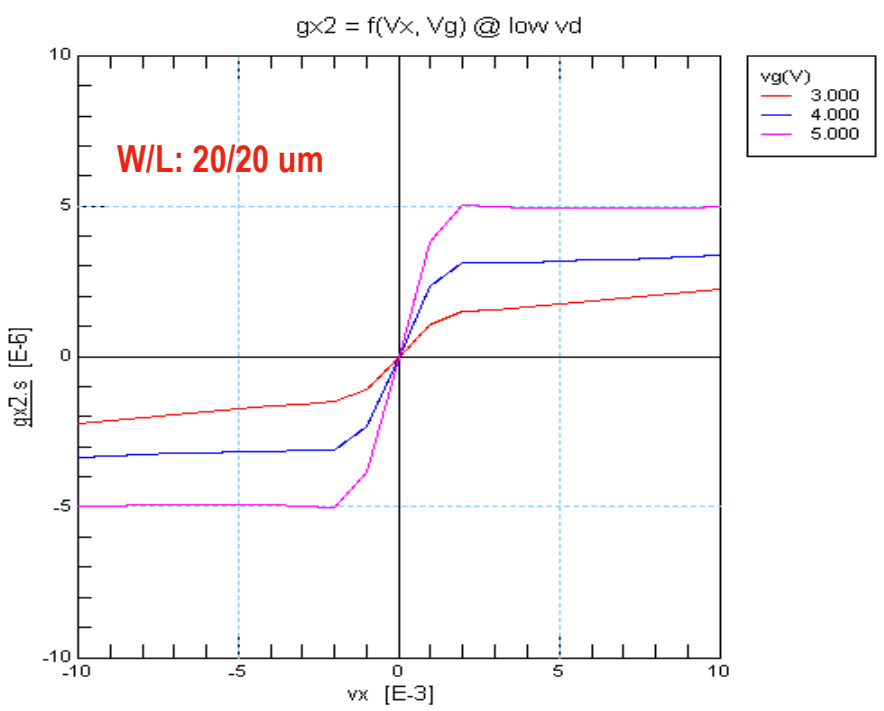
W/L= 20/4 um; Vds=0V

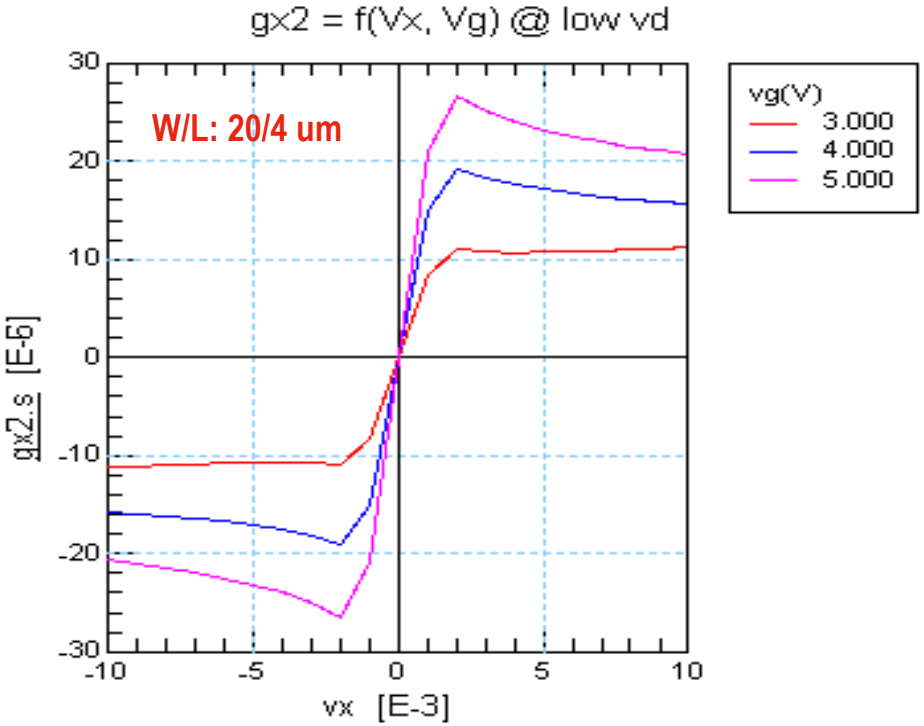
$Cgg=imag(y_{11})/\omega$

points: measurement; solid line: model

Benchmark Test
HiSIM_HV 1.0.2

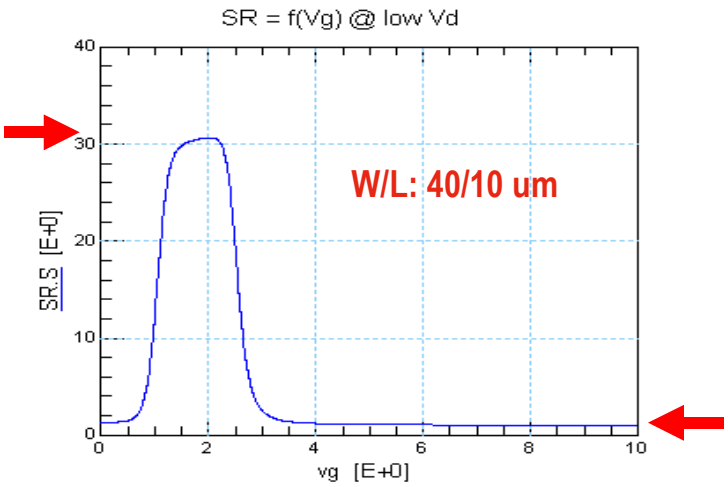
HiSIM_HV 1.0.2: Gummel Symmetry Test (Symmetry NMOS)

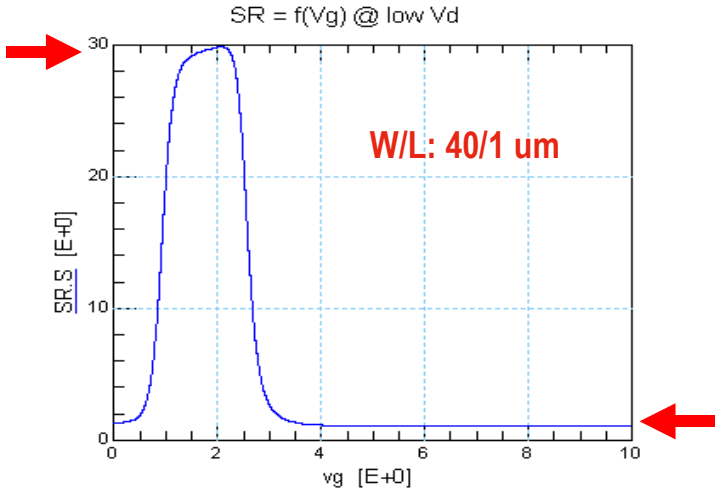




HiSIM_HV 1.0.2: Gummel Slope Ratio Test

Asymmetrical NMOS

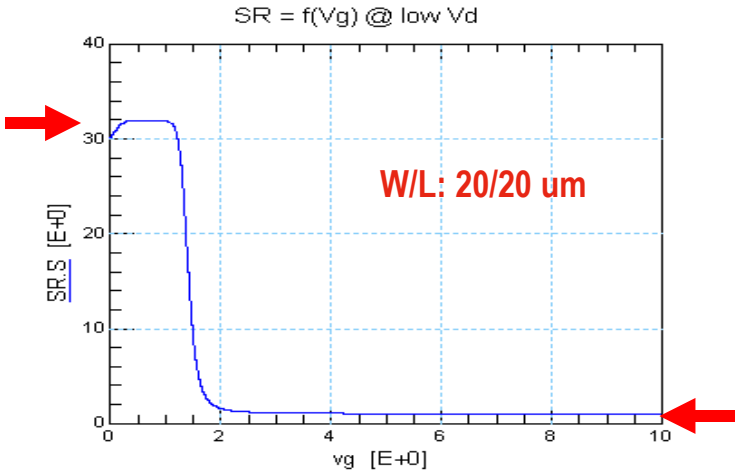


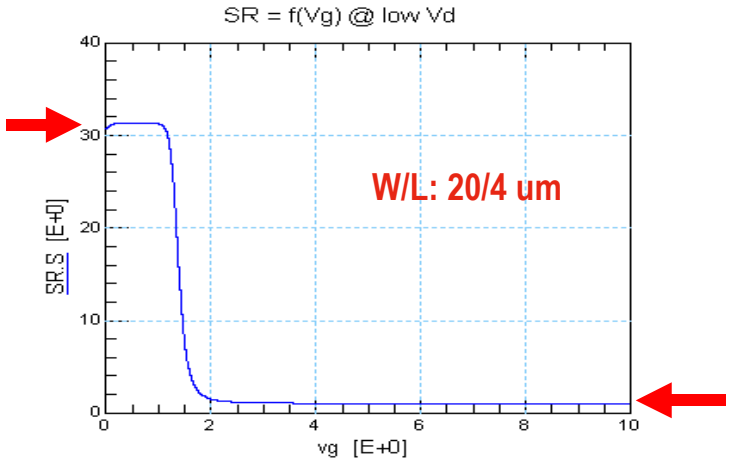


$$SR = \frac{(Id2 + Id1) * (Vd2 - Vd1)}{(Id2 - Id1) * (Vd2 + Vd1)}$$

Vd=0.1,0.2V; Vb=0V

Symmetrical NMOS

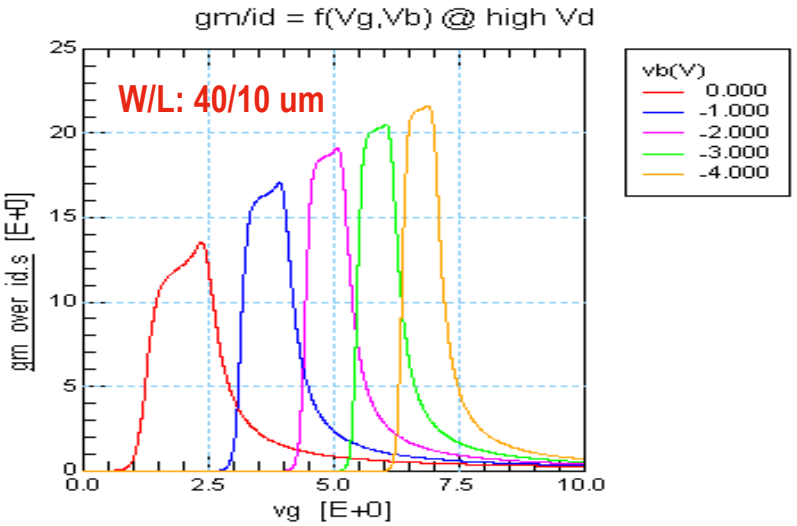


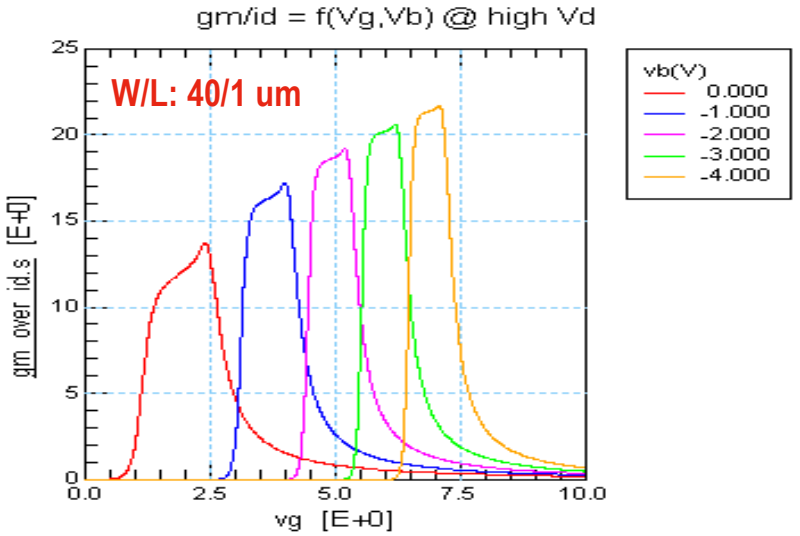


Vd=0.1,0.2V; Vb=0V

HiSIM_HV 1.0.2: Gummel Treetop Test

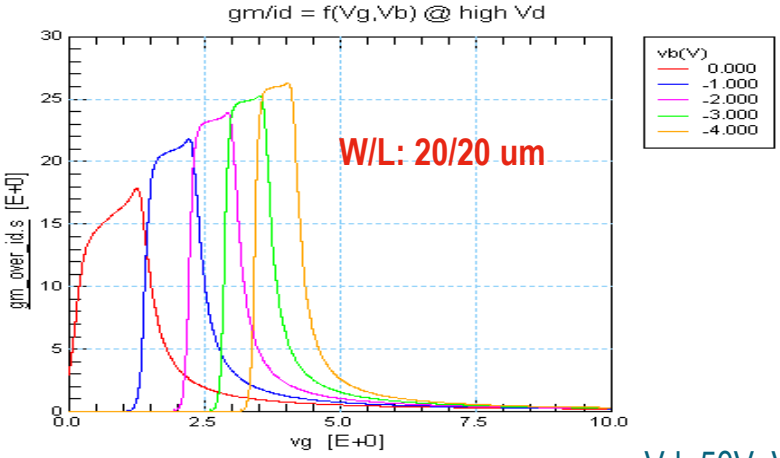
Asymmetrical NMOS

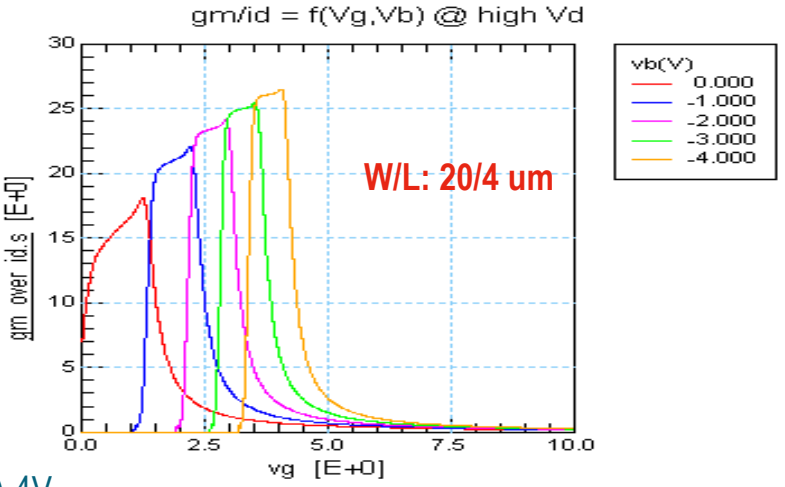




Vd=50V, Vb=0(-1)-4V

Symmetrical NMOS





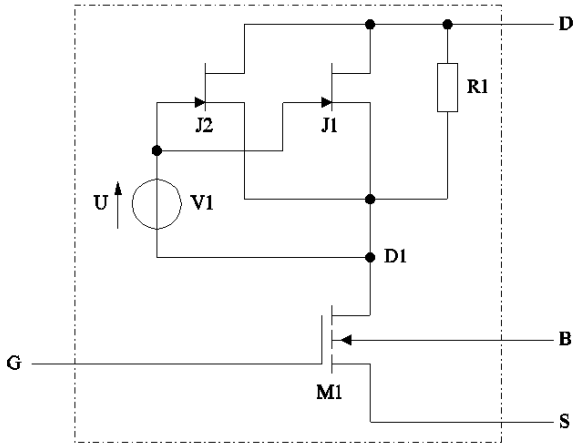
Vd=50V, Vb=0(-1)-4V

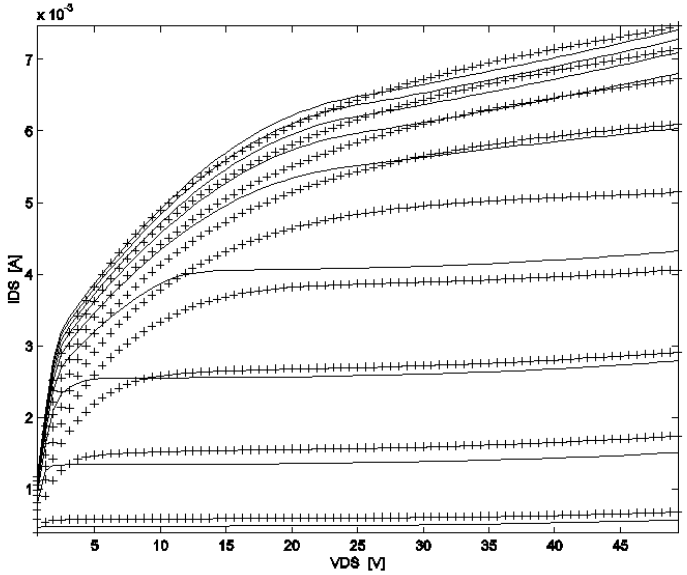
Benchmark Circuit Test Comparison:

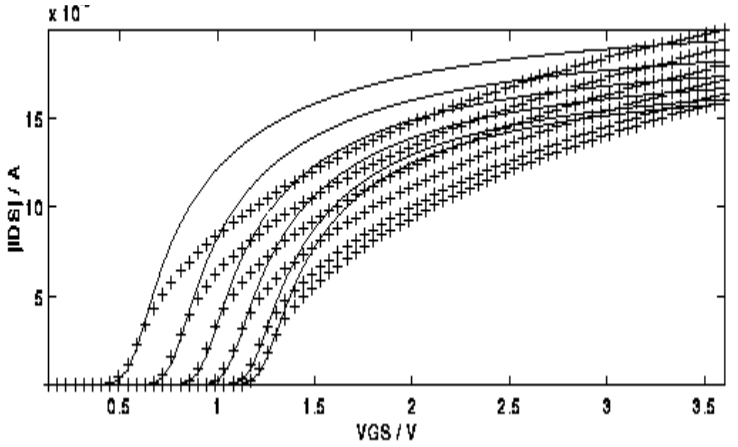
BSIM3-Sub-Circuit and HiSIM_HV 1.0.2

AMS BSIM3-Sub-Circuit Model for LDMOS and HV_MOS

BSIM3 based scalable sub-circuit model







Fitting problems:

- linear region
- quasi-saturation region

Benchmark Circuit I - Ringoscillator

Inverter chain:

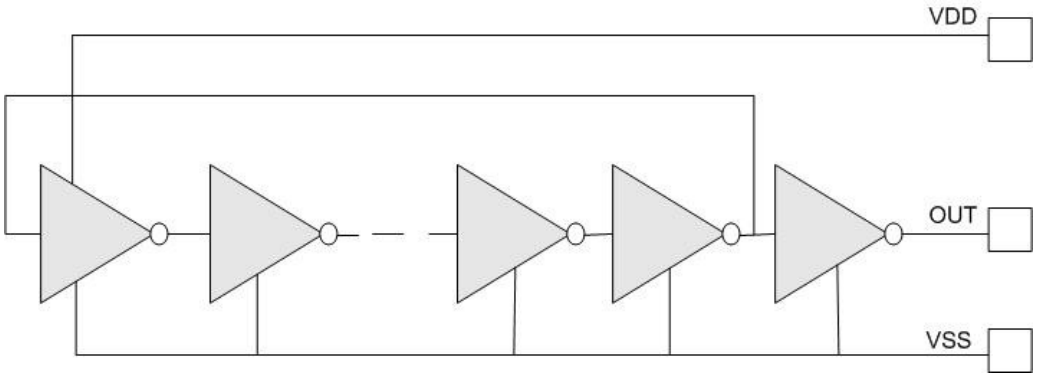
41 stages + 1 Buffer

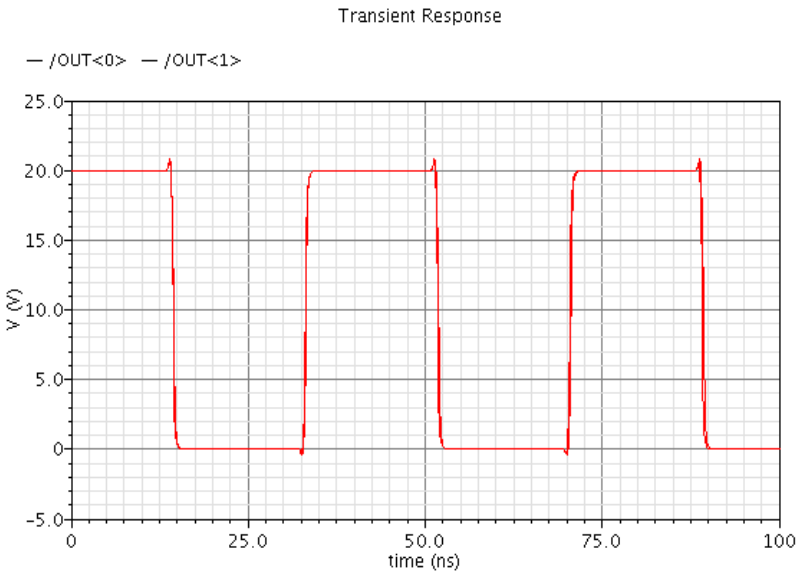
Important parameters:

Rise time, fall time, periodity

Relevant SPICE parameters:

G-D capacitance models





Operating System:

Linux 32Bit,

Dual Core Intel CPU T2400 @ 1.83GHz

Simulation time comparison:

Transient simulation: 100ns

	Total simulation Time:	Used Memory
Sub-circuit:	48,14s	9.56MB
HISIM model:	34,45s	6.48MB
Delta [%]:	~30	~33

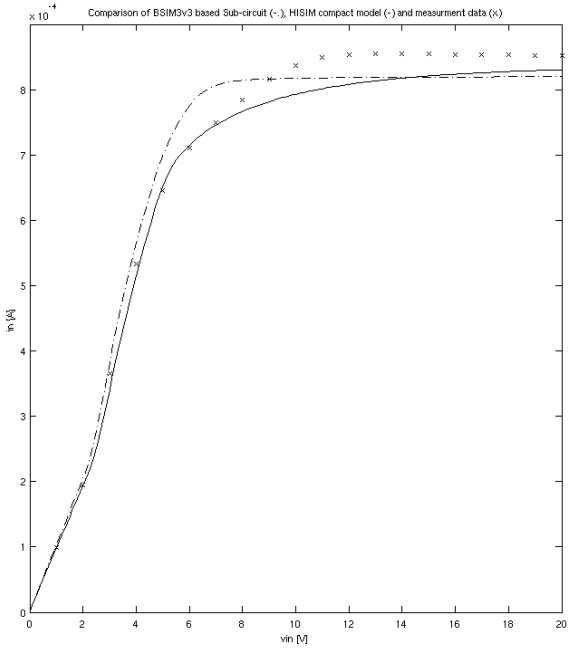
Benchmark Circuit II – Gate Switch

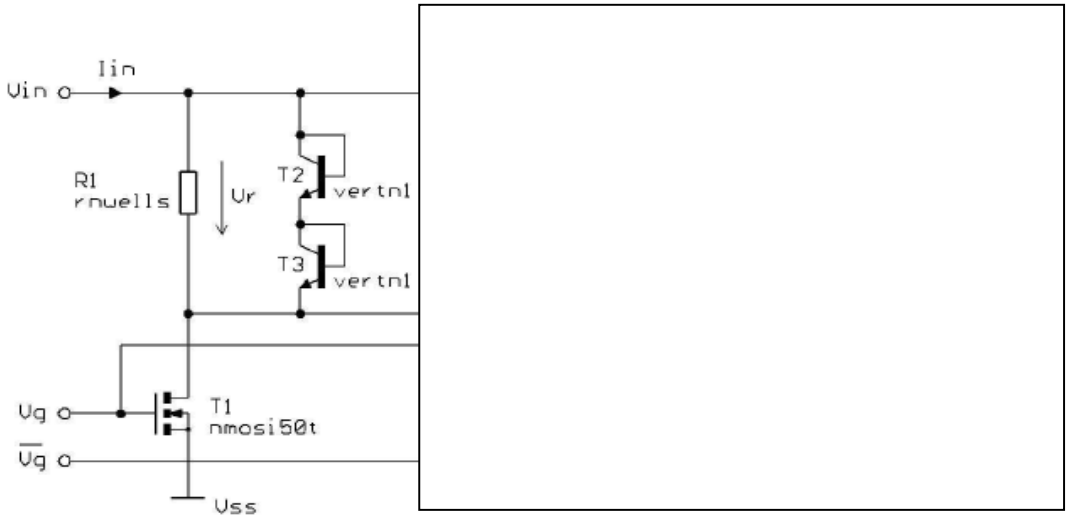
Operation:

Temperature stabilized Gate switch

Problem Specification:

Sub-circuit models differ because of too simple drain resistance model.





Accuracy check:

op:

vg=3.3V,

vin ramped over whole operating range

The linear region is expressed highly accurate by the compact model.

Smoother behavior of the whole curve.

Summary

- HiSIM_HV is a fully scalable analytical surface potential based model for HV MOSFFTs, includes most of the physical effect due to drift region.
- Model results shows very good agreement with measurement data for both symmetrical and asymmetrical MSOFET devices
- Self-heating model is also verified and shows good accuracy
- Circuit benchmark test shows high speed of simulation and accuracy
- Model can be used for sufficient accuracy for low-risk design of high-voltage ICs.

Acknowledgment: We would like to thank W. Pfanzl and W. Posch for pulse measurement and HiSIM code implementation in MATLAB, respectively.

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Thank you