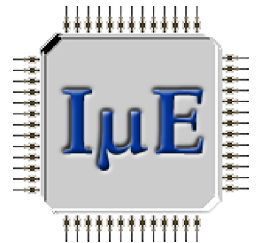


Mixed-Mode Device/Circuit Simulation



Tibor Grasser



Institute for Microelectronics

Gußhausstraße 27–29, A-1040 Wien, Austria

Technical University Vienna, Austria

<http://www.iue.tuwien.ac.at>

Outline

Circuit simulation and compact models

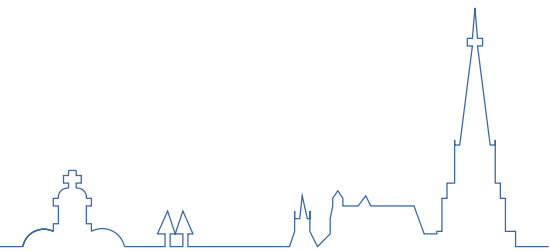
Numerical models instead of compact models

Challenges in numerical modeling

Mixed-mode device/circuit simulation

Examples

Conclusion

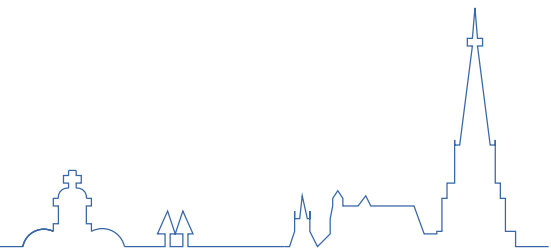


Circuit Simulation

Circuit simulation fundamental

Development of modern IC

To understand and optimize the way a circuit works



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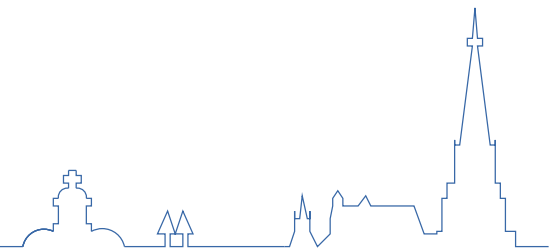
For circuit simulation we need

Lumped elements: R, C, L, etc.

Current and voltage sources, controlled sources

Semiconductor devices

Thermal equivalent circuit (coupling and self-heating)



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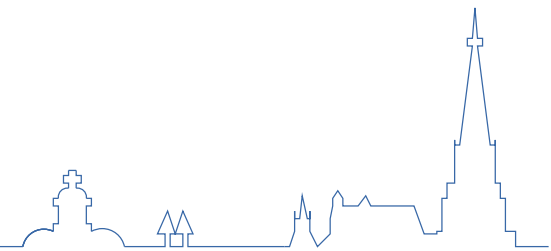
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Electrical/thermal properties of semiconductor devices

Characterized by coupled partial differential equations



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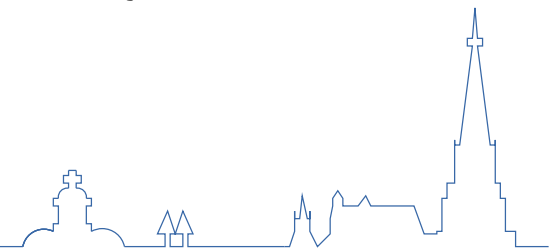
Electrical/thermal properties of semiconductor devices

Characterized by coupled partial differential equations

For the simulation of large circuits we need compact models

Obtained from simplified solutions of these PDEs or empirically

Must be very efficient (compact!)



Compact Modeling

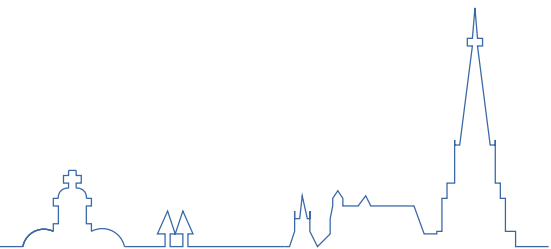
Derivation of compact models based on fundamental equations

Often the drift-diffusion framework is used

Simplifying assumptions on geometry, doping profiles, material parameters

⇒ *Compact model*

It is becoming increasingly difficult to extract main features



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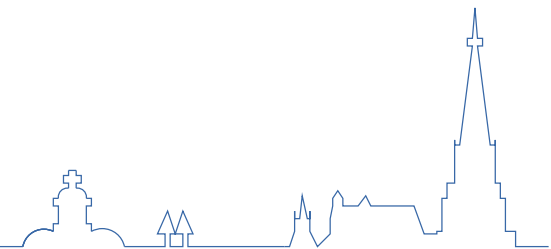
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Number of parameters

Physical meaning of these parameters

Predictiveness difficult to obtain, calibration required



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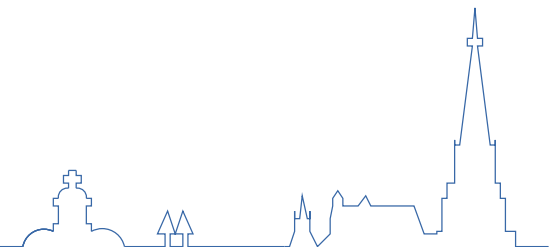
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Compact modeling challenges (ITRS)

Quantum confinement

Ballistic effects

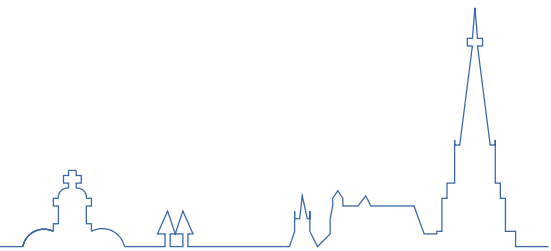
Inclusion of variability and statistics



Simulation with Compact Models

Advantages of using compact models

Very fast execution (compared to PDEs)



Simulation with Compact Models

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Disadvantages

Many parameters

Physically motivated parameters

Fit parameters

Parameter extraction can be quite cumbersome

Device optimization via geometry and doping profile hardly possible

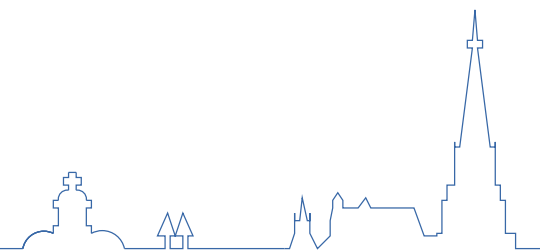
Considerable model development effort

Limited model availability (DG, TriGate, FinFETs, GAAFETs, etc.)

Scalability questionable

Quantum effects

Non-local effects



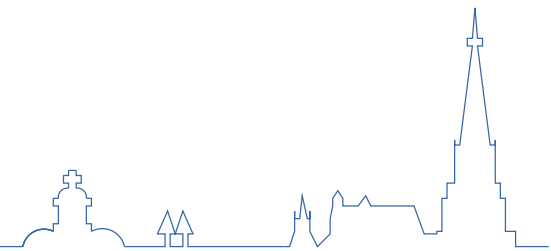
Mixed-Mode Simulation

Instead of

Analytical expressions describing the device behavior (compact models)

Rigorous device simulation based on

Coupled partial differential equations!



Compact Modeling – Numerical Modeling

Advantages of numerical device simulation

Fairly arbitrary devices (doping, geometry)

Realistic doping profiles from process simulation

Natural inclusion of

2D/3D effects

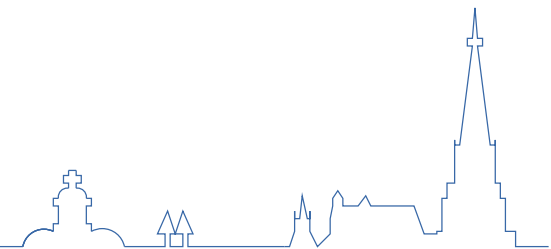
Non-local effects (via appropriate transport model)

Quantum mechanical effects (via simplified model or Schrödinger's equation)

Temperature dependencies

Sensitivity of device/circuit figures of merit to process parameters

Better predictivity for scaled/modified devices



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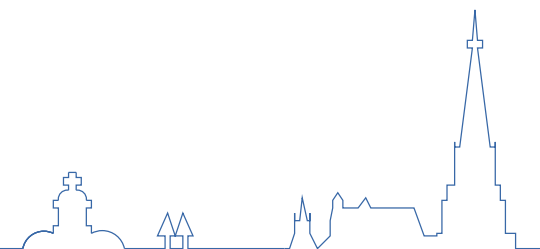
Better predictivity for scaled/modified devices

Disadvantages of numerical modeling

Performance (don't compare!)

Convergence sometimes costly/difficult to obtain

Realistic doping profiles from process simulation

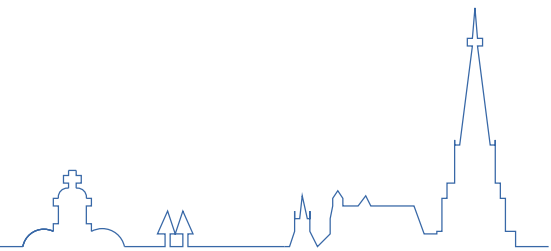


Challenges in Device Simulation

Feature size approaches mean free path

Ballistic effects become important

No ballistic transistor in sight, but still important effect



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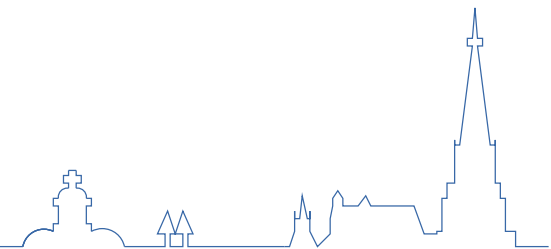
Feature size approaches electron wavelength

Quantum mechanical effects become important

Transport remains classical

Critical gate length around 10 nm

Modified transport parameters for thin channels



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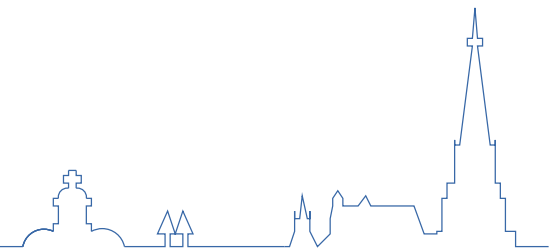
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Exploitation of new effects

Strain effects used to boost mobility

Substrate orientation and channel orientation



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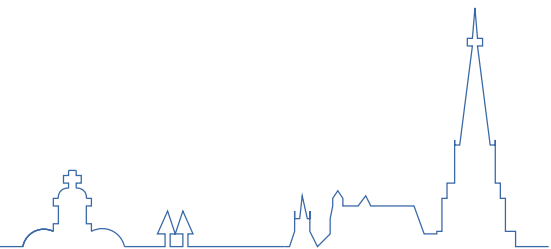
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Exploitation of new materials

Strained silicon, SiGe, Ge, etc.

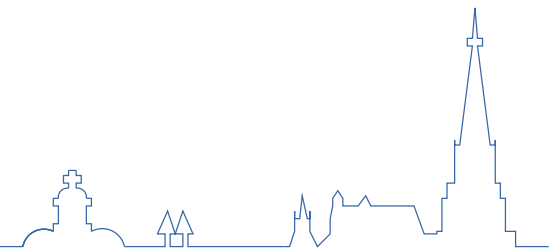
High-k dielectrics



Device Simulation

Classical transport described by Boltzmann's equation

Allows inclusion of sophisticated scattering models, quasi-ballistic transport



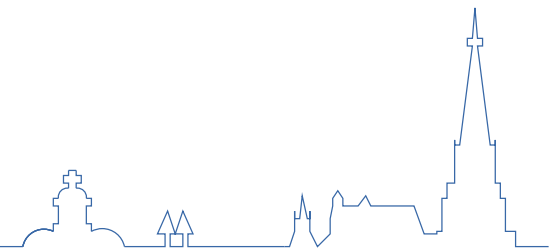
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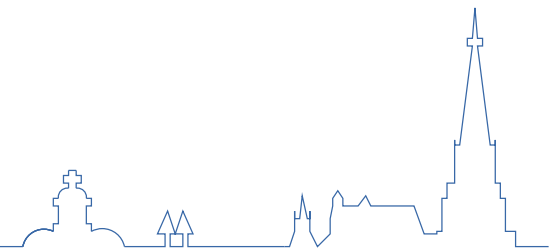
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Approximate solution obtained by just looking at moments of f

Simplest moment-based model: the classic drift-diffusion model

$$\epsilon \nabla^2 \psi = q(n - p - C)$$

$$\nabla \cdot (D_n \nabla n - n \mu_n \nabla \psi) - \frac{\partial n}{\partial t} = R$$

$$\nabla \cdot (D_p \nabla p + p \mu_p \nabla \psi) - \frac{\partial p}{\partial t} = R$$

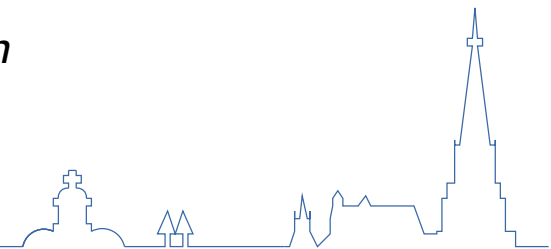
Requires models for physical parameters D , μ , and R

These models capture fundamental physical effects

Velocity saturation, SRH recombination, impact-ionization

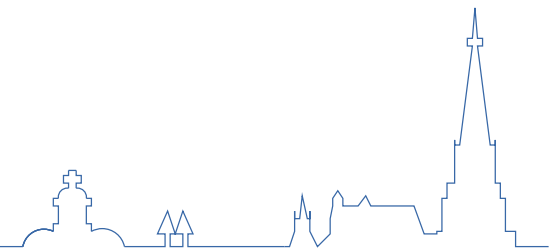
Models can be quite complex

Used to be basis for the derivation of compact models



Double-Gate MOSFETs

Drift-diffusion model inaccurate for short-channel devices



Double-Gate MOSFETs

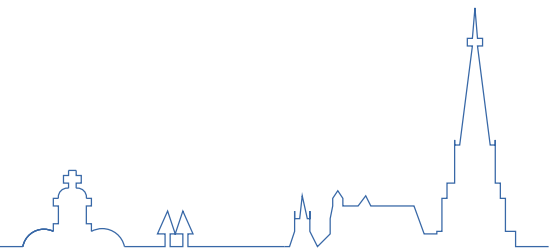
Drift-diffusion model inaccurate for short-channel devices

Higher-order moment models available

Comparison of scaled DG-MOSFETs

Comparison with fullband Monte Carlo data

Transport parameters from FBMC



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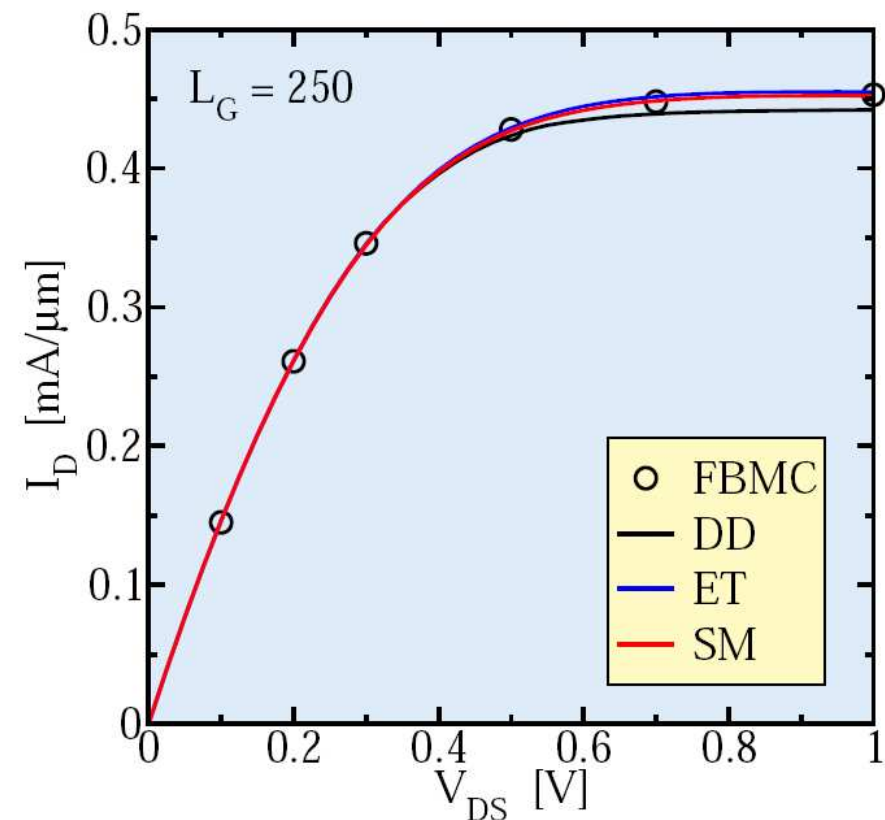
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No velocity overshoot



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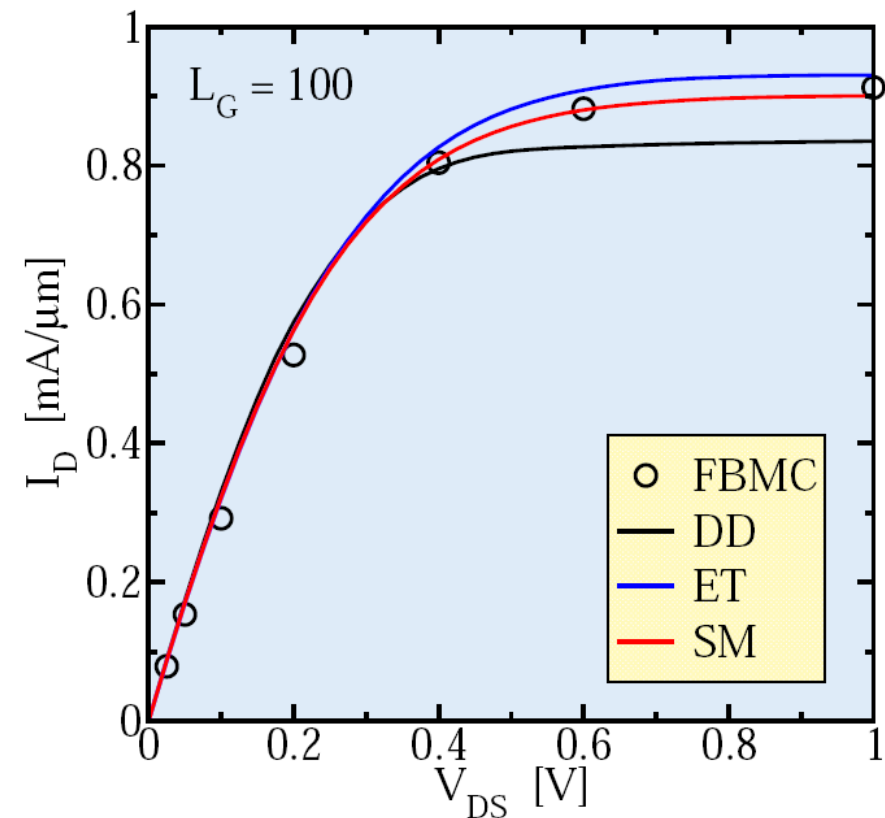
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ET accurate at 100 nm

Maxwellian distribution function



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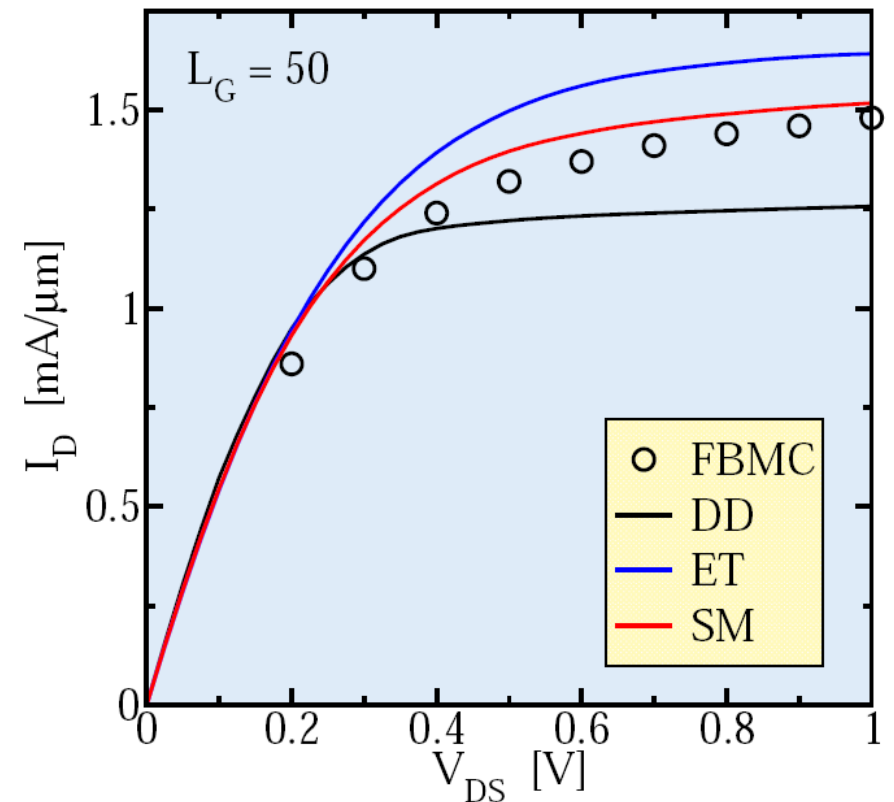
Maxwellian distribution function

SM accurate at 50 nm

Non-Maxwellian effects

Low computational effort

'TCAD' compatible



Mixed-Mode Simulation

Simulator coupling

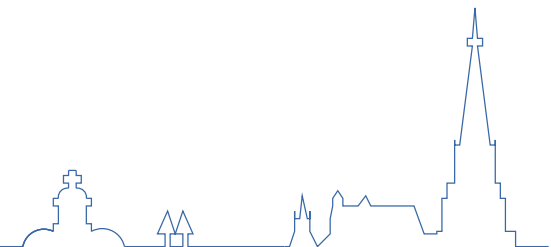
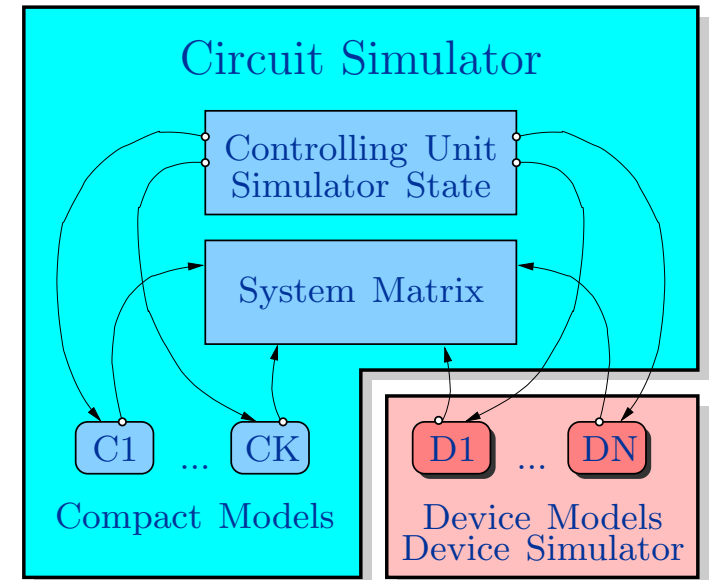
Simple, straight forward solution

Two-Level Newton algorithm

SPICE-like damping algorithms usable

Many iterations for device equations needed

Parallelization straight-forward



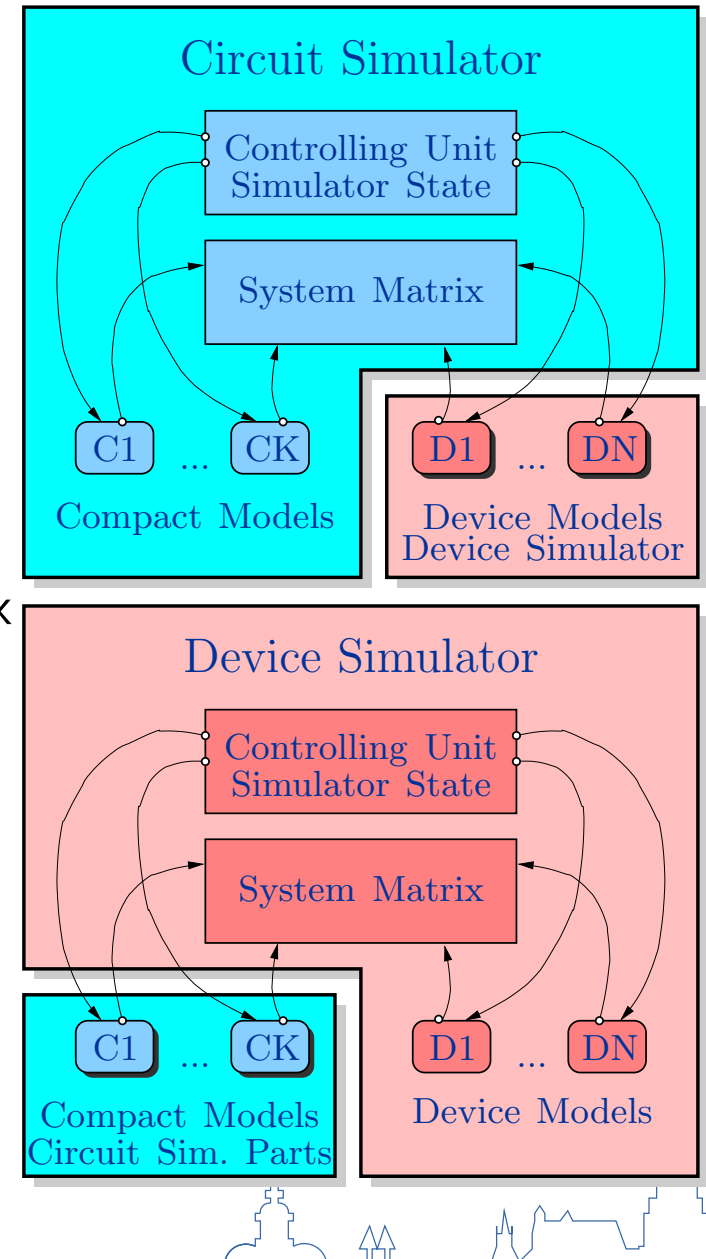
Mixed-Mode Simulation

Simulator coupling

- Simple, straight forward solution
- Two-Level Newton algorithm
- SPICE-like damping algorithms usable
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All-In-One solution (Full-Newton)

- Circuit and device equations in one single matrix
- Full-Newton algorithm
- Complex convergence behavior
- Parallelization more complicated



Simulator Coupling

Two-Level Newton

Device simulator is called for each circuit iteration

Fixed set of contact voltages

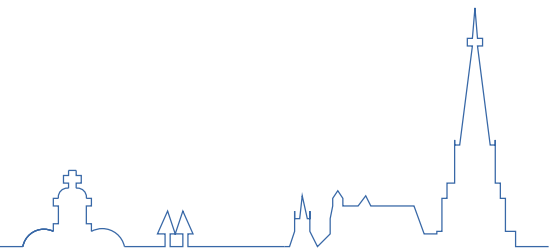
Contact current response I_C^k

Problematic: $g_{\text{eq}}^k = \left. \frac{\partial I_C}{\partial V_C} \right|_k$

Device simulator iterates until convergence

Last iteration as initial-guess

Linear prediction algorithm



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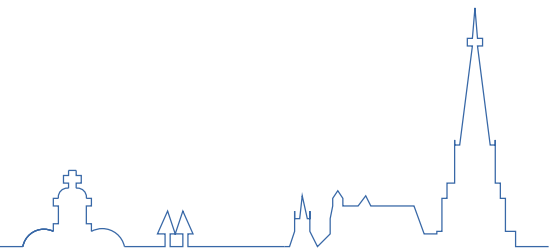
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Linear prediction algorithm

Quasi Full-Newton

Only one iteration of device simulator

Calculation of I_C^k and g_{eq}^k



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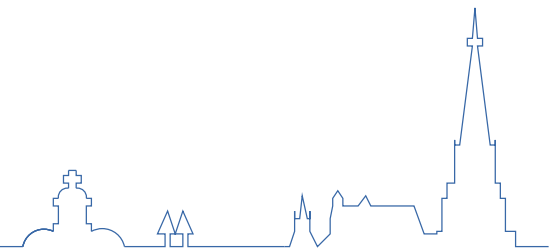
Calculation of I_C^k and g_{eq}^k

Advantages

Straight-forward parallelization

SPICE-like damping schemes can be applied

Stable operating point computation



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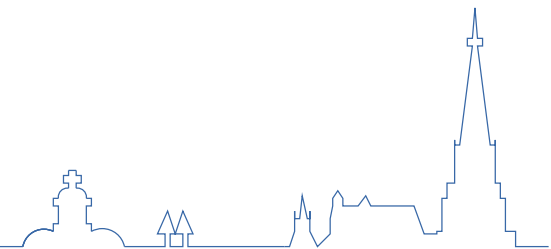
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Disadvantages

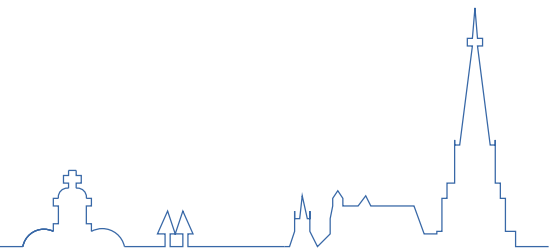
Considerable overhead



Full-Newton Approach

Device and circuit equations in one matrix

Simultaneous damping of device and circuit equations



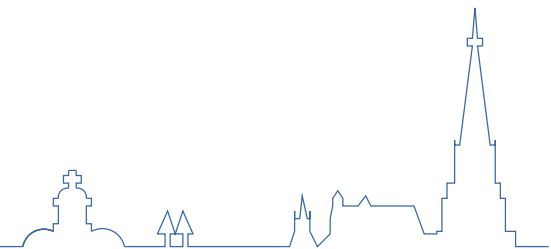
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No input-deck generation, no temporary input and output files, etc.



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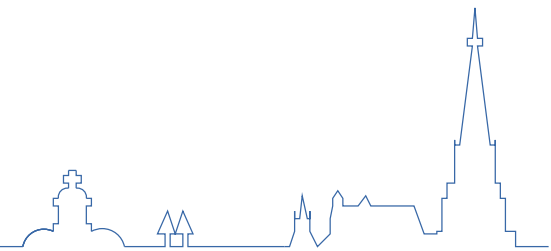
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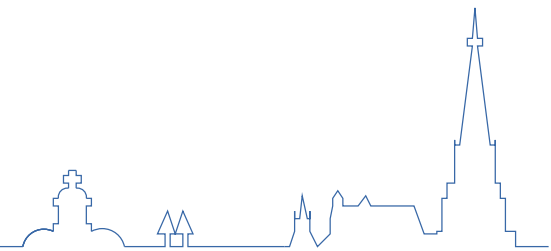
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Properties of the newton method

Quadratic convergence properties for a good initial-guess (**fast!**)

Initial-guess hard to construct

Damping schemes



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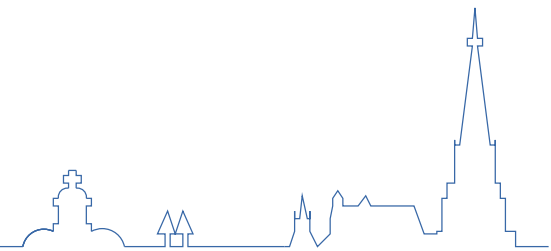
Reliable DC operating point calculation of utmost importance

Drift-diffusion solution as initial-guess for

Higher-order transport models

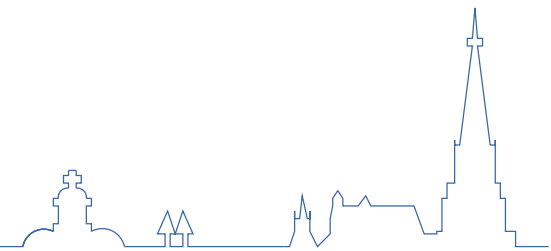
Electro-thermal solution

Transient simulations better conditioned



Convergence

Why is convergence hard to obtain?



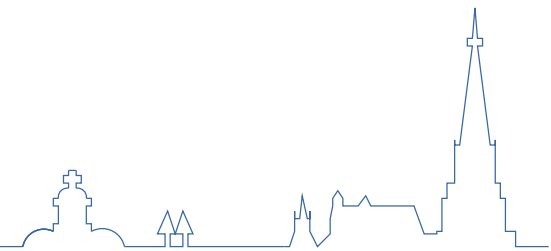
Convergence

Why is convergence hard to obtain?

Conventional boundary condition for numerical devices

$$V_{C,i} \text{ (device contact potential)} = \varphi_{C,i} \text{ (node voltage)}$$

Carrier concentrations depend exponentially on the potential



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No pure voltage boundary conditions

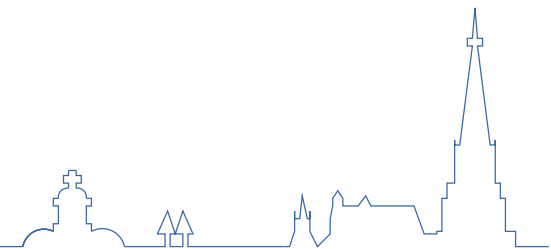
Current flowing out of the contact affects node voltages

System is extremely unstable at the beginning of the iteration

Similar situation as with current boundary condition

Shifts in the DC offset require many iterations

Distributed quantities provide 'internal state'



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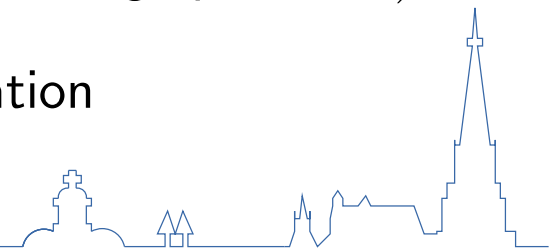
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Alternative boundary condition for numerical devices

$$V_{C,i} = \varphi_{C,i} - V_{\text{ref}} \quad \text{with} \quad V_{\text{ref}} = \frac{1}{N_c} \sum_j \varphi_{C,j} \quad \text{(average potential)}$$

Average potential changes during the iteration and operation



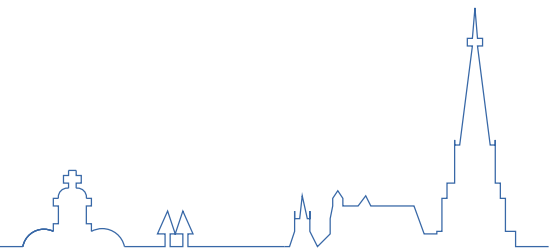
Convergence – Damping Schemes

Simple Methods

Limitation of node voltage update to $2V_T$

Many iterations needed

Initial guess close to the solution (experimental value: ± 0.2 V)



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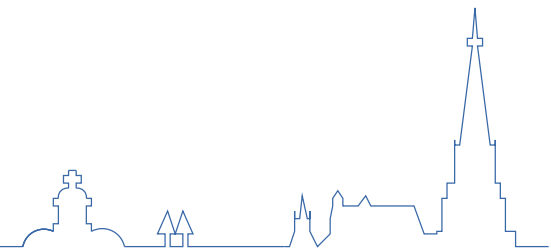
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Traditional device simulation methods

Damping after Bank and Rose (SIAM 1980)

MINIMOS damping scheme

Standard damping schemes not suitable for mixed-mode problems



Convergence – Embedding Scheme

Shunt an iteration dependent conductance G_S^k at every contact

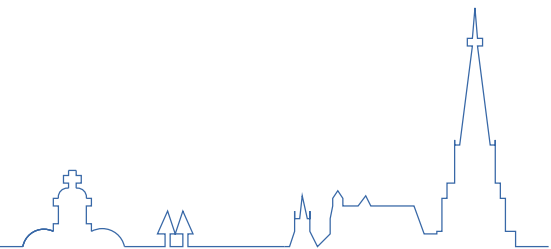
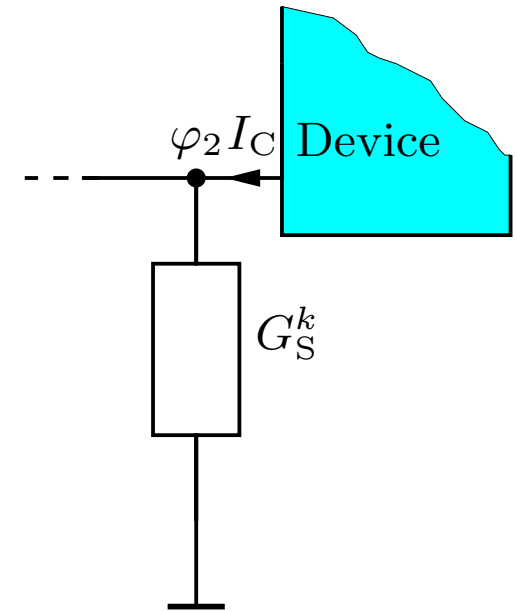
Purely empirical expression

$$G_S^k = \max\left(G_{\min}, G_0 \times 10^{-k/\kappa}\right)$$

$$G_0 = 10^{-2} \text{ S}$$

$$G_{\min} = 10^{-12} \text{ S}$$

$$\kappa = 1.0 \dots 4.0$$



Convergence – Embedding Scheme

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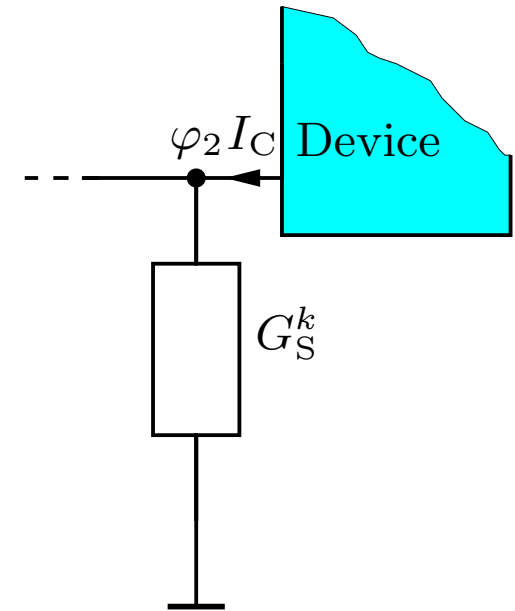
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$$G_0 = 10^{-2} \text{ S}$$

$$G_{\min} = 10^{-12} \text{ S}$$

$$\kappa = 1.0 \dots 4.0$$



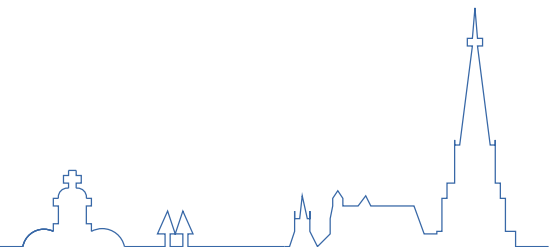
Method works for small circuits

Zero initial-guess for node voltages

Charge neutrality assumptions for semiconductor devices

Convergence within 20–50 iterations

Comparable to SPICE with compact models

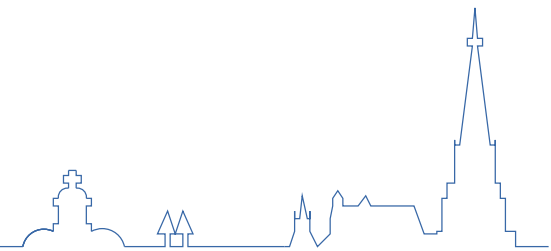


Examples

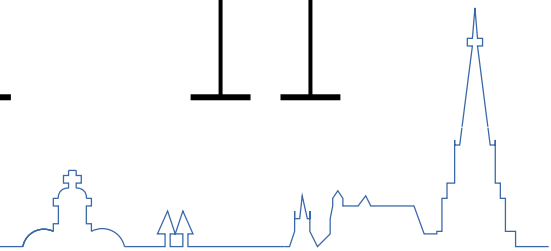
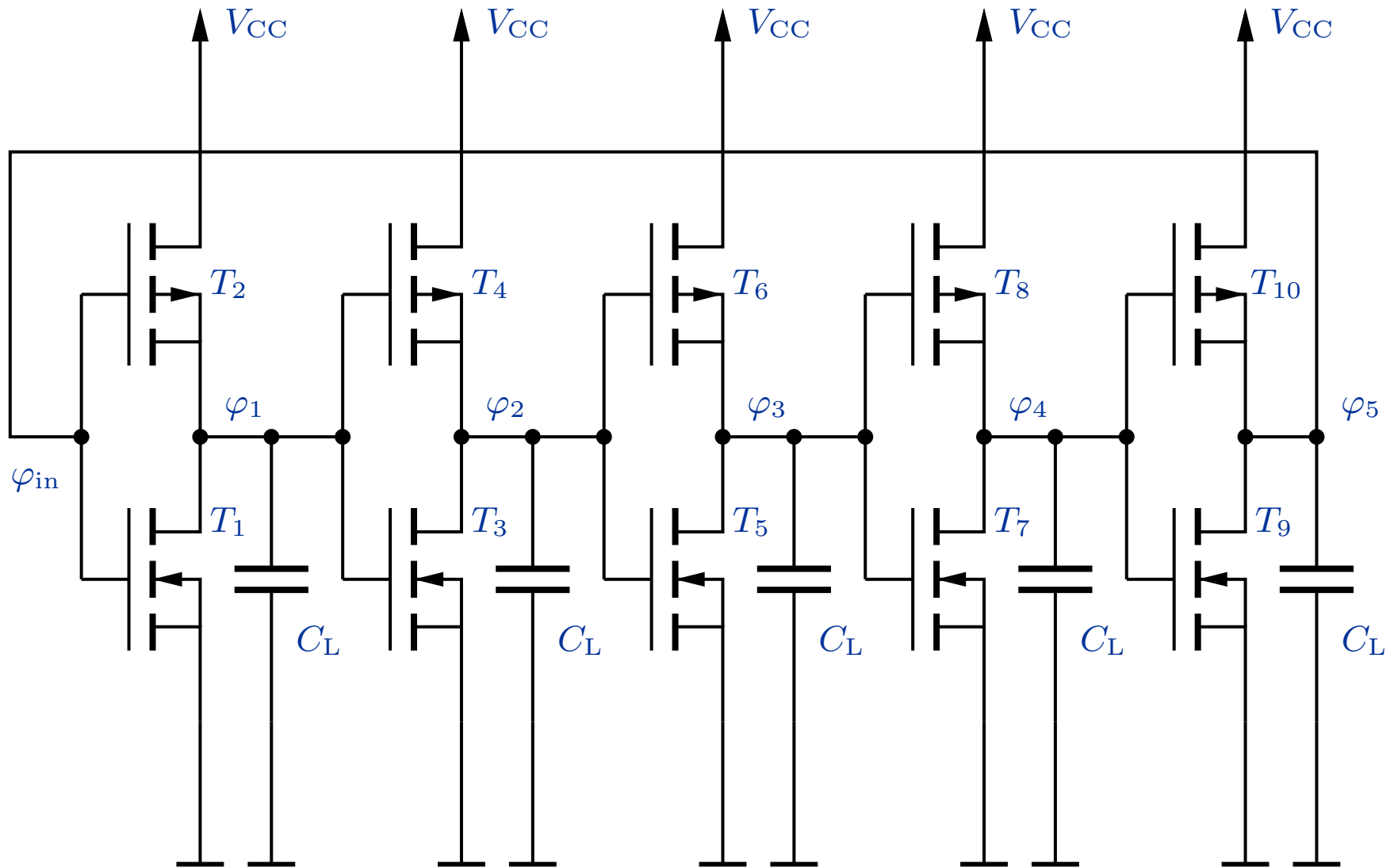
Five-stage CMOS ring oscillator

Long-channel/short-channel behavior

Electro-thermal analysis of an operational amplifier ($\mu\text{A}709$)



Five-Stage CMOS Ring Oscillator



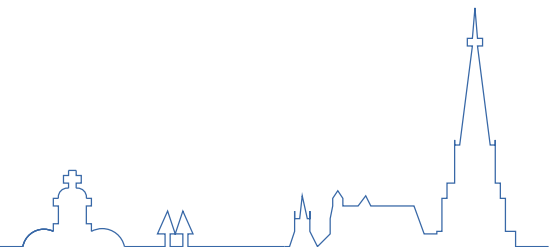
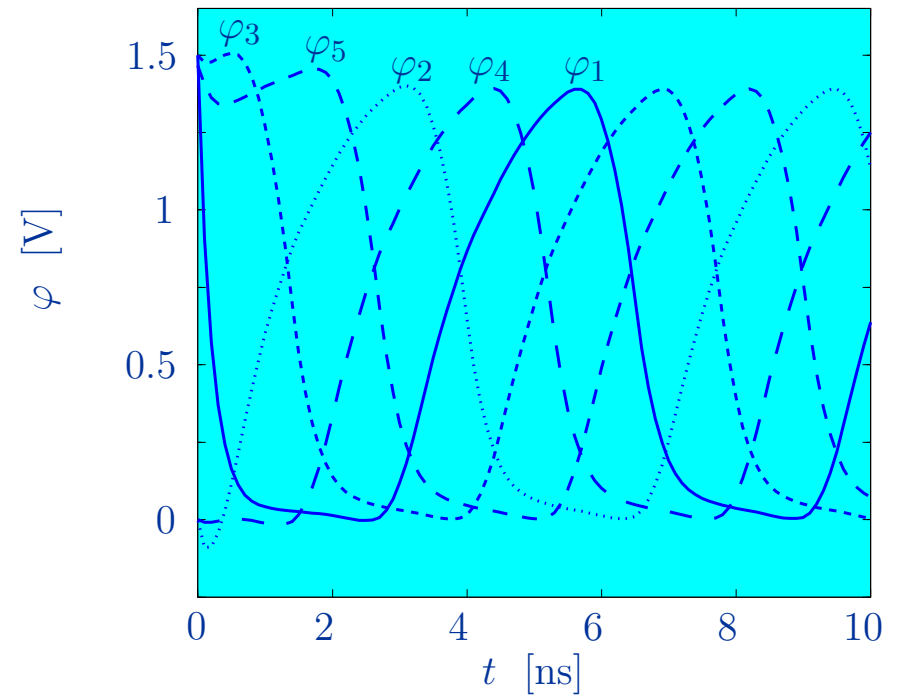
CMOS Ring Oscillators

Long-channel devices ($L_g = 2 \mu\text{m}$)

First timestep: $\varphi_{\text{in}} = 0 \text{ V}$

Excellent agreement DD and ET

Non-local effects negligible



CMOS Ring Oscillators

Long-channel devices ($L_g = 2 \mu\text{m}$)

First timestep: $\varphi_{\text{in}} = 0 \text{ V}$

Excellent agreement DD and ET

Non-local effects negligible

Short-channel devices ($L_g = 0.13 \mu\text{m}$)

Significant difference DD and ET

Non-local effects important

Larger currents for ET

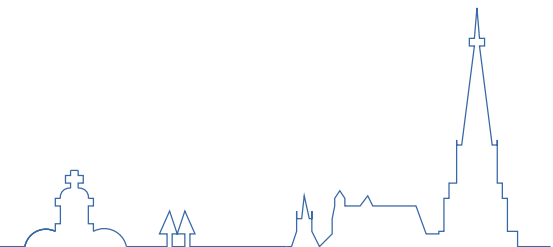
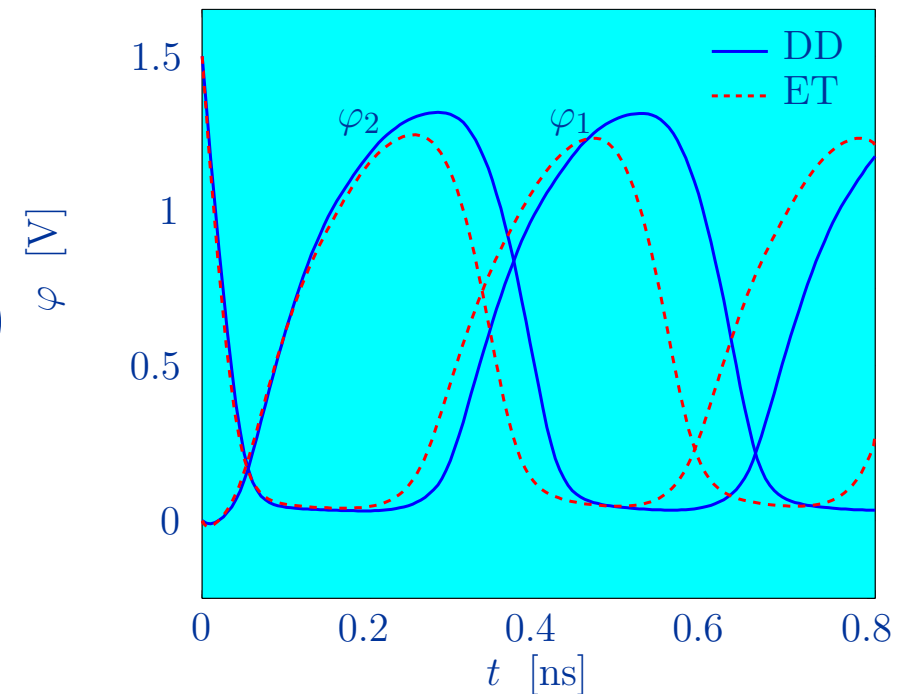
15% difference in delay time

Complexity of models can be increased

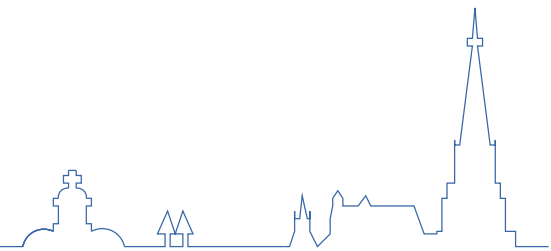
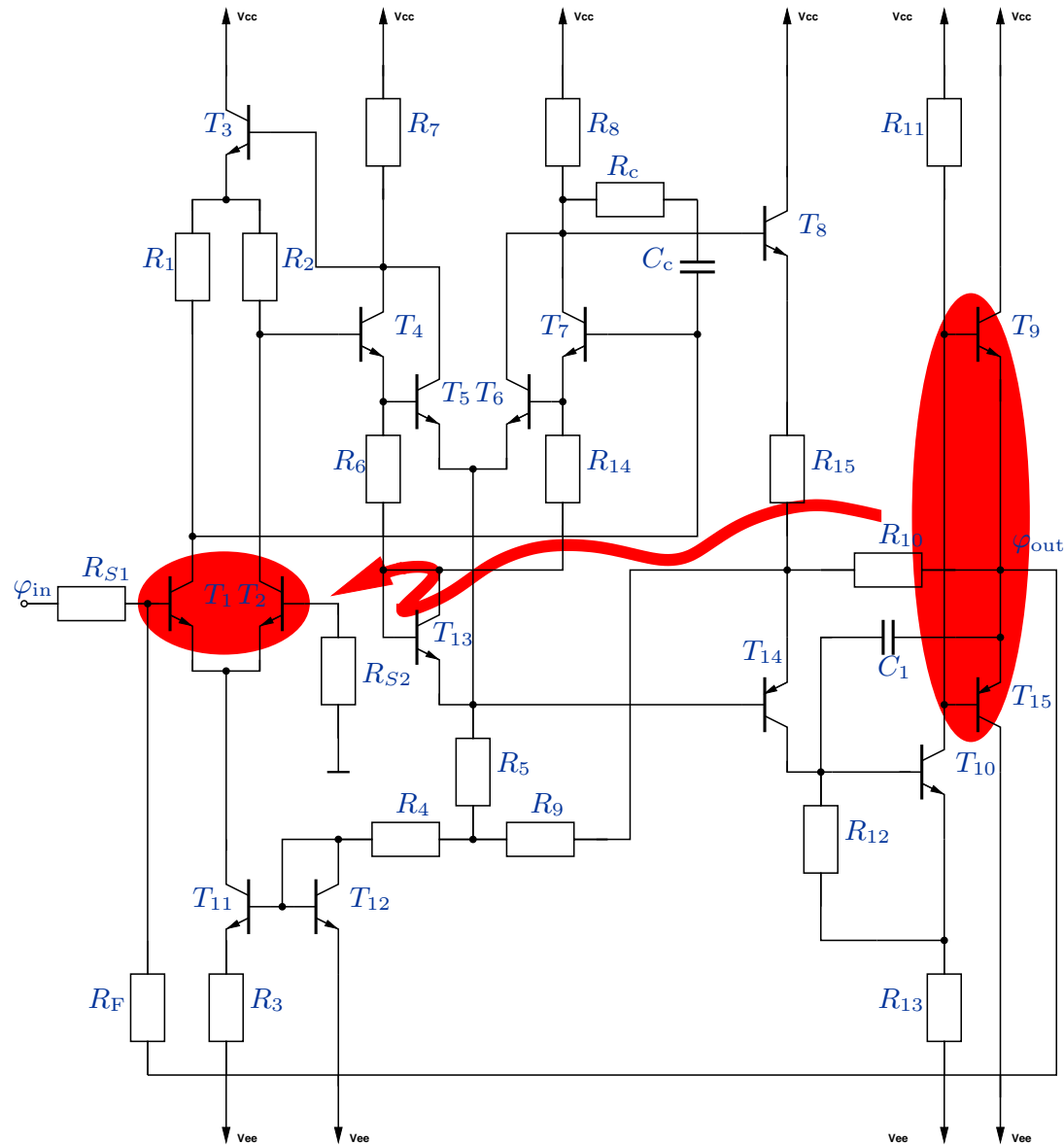
Higher-order transport models

More accurate quantum corrections

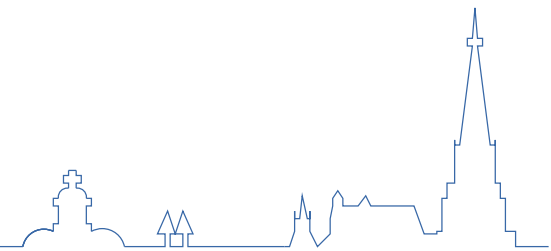
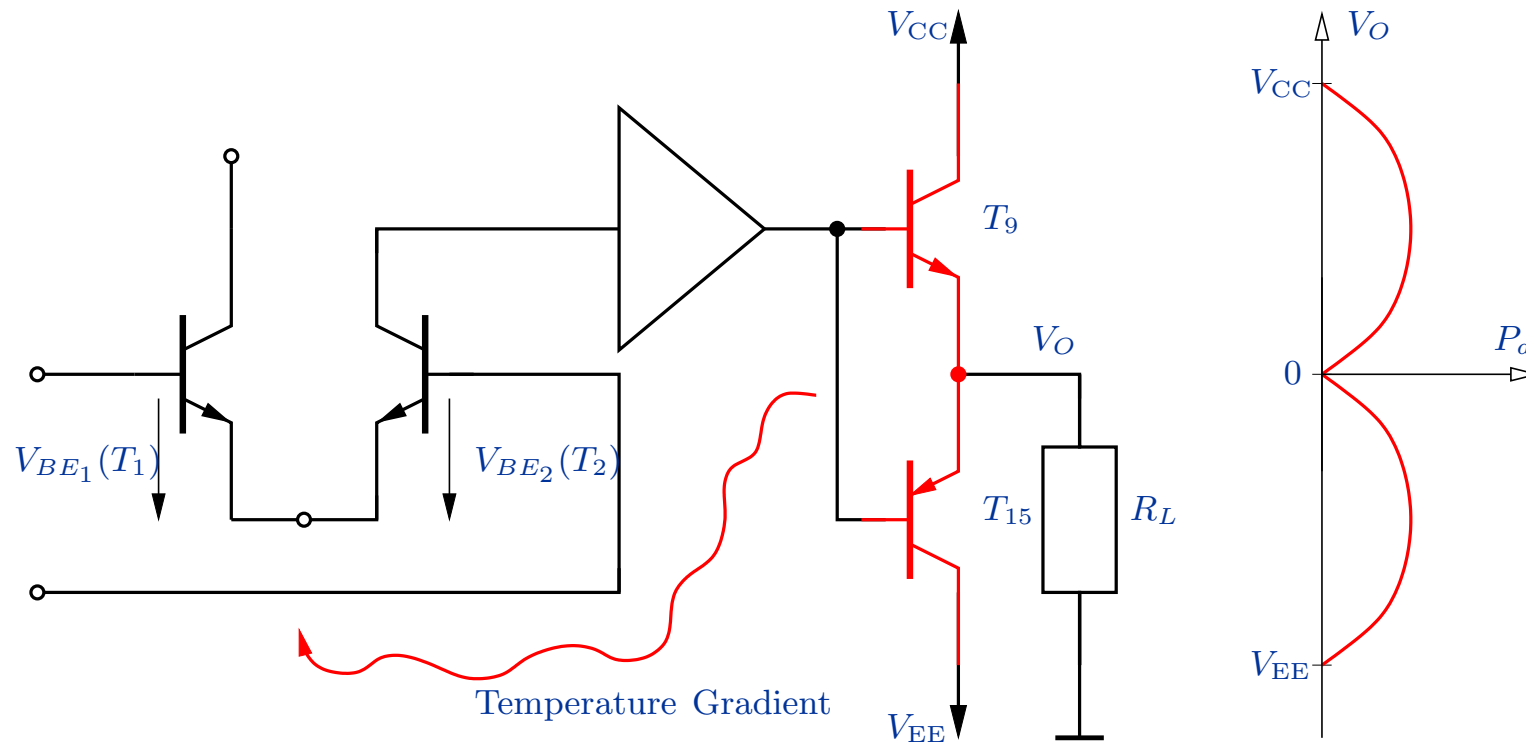
Different mobility models



Electro-Thermal Analysis of a $\mu\text{A}709$



Electro-Thermal Analysis of a μ A709



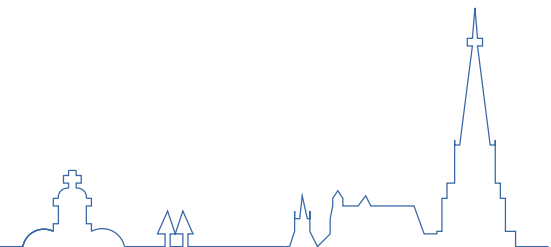
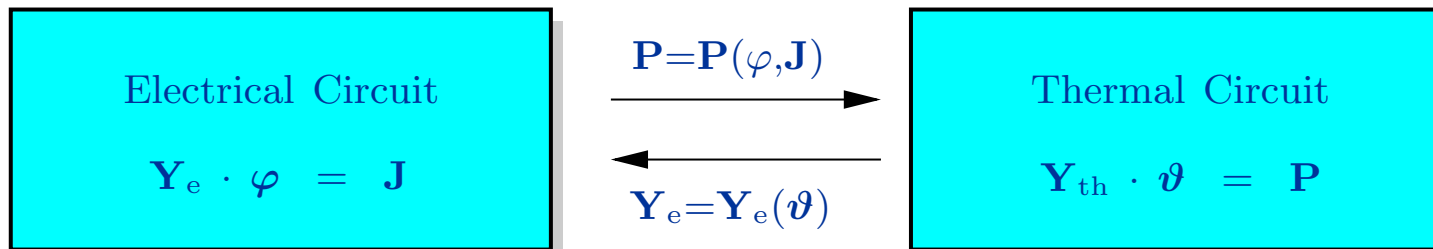
Thermal Circuit

Thermal coupling modeled via a thermal circuit

Thermal coupling between individual devices

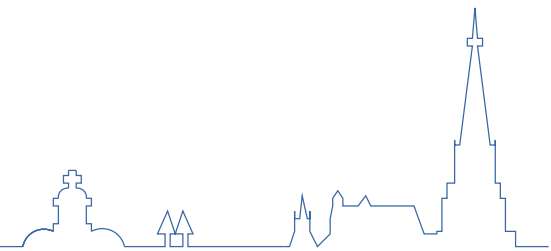
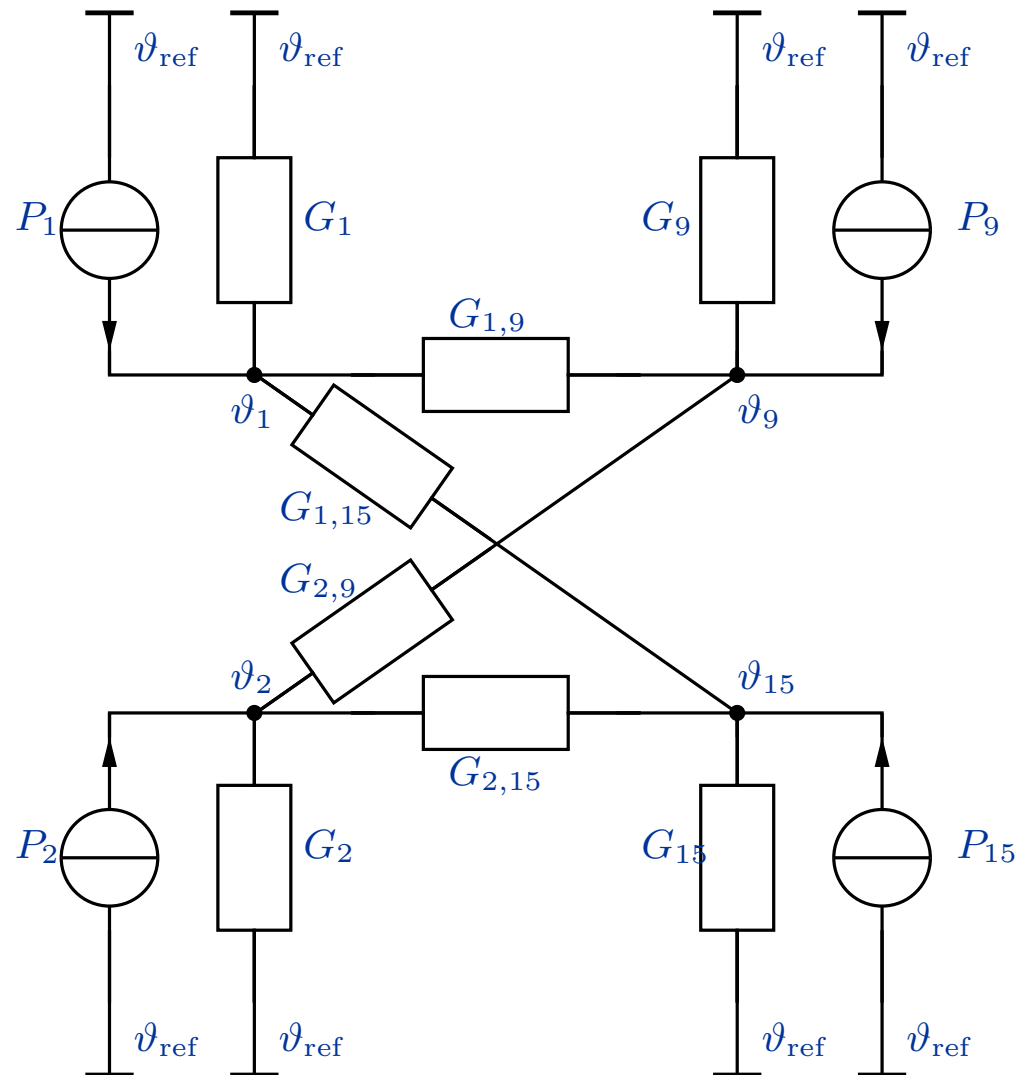
Thermal equations similar to Kirchhoff's equations

Formally derived from the discretized lattice heat-flow equation



Electro-Thermal Analysis of a μ A709

Simple thermal equivalent circuit

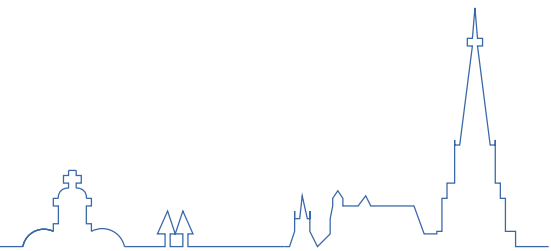


Electro-Thermal Analysis of a μ A709

Electrical simulation

All 15 transistors numerically simulated

System-size: 37177, simulation time: 1:08 hours (101 points, DC transfer)



Electro-Thermal Analysis of a μ A709

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Electro-thermal simulation

Input and output stage with self-heating (4 Transistors)

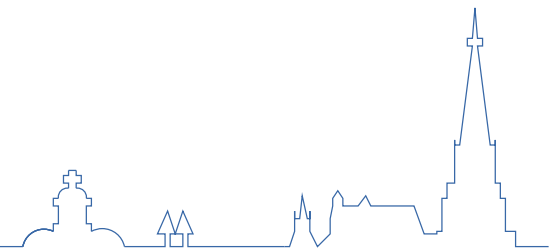
Thermal coupling effects

Thermal feedback from the output to the input stage

Thermal interaction between all 4 transistors

Highly non-linear problem, complex convergence behavior

System-size: 40449, simulation time: 3:08 hours



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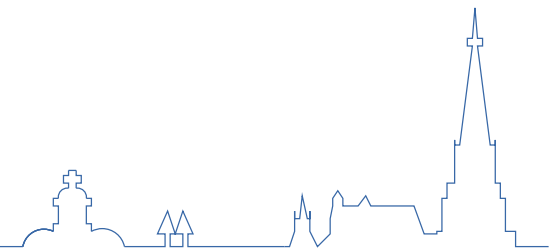
System-size: 40449, simulation time: 3:08 hours

Electro-thermal simulation with simplified self-heating model

Same coupling effects as before

Practically same results

System-size: 38477, simulation time: 1:22 hours



Electro-Thermal Analysis of a μ A709

DC Stepping

Gain ≈ 35000

$\Delta\varphi_{\text{out}} = 0.7 \text{ V}$ (101 points)

Critical point 0 V

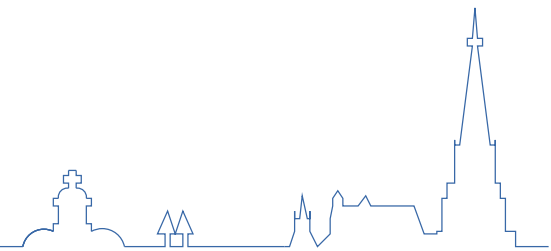
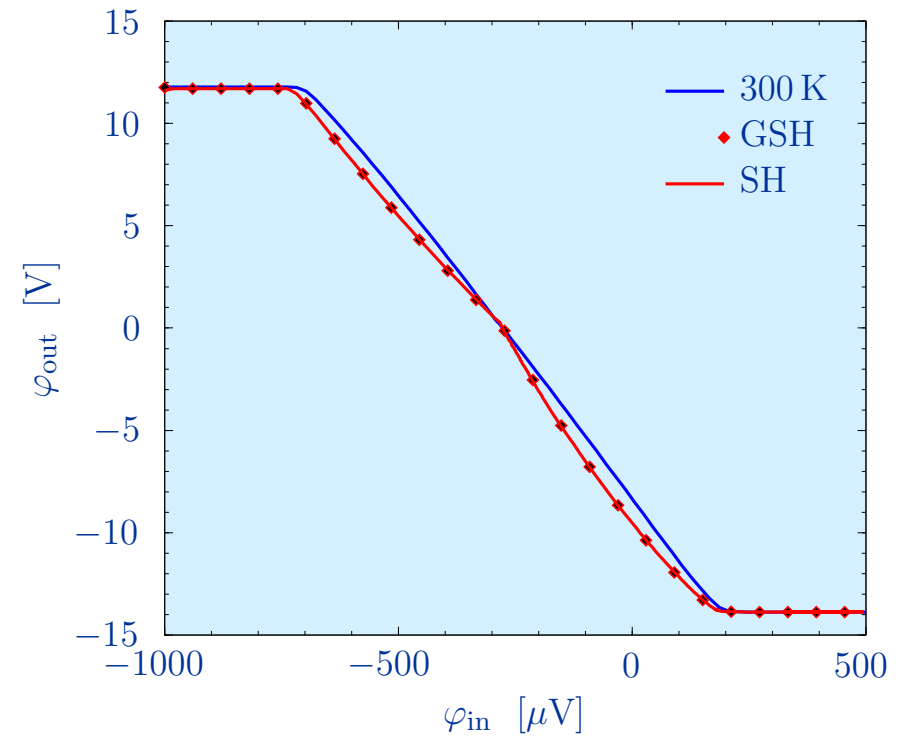
Thermal feedback caused bumps

Input stage: ΔT

$\Delta T \propto P$

$\max(\Delta T) = -22 \text{ mK}$

Input voltage difference



Electro-Thermal Analysis of a μ A709

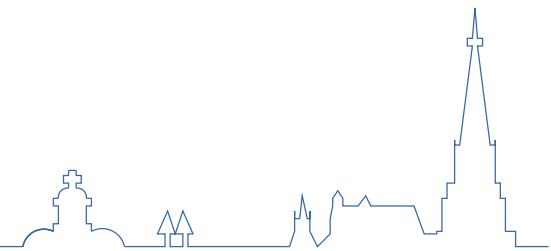
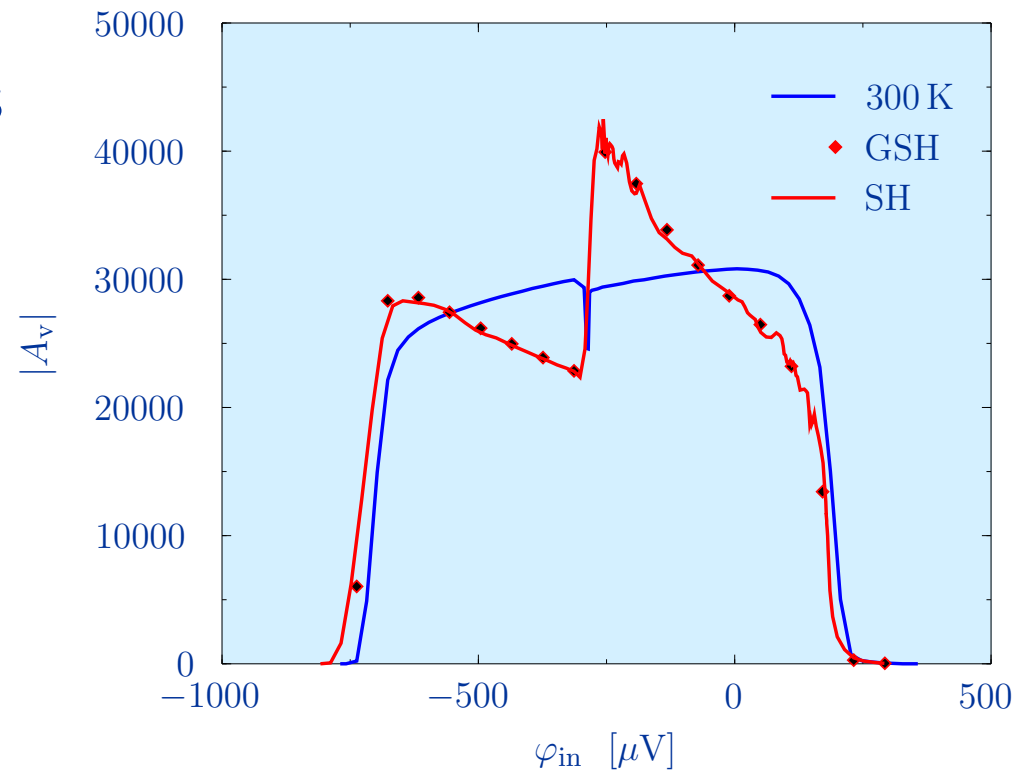
Open-loop voltage gain $|A_v|$

Optimistic thermal conductances

Stronger impact published

$|A_v|$ can even change sign

OpAmp can become unstable



Conclusions

For circuit design compact models are indispensable

Intermediate phase when devices structures is not established

Mixed-mode circuit/device simulation can be used

Motivation for mixed-mode device-circuit simulation

When compact models are inconvenient/not available

Verification of compact models in a more realistic environment

Optimization of devices

Exploitation of new device designs

Examples have been simulated with MINIMOS-NT

Go to <http://www.iue.tuwien.ac.at> and try it

