A Physically Based, Scalable MOS Varactor Model and Extraction Methodology for RF Applications

James Victory[1], Zhixin Yan[1], Gennady Gildenblat[2], Colin McAndrew[3], Jie Zheng[1]

1 Jazz Semiconductor, Newport Beach, CA

2 Pennsylvania State University, State College, PA

3 Freescale Semiconductor, Tempe, AZ , USA

Outline

- Introduction
- Frequency Dependent Analytical Surface Potential Based MOS Capacitance Model (Implemented in VerilogA)
- MOS Varactor Model (Implemented in VerilogA)
- Physical Parameter Extraction
- Model Verification
- Conclusions

Introduction (1)

- **MOS Varactor Modeling Prior Art:**
  - Force MOSFET model, BSIM usually the choice, to emulate MOS capacitor
    - Float source and drain to force deep depletion
    - Kinks in accumulation-depletion interface, heart of CV tuning in varactor
  - Polynomial CV equations, no physical basis
  - Reasonable models for parasitics*
  - Verification over limited geometry, most papers show only 1 geometry
    - No emphasis on extraction
  - References

K. Molnar, G. Rappitsch, Z. Huszka, and E. Seebacher, “MOS Varactor Modeling With a Subcircuit Utilizing the BSIM3v3 Model”, *IEEE Trans. Electron Devices*, vol. 49, no. 7, pp. 1206-1211, July 2002

C. Geng, K. S. Yeo, K. W. Chew, J. Ma, and M. A. Do, “A Simple Unified Scaleable RF Model for Accumulation-Mode Varactor”, *Proc. 2000 ICDA*

*S. Song and H. Shin, “An RF Model of the Accumulation-Mode MOS Varactor Valid in Both Accumu-lation and Depletion Regions”, *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1997-1999 , September 2003

Introduction (2)

- **Key things to get right:**
  - Physical CV equation dependent on process and geometry parameters to allow accurate statistical modeling
    - Cmax/Cmin, tuning range variation with geometry
    - Accurate dC/dV critical for VCO phase noise
  - Accurate models for device resistance over geometry
    - Combined with C yields accurate quality factor (Q) key to VCO phase noise
    - Provides designer ability to trade off tuning range for Q
    - Allows accurate statistical modeling
  - Proper dependence of metal parasitics on device layout
    - Parasitics included as part of model, not extraction decks!
    - Poor layout of MOS Varactor needs to be known up front

Frequency Dependent Analytical Surface Potential Based MOS Capacitance Model (1)

- Inversion charge in MOS capacitor thermally generated, not supplied by source/drain regions as in MOSFET
- Full solution requires inclusion of continuity equations, not practical for circuit simulation
- Inversion charge relaxation time approximation provides reasonable physical model suitable for circuit simulation
- Analytical surface potential solutions incorporated based on work for SP (Penn State) MOSFET model.
- Important for VCO design where DC biasing in inversion, allowing inversion charge to form, will change the frequency response
  - Different than DC biasing in depletion with RF signal swinging into inversion region, inversion charge has no time to form.
- Developed and verified with device simulation in DESSIS

Frequency Dependent Analytical Surface Potential Based MOS Capacitance Model (2)

$$\frac{dq_i}{dt} = \frac{q_i^{(0)} - q_i}{\tau}$$

Inversion charge (normalized) relaxation equation,

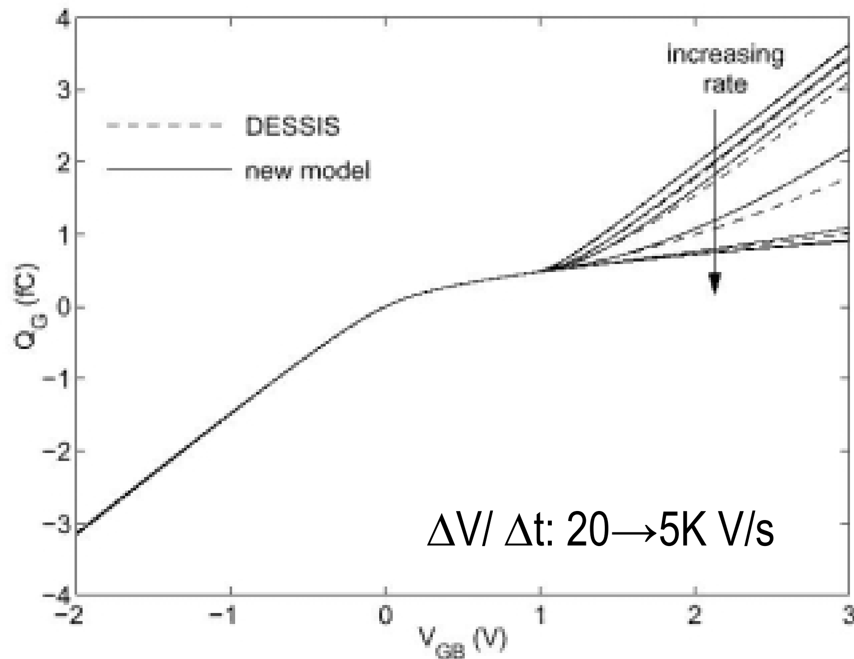
$q_i^{(0)}$: static inversion charge generated from static analytical surface potential

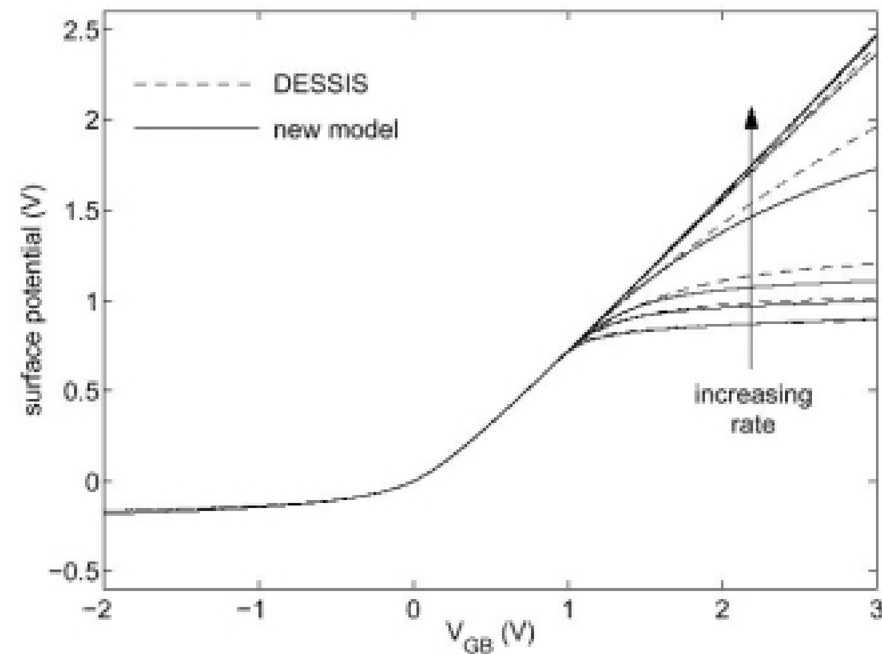
$$[V_{GB}(t) - V_{FB} - \psi(t) - q_i(t)]^2 = \gamma^2 \Phi_t [u - 1 + \exp(-u)]$$

Time dependent surface potential equation

$$u = \frac{\psi(t)}{\Phi_t}$$

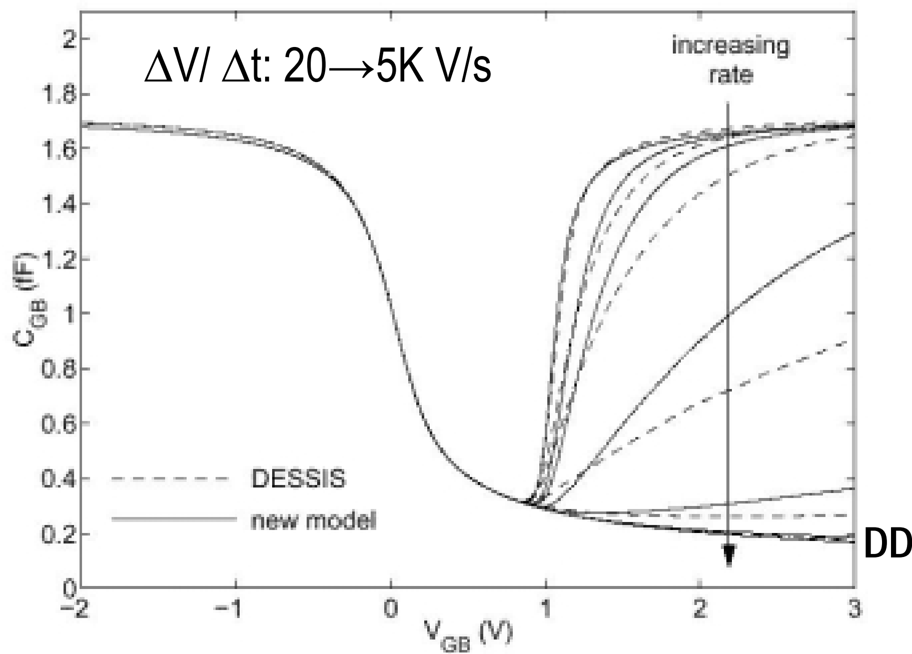
normalized surface potential



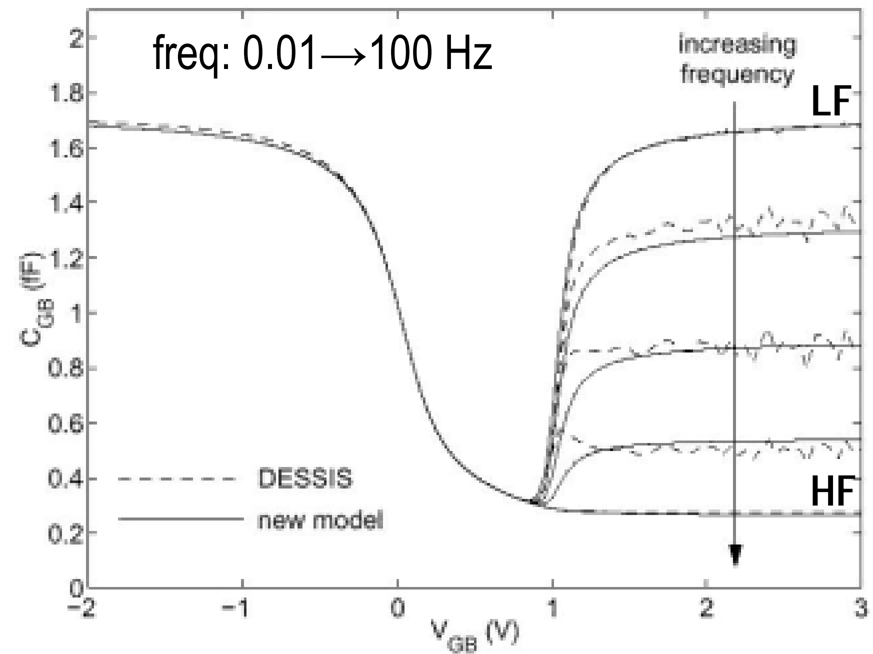


Frequency Dependent Analytical Surface Potential Based MOS Capacitance Model (3)

Transient



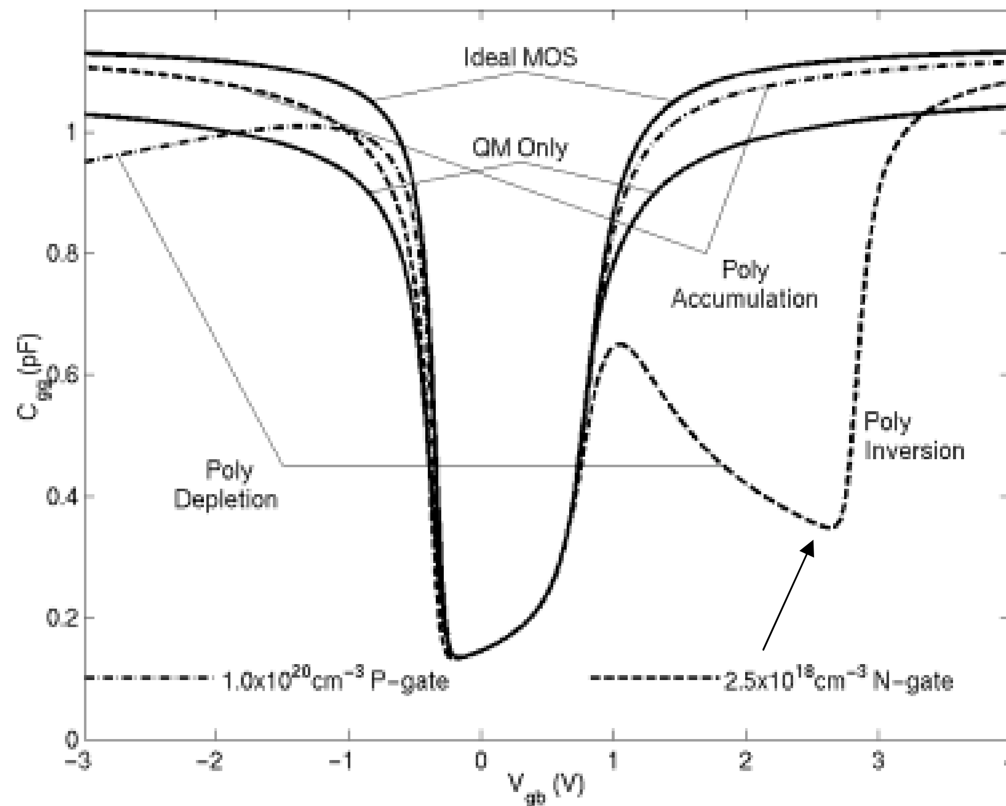
AC



QM and PD effects

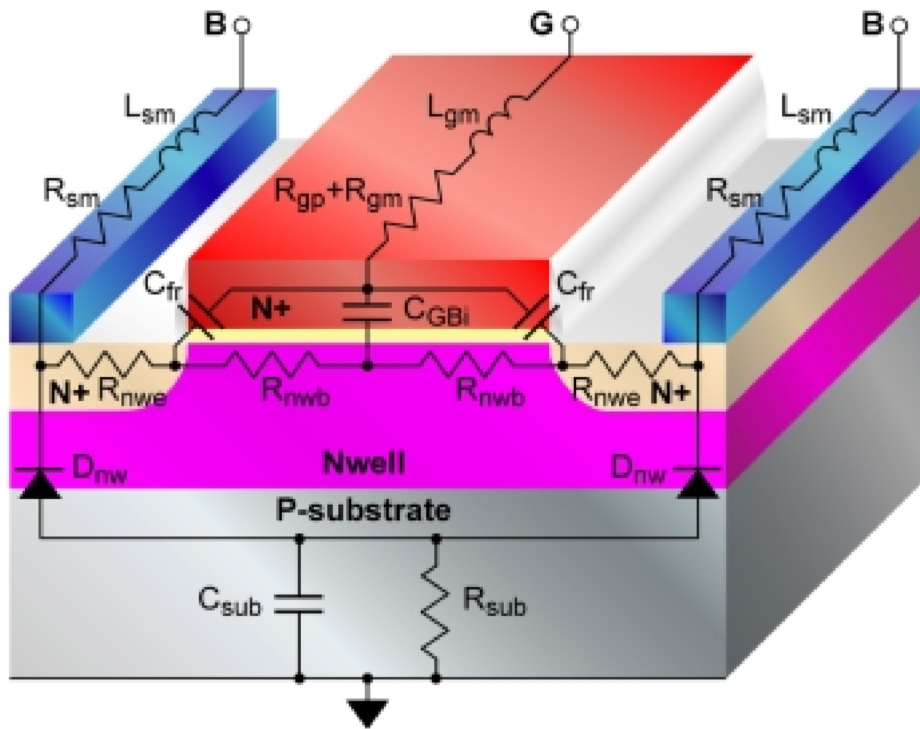
Innovation Manufactured

- All QM and PD effects included in model
- poly inversion included for completeness, unlikely in practice



MOS Varactor Model and X-section

Innovation Manufactured



- C_{GBi}: MOS cap intrinsic tuning element
- C_{fr}: fringing and overlap capacitance, degrades tuning for short Lg

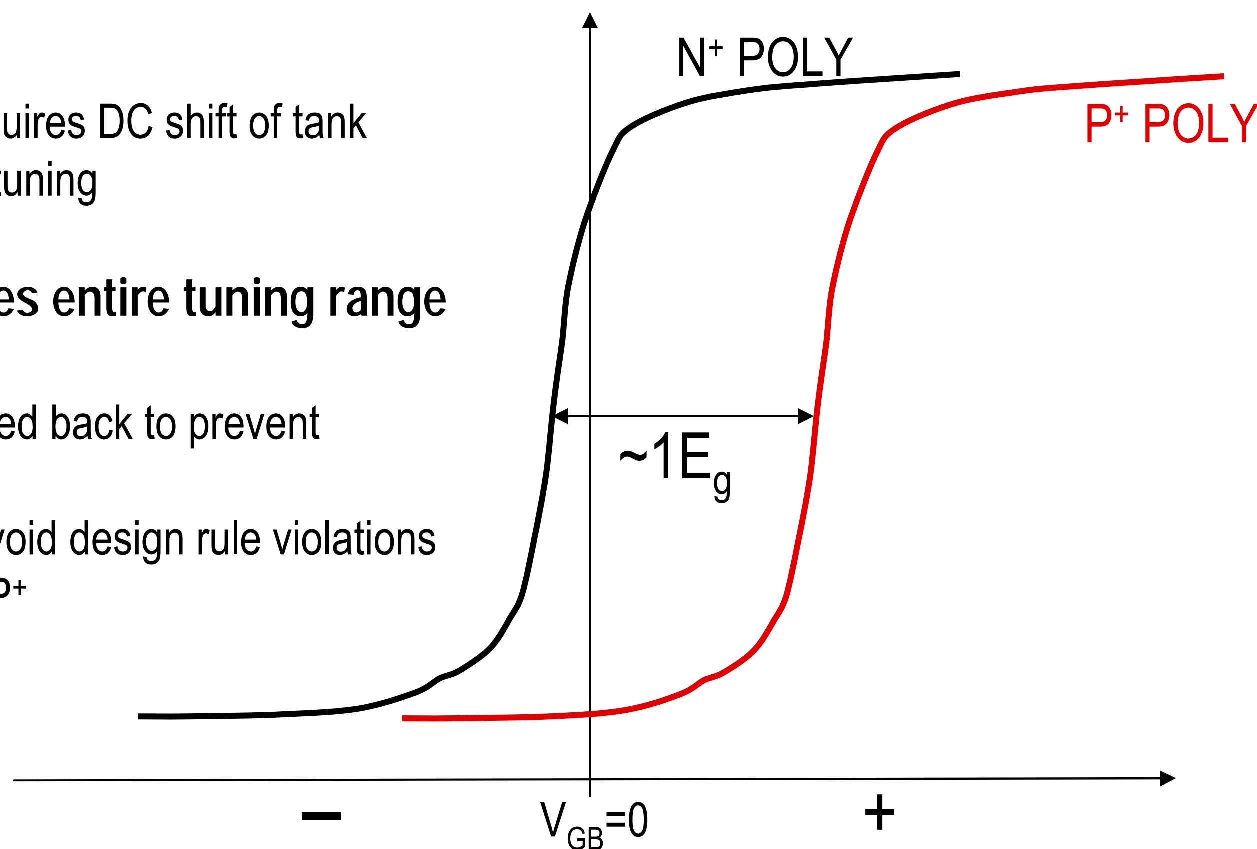
- $R_{nwb}+R_{nwe}$: Nwell resistance dominates
- R_{nw} voltage dependence negligible
  - 0.18μm and below due to heavy doping
  - Accumulation resistance model included in references
- Rgp: gate poly resistance (horizontal salicided and vertical sal-poly contact)
- Rgm, Rsm: interconnect resistance including metal and vias, calculated from sheet ρ, geometry and finger configuration
- Lgm, Lsm: interconnect inductance calculated from Greenhouse, geometry and finger configuration
- Dnw: well-substrate diodes
- Rsub, Csub: substrate network to match y22, usually not important since Nwell is tuning node

N+ vs. P+ Poly

Innovation Manufactured

- **N^+ poly on Nwell by self-alignment allows for shortest Lg**
  - highest Q
  - typical VCO biasing requires DC shift of tank voltage to allow for full tuning

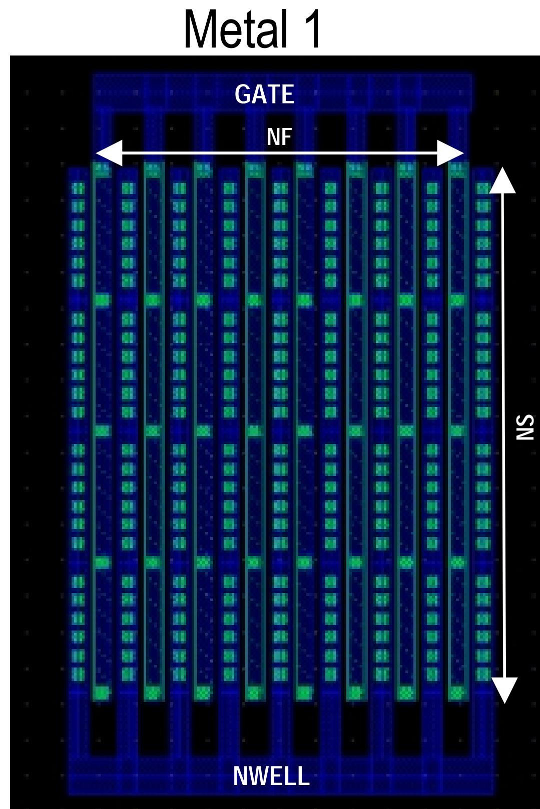
- **P^+ poly on Nwell provides entire tuning range on $+V_{GB}$ axis**
  - N^+ contact to Nwell pulled back to prevent counter doping of poly
  - Lg > Lmin to allow to avoid design rule violations in implanting poly with P^+
  - decreases Q



MOS Varactor Layout and Metal Connection Considerations

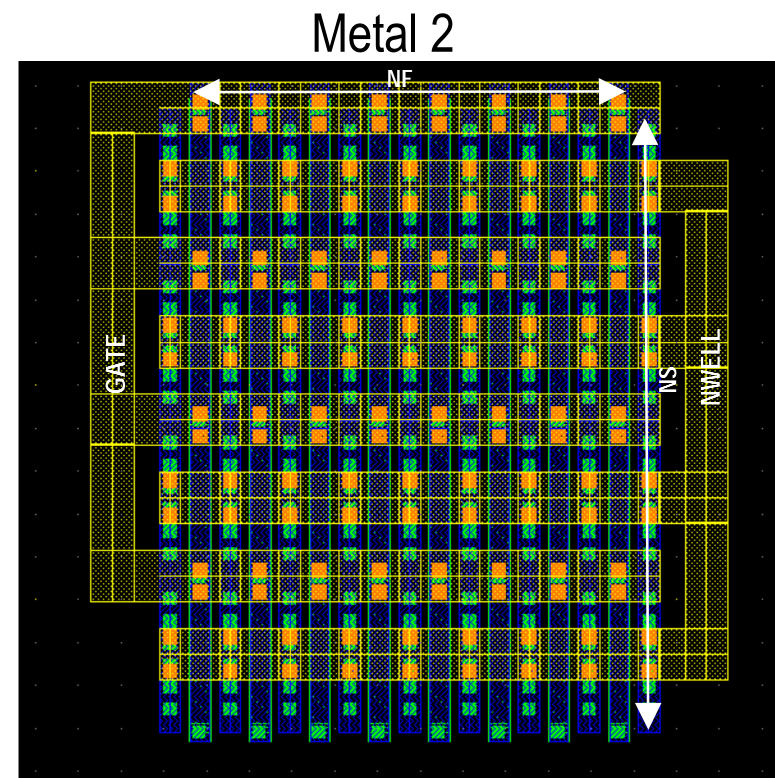
Innovation Manufactured

Metal 1



VS.

Metal 2

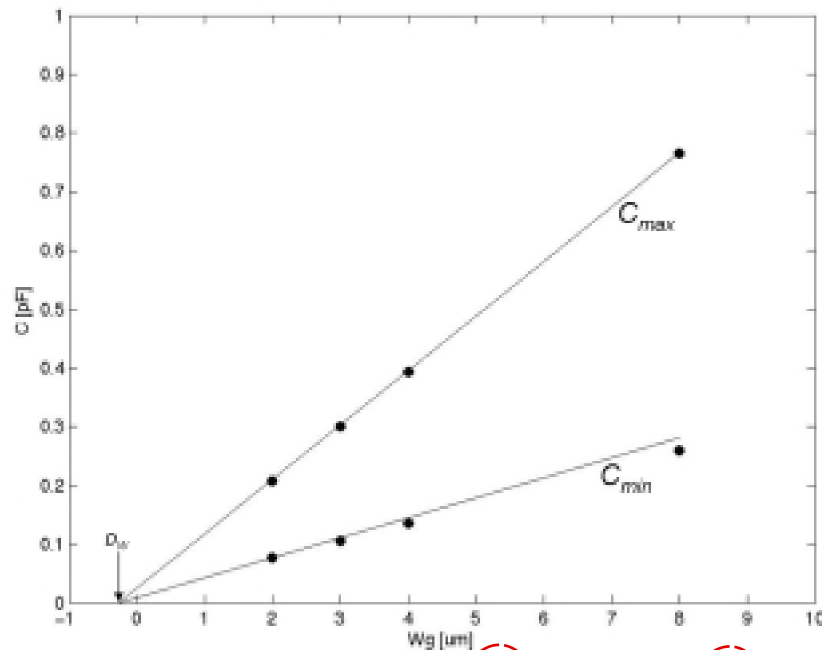


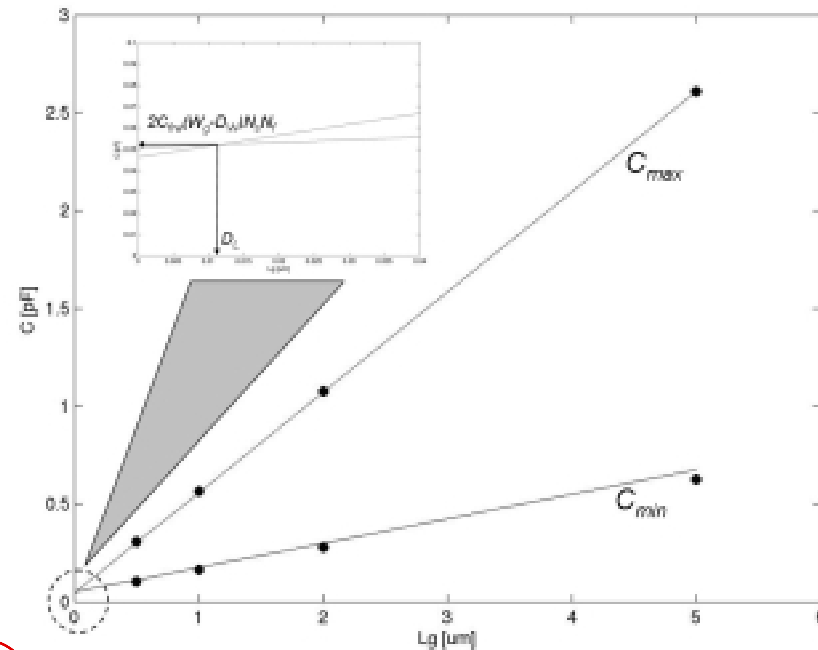
- Metal R and L ~ NS/NF (segments)
- High metal resistance (thin M1)
- Low metal capacitance (M1-M1)

- Metal R and L ~ NF/NS (fingers)
- Low metal resistance (wide M2)
- High metal capacitance (M2-M1)

Parameter Extraction: Scalable MOS Capacitance
(All extraction and verification performed on 0.18μm technology)

- Regression fitting of C_{max} and C_{min} on W_g and L_g yields D_L, D_W, C_{frw}
- T_{ox}, N_b (well doping), QM, and PD parameters extracted from large plate capacitor





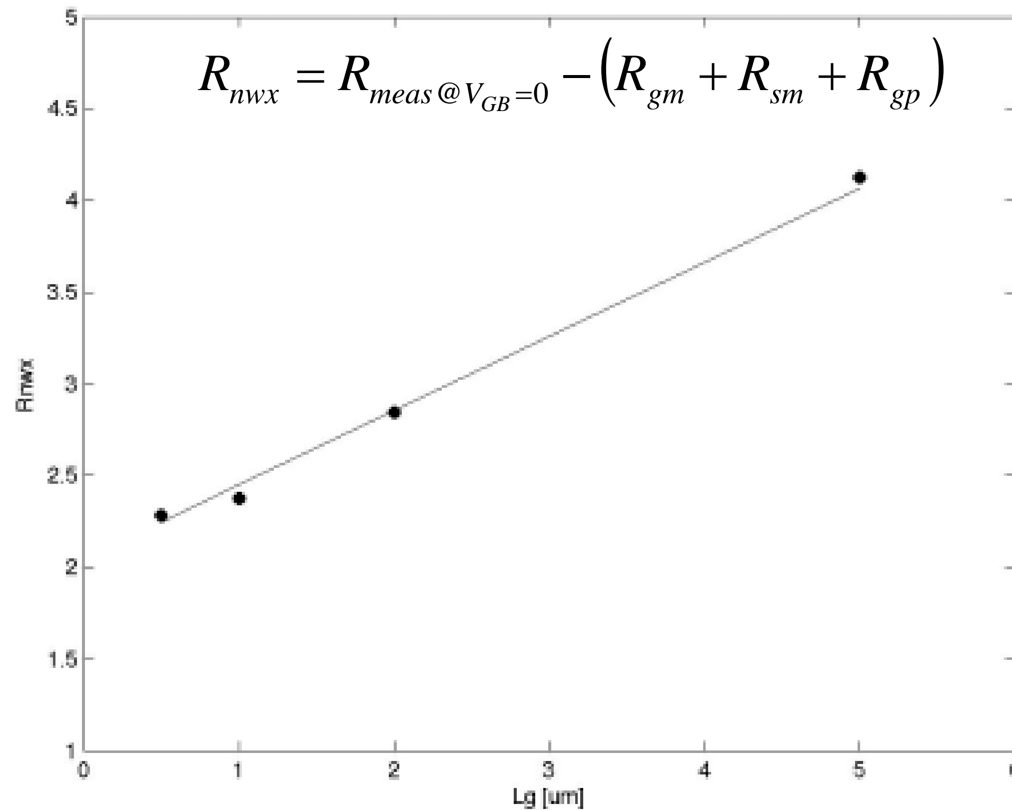
$$C_{max} = \left(C_{ox} \cdot \left(L_g - D_L\right) \cdot \left(W_g - D_W\right) + 2C_{frw} \cdot \left(W_g - D_W\right)\right) \cdot \left(N_s \cdot N_f\right)$$

$$C_{min} = \left(\frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}} \cdot \left(L_g - D_L\right) \cdot \left(W_g - D_W\right) + 2C_{frw} \cdot \left(W_g - D_W\right)\right) \cdot \left(N_s \cdot N_f\right)$$

Scalable NWELL Resistance Model Extraction (1)

Innovation Manufactured

- Nwell resistance dominates
- Rgp, Rgm, and Rsm calculated from physical equations and subtracted from measured resistance



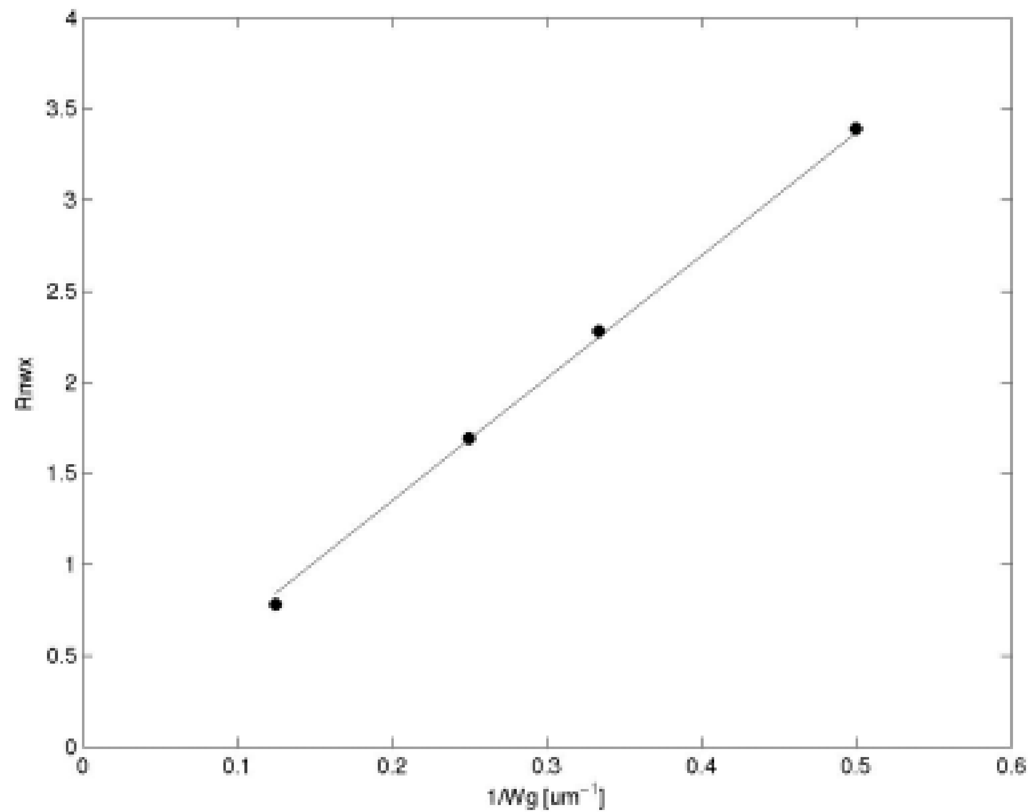
$$R_{nwell} = \frac{R_{end}}{Wg} + \frac{\rho_{nw} \cdot Lg}{Wg \cdot 12}$$

Lg=0 intercept yields R_{end}

Slope yields ρ_{nw}

Scalable NWELL Resistance Model Extraction (2)

- Plot of measured and extracted Rnwx vs. 1/Wg verifies extraction procedure



MOS Varactor Model Verification (C&Q): Varying Lg

3x0.5x2x10 | 3x1x2x10 | 3x2x2x10 | 3x5x2x10

Cgb [pF]

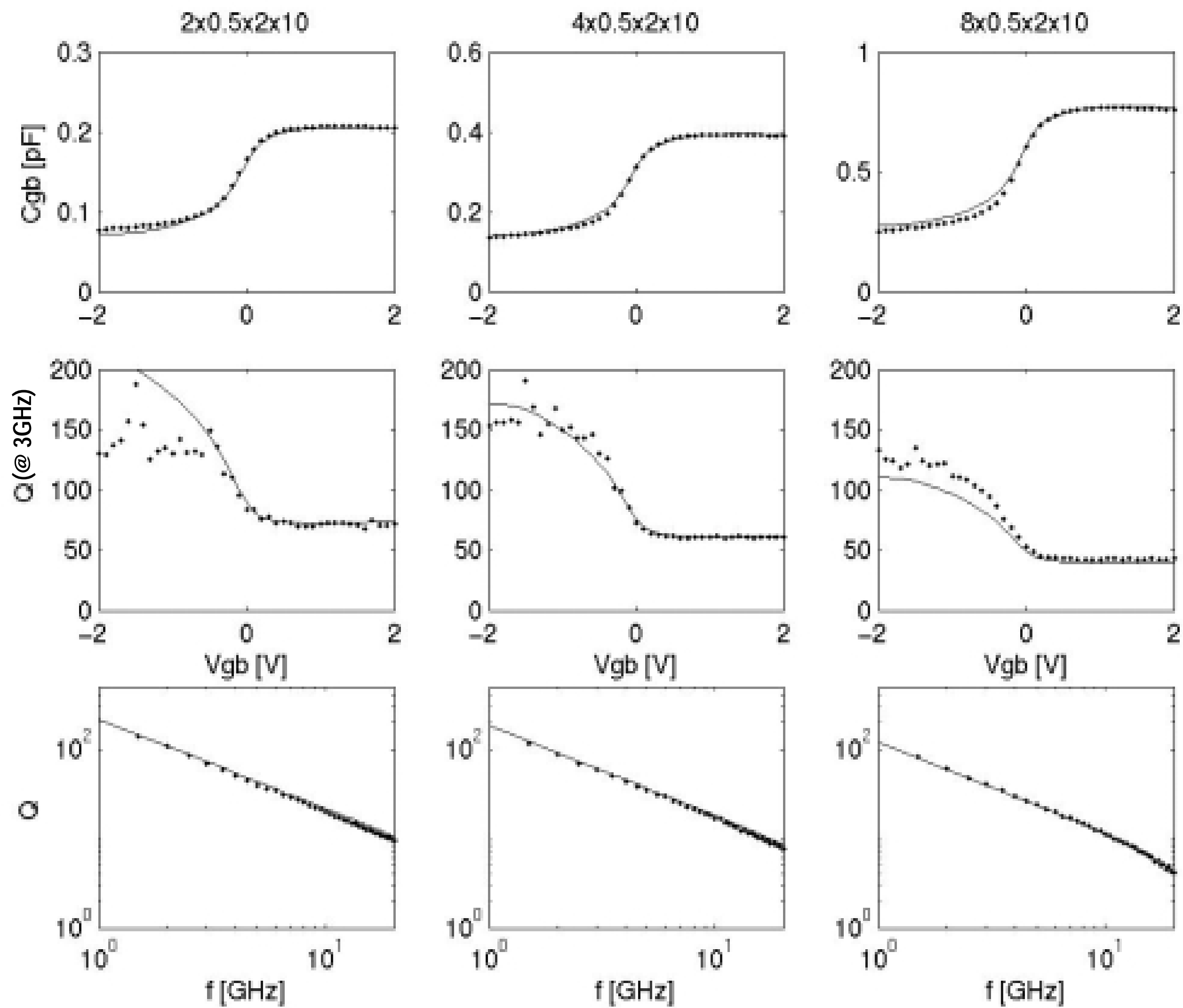
Q (@ 3GHz)

Vgb [V]

Q

f [GHz]

MOS Varactor Model Verification (C&Q): Varying Wg



MOS Varactor Model Verification (C&Q): Varying NsxNf

3x0.5x5x4

3x0.5x10x2

Cgb [pF]

Q (@ 3GHz)

Vgb [V]

Q

f [GHz]

Inductor influence

Conclusions

- First time Frequency Dependent Analytical Surface Potential Based MOS Capacitance Model, protects design from improper biasing.
- Physical scalable models for device parasitics to ensure accurate CV and Quality Factor (Q) simulation
  - Scalable model provides designer option to trade CV tuning vs. Q
  - Physical parameter set and model provide foundation for accurate statistical modeling of process variation
- References for this material:

J. Victory, C. C. McAndrew, and K. Gullapalli, "A Time-Dependent, Surface Potential Based Compact Model for MOS Capacitors", IEEE Electron Device Lett., vol. 22, no. 5, pp. 245-247, May 2001

J. Victory, Z. Yan, G. Gildenblat, C.C. McAndrew, J. Zheng, "A Physically Based, Scalable MOS Varactor Model and Extraction Methodology for RF Applications," ***IEEE Trans. Electron Devices*****, vol. 52, no. 7, pp. 1343-1354, July 2005**