Challenges & Strategies for the SPICE Model Extraction & Simulation of the PD-SOI Technology

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Outline

- Bulk CMOS vs. PD-SOI CMOS
- Self-heating
- Floating-Body Modeling: History-Effect
  - Definition
  - Underlying Physics
  - Key Components & Their Impacts
- Parameter Extraction Flow
- Challenges in Measurement & Extraction
- Tied-Body Modeling
  - History-Effect in Tied-Body CMOS
  - Parasitic Gate Capacitance
  - Distributed Body Resistance
- Conclusion
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Bulk CMOS vs. PD-SOI CMOS

- The chief difference of the PD-SOI is that the body of each SOI transistor is an independent 4th terminal for the device.
- When absolutely needed, the body can be fixed to a chosen potential with a body tie:

However, in 99.9% of the chip, transistors will be operating as floating body devices.
Self-Heating

- Thermal conductivity
  - $K_{si} = 60 - 148 \text{W/mK}$
  - $K_{ox} = 0.2 - 1.2 \text{W/mK}$
- Relatively poor modeling
- Occasional convergence issue
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CMOS Inverter Operation
Definition of History-Effect

1st switch: input transition after being held constant for a long time.

2nd switch: input transition short time after the 1st switch.

\[ H = \frac{\tau_{1st} - \tau_{2nd}}{\tau_{2nd}} \]
**Typical History-Effect**

- Delay is subject to switching history of the logic gate.

**Evolution of Switching Delay**

- $t_r=t_f=0.8\,\text{ns}$
- $t_{\text{per}}=40\,\text{ns (50\% duty)}$
- step=100\,\text{ps}

**Input Clock Shape**
What Causes History-Effect?

- Body Potential is a function of:
  - Capacitive coupling to
    - Source
    - Drain
    - Gate
    - Substrate (small)
  - Diode Leakages to
    - Source
    - Drain
  - Gate Leakage
  - Impact Ionization
- Also subject to the previous switching history
Combined Capacitive/Resistive Network

C1 R1 C2 R2

R-Divider

C-Divider

RC Decay

R-Divider

Time

Voltage
Time for Actual Contribution to Speed

- 1st SW: Initial DC
- 2nd SW: Initial DC + Capacitive Coupling
Capacitive Coupling

- Capacitive coupling is stronger to drain than to gate.
Key Components (Initial DC Condition)

- **1st SW Initial**
  - KCL balance between forward and reverse $I_{dio}$
  - Accumulation $I_{gb}$ is much smaller than forward $I_{dio}$

- **2nd SW Initial**
  - KCL balance between forward $I_{dio}*2$ and inversion $I_{gb}$
Key Components (AC Coupling)

- Basically a voltage-divider that consists of:
  - gate-body capacitance and junction capacitance
- Drain AC coupling is more significant than gate AC coupling

\[ \Delta V_{bs} = V_{DD} \frac{C_{j,rev}}{C_{gb,acc} + C_{j,for} + C_{j,rev}} \]
Key Components (Body-Effect)

- Body potential is established mostly by diode and gate characteristics (DC & AC).
- This body potential is translated into the actual switching performance by the body-effect (the main transfer function).
Impact of Gate Capacitance & Current

- $C_{gb}$ is critical for $V_{DD}$ dependence slope
- $I_{gb}$ is a major factor in 130nm technology and below

\[ \Delta V_{b,2nd} = V_{DD} \frac{C_{db}}{C_{gb} + C_{sb} + C_{db}} \]
**Impact of Diode Current**

- The diode current characteristic is the key characteristic dominating the $V_{DD}$ and temperature dependences of the history-effect:
  - Proportional to forward Idiode
  - Inversely proportional to reverse Idiode

![Forward $I_{diode}$ Level Impact](image)

![Reverse $I_{diode}$ Impact](image)
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Intrinsic MOSFET characteristics has only small impact on history effect.
PD-SOI Parameter Extraction Procedure

- **Body-Effect & Cg Fitting**
  - Very Crude IV Fitting
    - Body Currents Fitting ($I_{diode}, I_{gb}, \text{etc}$)
  - Check History Effect
    - Refine All IV Fitting

- Tied Body
- Floating Body
Challenges in Measurement & Extraction

- Active
- Gate Poly
- P+ I/I

Parasitic Opposite Type Gate

Neck Easily Gets Fully-Depleted
Parasitic Opposite-Type Gate

- Big discrepancy in Igb characteristic due to the parasitic
  - Especially in inversion region
- Need a bulk wafer
Fully-Depleted Neck

- Low-doping neck can cause artifacts in measured data
Sometimes the body effect is not able to fit for the entire range. Then some range should be compromised. Separating TB and FB models maybe more desirable.
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Can Body Be Really Tied?

- Tied-body PD-SOI circuit experiences the coupling effects exactly same as floating-body one.
- Thus it exhibits history effect too.
BSIM-SOI: Gate Capacitance

Physical

Ap+  An+
Body

Source

BSIM-SOI

Agbc p

Drain

Source

Rbodyext  Rbp

p+/p-  n+/p-  n+/p

p+/p-  n+/p-  n+/p

Rbodyext  Rbp
BSIM-SOI: Gate Capacitance

Gate Capacitance

\[ Q_{GB} \approx \int_{V_{FB}}^{V_T} C_G \cdot dV_{GS} \]

\[ Q_{GC} \approx \int_{V_T}^{V_{DD}} C_G \cdot dV_{GS} \]

Over-Estimated
The charge ratio is 0.2~0.5 within practical range
  - 2 ~ 5x overestimation
  - Its impact of switching delay is not negligible
BSIM-SOI: Distributed Body Resistance

Distributed

Single Lumped

Measurement

Model

DC Values

AC Values?
BSIM-SOI: Distributed Body Resistance

**Rule of Thumb**
- Factor of $1/3$ for single-side contact; $1/12$ for double-side contact
- Mathematically derived for gate resistance noise
- Applicable for other distributed resistance associated with active gain

**Single-Side (T-Gate)**
- $W_N = W_p/2$
- $A_{gbcp} = A_{n+} + A_{p+}/3$
- $W_N = WP/2$, $= 5 \mu m$
- $W_N = WP/2$, $= 1 \mu m$

**Double-Side (H-Gate)**
- $A_{gbcp} = A_{n+} + A_{p+}/3$
- $R_{bodyext} = 10K\Omega$
- $W_N = W_p/2$
- $= 5 \mu m$
- $W_N = W_p/2$
- $= 1 \mu m$
Conclusion

- Self-heating is poorly modeled in general and worsens the convergence
- History-effect is one of the major difficulties in floating-body PD-SOI parameter extraction
  - It has to be taken care of in the early stage of extraction
  - Accurate measurement & extraction of key components are very tricky and challenging
- Tied-body PD-SOI parameters need to be carefully chosen for BSIM-SOI model
  - Parasitic gate capacitance needs to be scaled
  - Body resistance should be scaled by 1/3 for single-side; 1/12 for double-side