DC and AC modeling of minority carriers currents in ICs substrate

Camillo Stefanucci, Pietro Buccella, Maher Kayal and Jean-Michel Sallese
Swiss Federal Institute of Technology
Lausanne, Switzerland

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Outline

- Smart Power IC and existing design flow
- EPFL Substrate Model
  - DC examples
  - AC examples
- Model application and new design flow
Smart Power ICs

- High-voltage (50V) and low-voltage (5V) devices co-exists on the same chip
- Substrate triggered mechanisms cause destructive latch-up
- EPFL Substrate Model developed to simulate these effects during design

[1] B. Murari, Smart Power ICs, Springer-Verlag, 2002
Mixed-Signal Design flow

Design
Spice Simulation

Layout
Automation

Extract circuit parasitics from layout
Post-layout Simulation

Is Mixed-Signal Design Flow appropriate for robust High-Voltage / High Power Design?

Modify Schematics to meet design targets

Modify Layout to meet design targets

Foundry
Parasitic substrate currents

- Minority carriers’ propagation in the substrate
- Parasitic bipolar transistors automatically detected from layout
- EPFL Substrate Model is based on multi-junction parasitic current paths

Electrical circuit simulator neglects minority carriers!

EPFL Substrate Model

- **Physics** based model based on 1D drift-diffusion equation (**verilog-A**)
- 4-terminal devices: majority and **minority** carriers.
- Equivalent currents and voltages for minority carriers can be simulated at **circuit level**.
- Parasitic network extraction with a substrate **meshing** strategy.

**EPFL diode**

**EPFL resistance**

**EPFL contact**

Only diodes and resistors can simulate transistor effect!

Model under validation in AMS HV 0.35 μm and ST BCD 0.16 μm technologies
Model equivalent circuits

- **TCC** (Total Current Circuit) and **MCC** (Minority Carrier Circuit) highly coupled to model substrate conductivity modulation.

- Geometrical and technology (doping, lifetime...) input parameters for the model.

\[
G_{\text{min}} = \frac{qA}{\Delta x} (\mu_p + \mu_n) \hat{n}
\]

\[
G_0 = \frac{qA}{\Delta x} (\mu_p N_a + \mu_n n_0)
\]

\[
I_{\text{bulk}} = qA(D_n - D_p) \frac{d\hat{n}}{dx}
\]

\[
G_d = \frac{AD_n}{\Delta x}
\]

\[
G_c = \frac{A\Delta x}{2\tau_n}
\]

\[
g_{md} = A\mu_n \frac{V_{eq,1} + V_{eq,2}}{2}
\]


AC modeling extension

- **Capacitive effects** can be automatically tracked by the distributed substrate network approach.
- **Junction capacitance** is similar to the one of SPICE model and **diffusion capacitance** is dependent on minority carriers.

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Model parameters

### DC Model Parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>NTUB doping</td>
<td>8.5x10^{18} cm^{-3}</td>
</tr>
<tr>
<td>PTUB doping</td>
<td>6.1x10^{16} cm^{-3}</td>
</tr>
<tr>
<td>PSUB doping</td>
<td>9.0x10^{14} cm^{-3}</td>
</tr>
<tr>
<td>$\tau_p$ hole lifetime</td>
<td>2.0 µs</td>
</tr>
<tr>
<td>$\tau_n$ elec. lifetime</td>
<td>5.0 µs</td>
</tr>
<tr>
<td>$\tau_{rec}$ rec. lifetime</td>
<td>3.5 µs</td>
</tr>
<tr>
<td>N junction depth</td>
<td>5 µm</td>
</tr>
</tbody>
</table>

### AC Model Parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC coefficient</td>
<td>1 µm</td>
</tr>
<tr>
<td>Grading coefficient m</td>
<td>0.5</td>
</tr>
<tr>
<td>Built-in potential</td>
<td>0.67</td>
</tr>
</tbody>
</table>
DC Parasitic BJT

Temperature dependencies are included as well in the model.

AC selected examples

**Diode** capacitance (and inductance) can be efficiently simulated.

**BJT** cut-off frequency and frequency degradation of beta can be simulated.

*Spice simulation time 9 min – TCAD simulation time 10 hours*
Transient simulations

- Transient study of coupling phenomena is different in low and high injection regime

Spice netlist (128 nodes) 10ms – TCAD 15s per time step
EPFL Model usage

1. Meshing

2. Equivalent Circuit

3. Simulation

Spice netlist (10000 nodes) < 2 min

High Voltage Design flow

- Design
  - Spice Simulation

- Layout Automation
  - Modify Layout to meet design targets

- Extract circuit parasitic from layout
  - Post-layout Simulation

- Modify Schematics to meet design targets

Add active protection to:
- suppress parasitic thyristor
- prevent Latch-up
Thank you!

Q&A

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