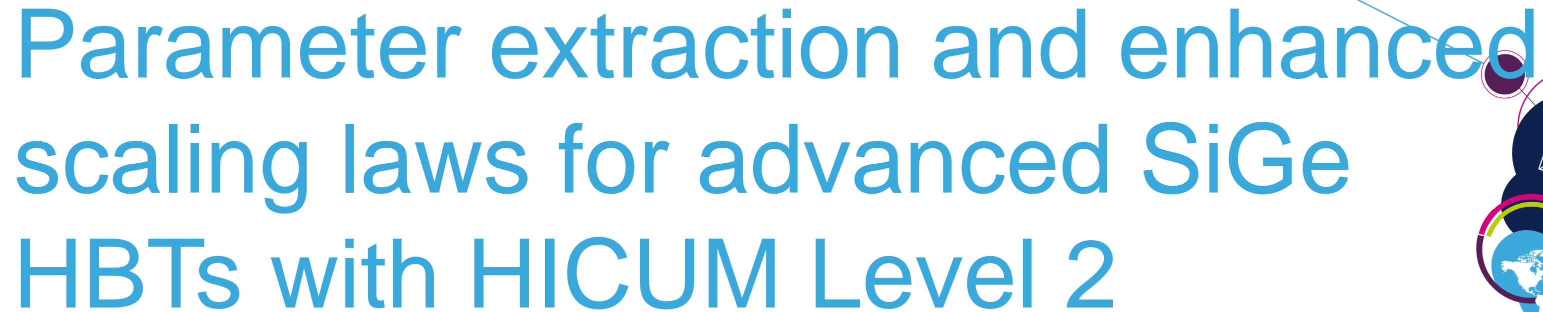


Parameter extraction and enhanced scaling laws for advanced SiGe HBTs with HICUM Level 2

T. Rosenbaum[1,2,3], D. Céli[1], M. Schröter[2], C. Maneux[3]

Modeling **of** **S**ystems **AK**
Grenoble, France, March 12, 2015

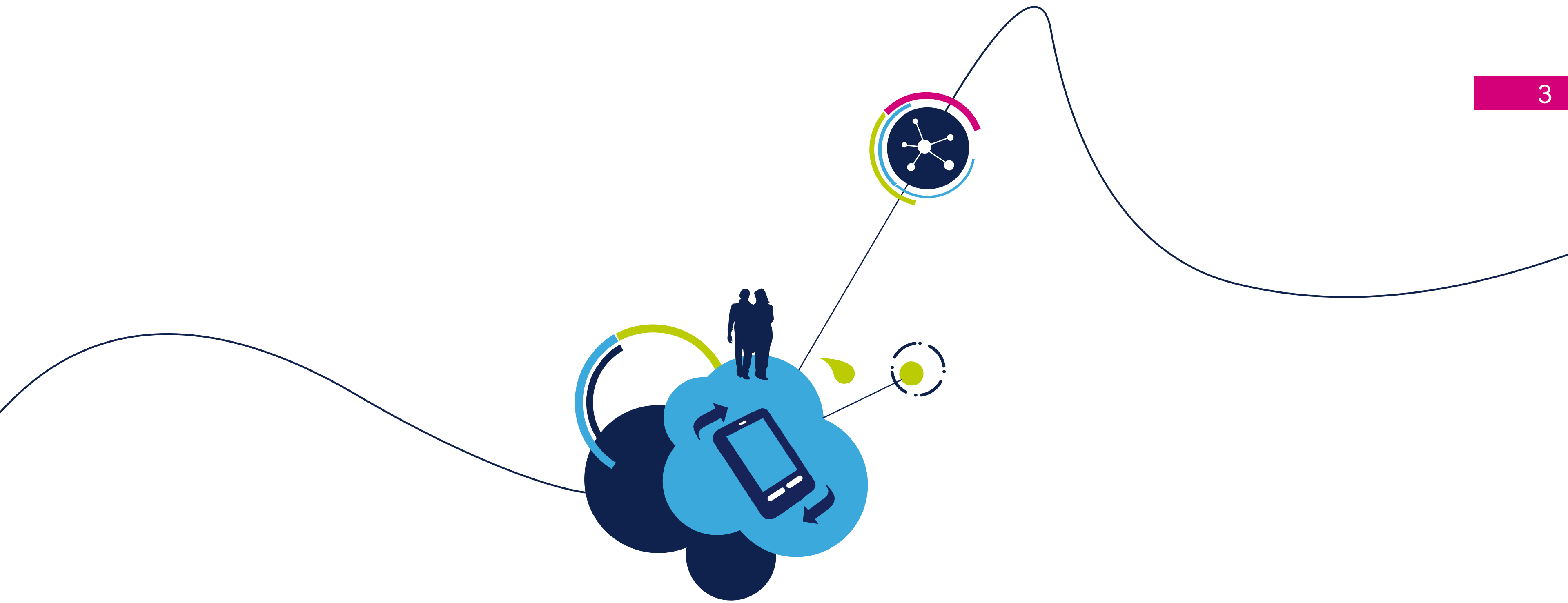
[1]STMicroelectronics, 38920 Crolles, France
[2]CEDIC, Technische Universität Dresden, 01062 Dresden, Germany
[3]IMS, Université Bordeaux I, 33405 Talence, France

life.augmented

Outline

- Introduction & Motivation
- HICUM L2 overview
- Geometry scaling for HBTs
  - Standard scaling approach (P/A)
  - Transfer current scaling – γ_C approach
  - Modeling the bias dependence of γ_C
- Example extraction for advanced SiGe HBTs
  - Generic scaling method
  - Transit time scaling
  - Scaling of the internal collector resistance
- Results and Conclusion

life.augmented



Introduction

Introduction & motivation

- Circuit design
  - Relies on accurately modeled characteristics
    - **DC behavior** (I/V curves, e.g. collector & base current for a HBT)
      - Affected by self-heating, external resistances
    - **AC behavior** (small signal parameters vs. frequency)
      - Affected by self-heating, external resistances & capacitances
      non quasi-static effects
  - Various kinds of circuits
    - Focus on certain transistor characteristics
      - e.g. mixers, power amplifiers at VHF require accurate S-parameter modeling

    ⇒ Modeling engineer needs to account for all eventualities
- Process engineering
  - Focuses on achieving performance targets
    - Targets are hard to achieve

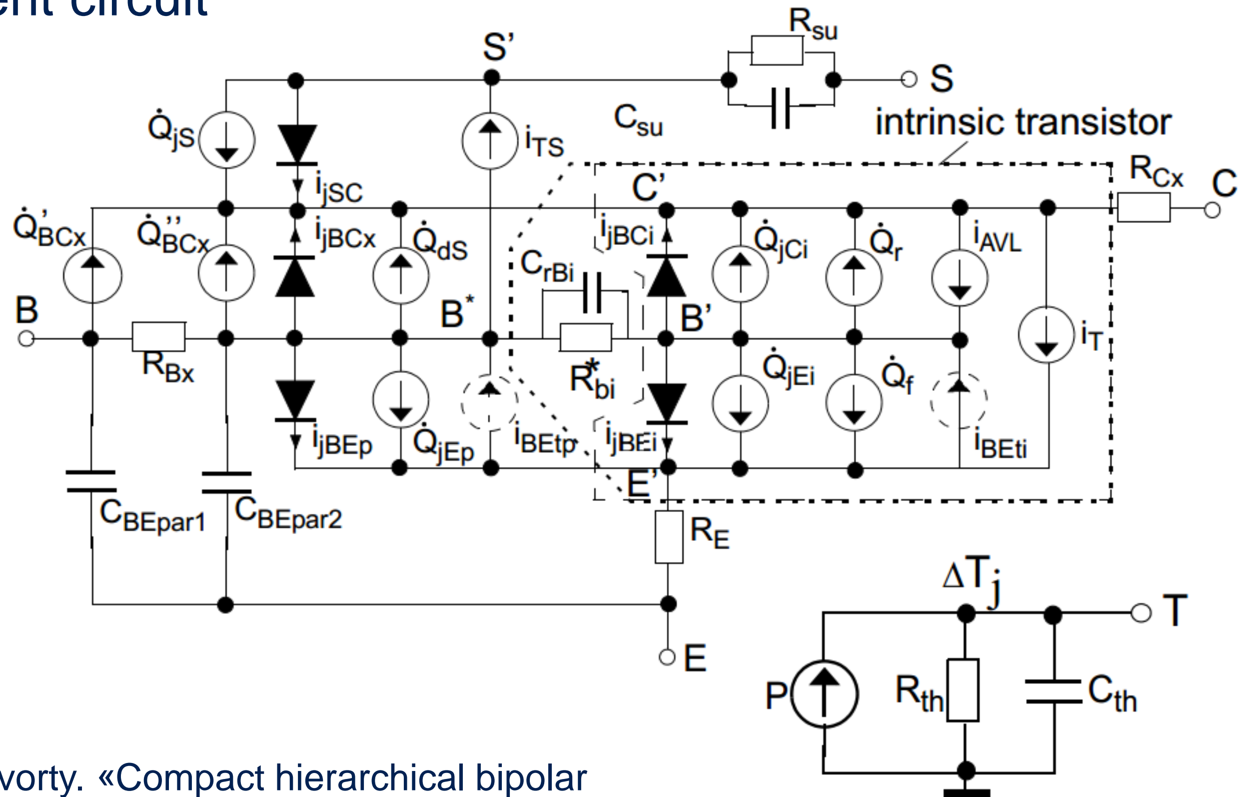
    ⇒ Recent architectures are getting more complex

    ⇒ Modeling complexity increases

life.augmented

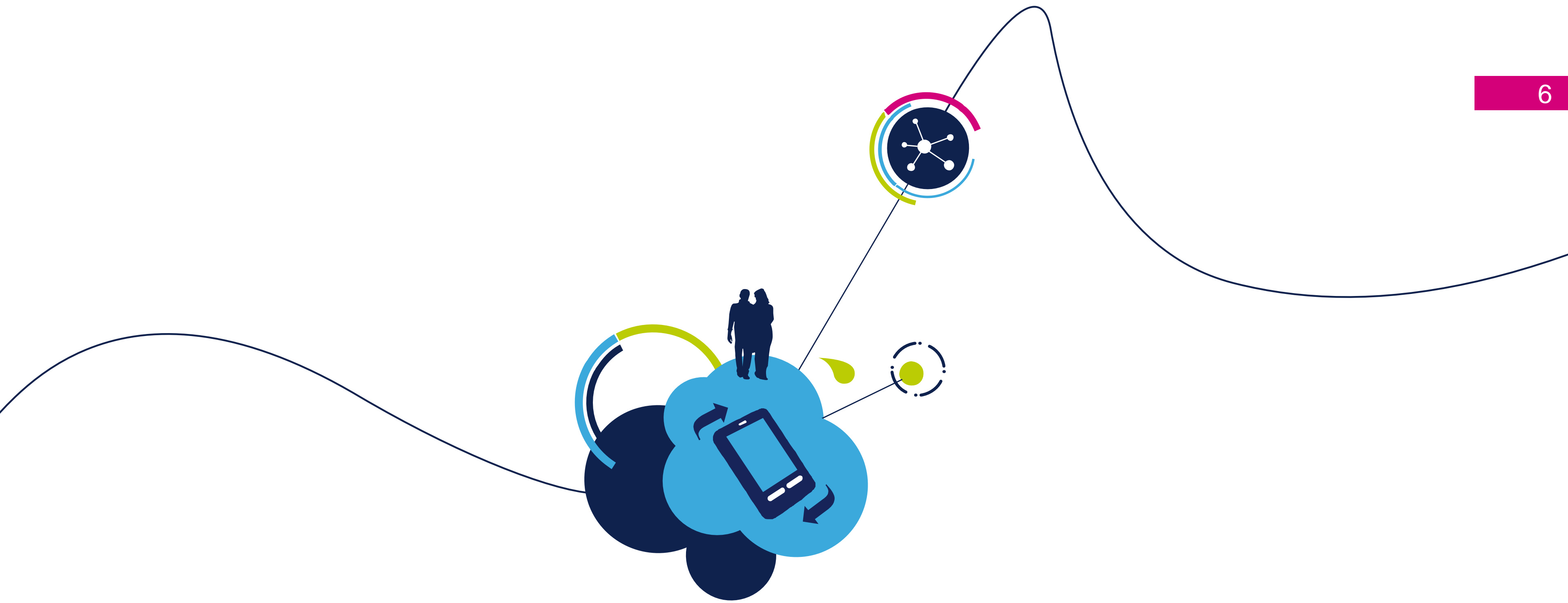
HICUM L2 2.33 overview [1]

- Physics based compact model for BJTs/HBTs
  - Targets high frequency applications and high currents
  - Has been applied successfully to silicon- and III/V material-based HBTs
  - Standard model available for most commercial simulators
- Large signal equivalent circuit
  - Internal transistor
    - Depletion charges
      Transfer current
      Int. base current
      Int. base resistance
      Transit-time charge
      Avalanche
  - External elements
    - Ext. resistances
      Ext. base current
      Ext. capacitances
      Substrate network
      Substrate transistor
  - Thermal network



[1] M. Schroter, A Chakravorty. «Compact hierarchical bipolar transistor modeling with HICUM». World Scientific, 2010.

life.augmented



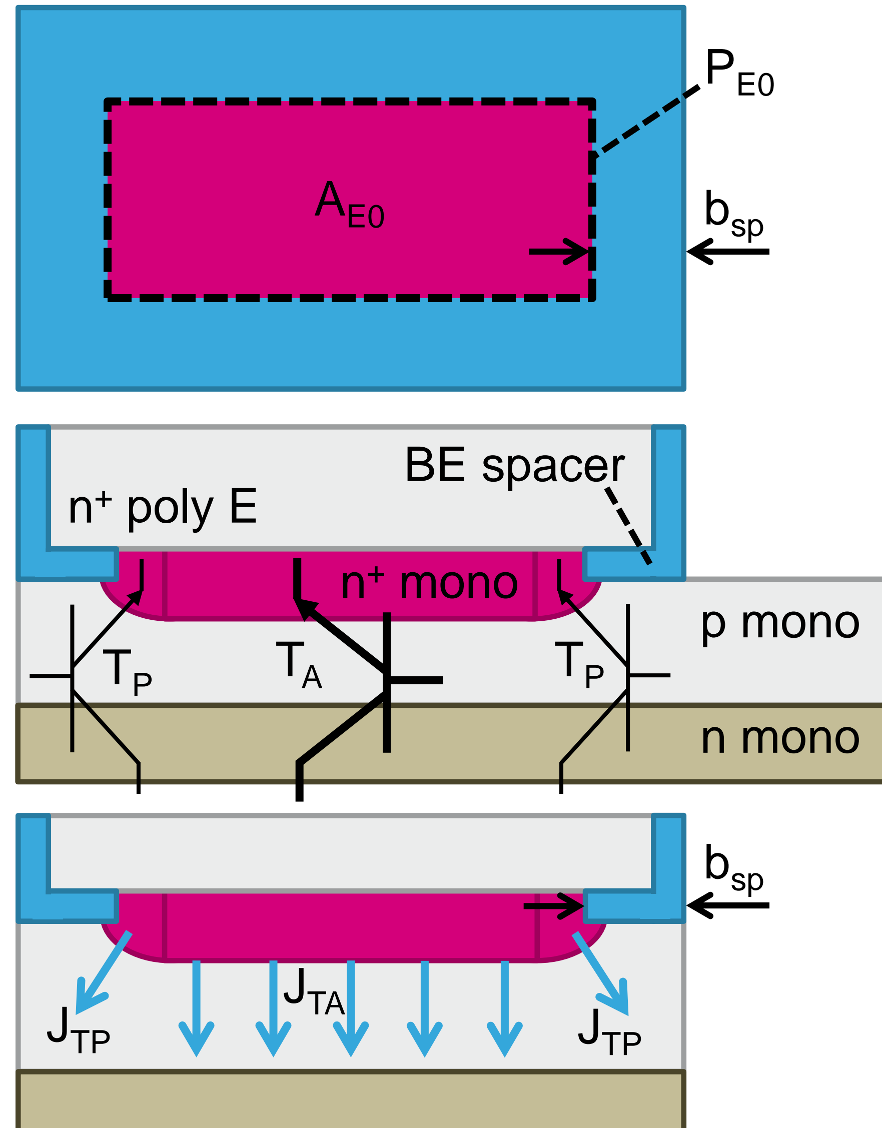
Geometry scaling for HBTs

Geometry scaling for HBTs

- Circuit design
  - Requires different transistor sizes for different types of applications

  ⇒ Necessary to perform geometry scaling
- Geometry conventions – top view
  - Blue area
    - Corresponds to drawn emitter area
  - Red area
    - Emitter area enclosed by BE-spacer
- Cross-section of typical HBT
  - Consists of two transistors
    - Transistor associated with area (A_{E0})
    - Transistor associated with perimeter (P_{E0})
  - Total transfer current

$$I_{T,tot} = J_{TA} A_{E0} + J_{TP} P_{E0}$$



life.augmented

Standard scaling approach (P/A)

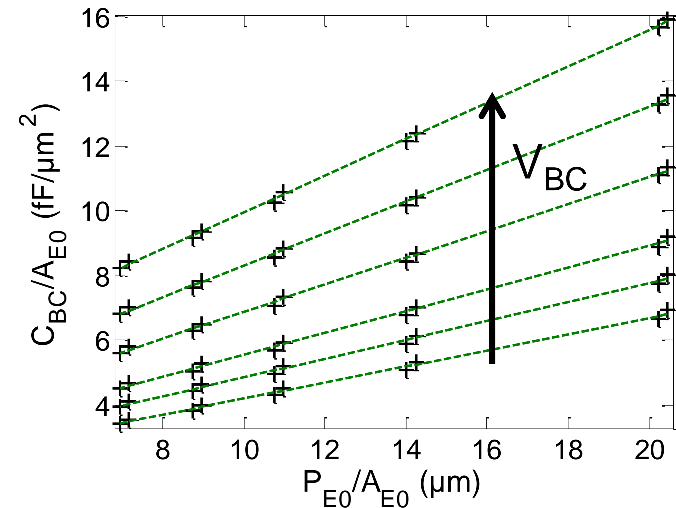
- Example for base collector capacitance
  - Measure capacitance for various transistor widths and lengths

$$C_{BC,meas} = C_{jCi} A_{E0} + C_{jCx} P_{E0}$$

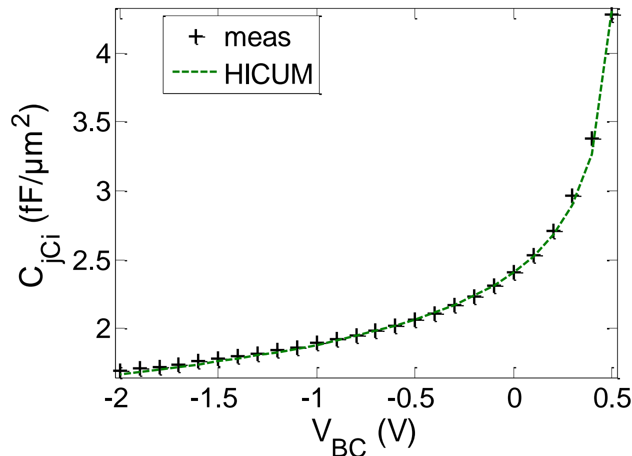
  - Normalize on area

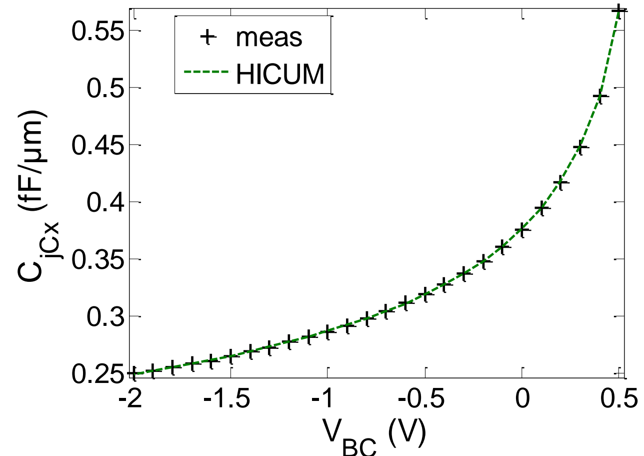
$$C_{BC,meas}/A_{E0} = C_{jCi} + C_{jCx} P_{E0}/A_{E0}$$

$\Rightarrow$ Offset corresponds to area component
Slope corresponds to perimeter



- Result (measurement data B55 [2])





[2] P. Chevalier et al. « A 55 nm Triple Gate Oxide 9 Metal Layers SiGe BiCMOS Technology Featuring 320 GHz fT / 370 GHz fMAX HBT and High-Q Millimeter-Wave Passives ». Proc. IEEE IEDM, 2014.

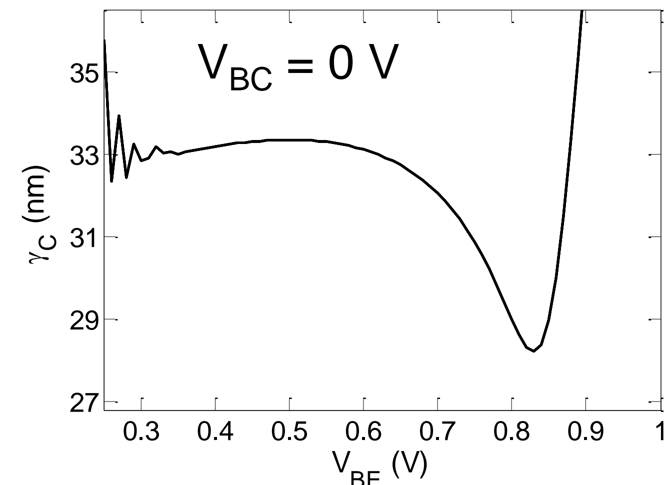
life.augmented

Transfer current scaling - γ_C

- HICUM model description
  - Consists of various elements for perimeter and area
    - Capacitances, base current
  - Does not feature peripheral transfer current due to various reasons
    - Was not necessary up to now, as γ_C approach worked reasonably well (P & A components behaved similarily)
    - Would increase simulation runtime and extraction effort
- The γ_C approach – example on TCAD data
  - Associate perimeter contribution to effective area

$$I_{T,tot} = J_{TA}A_{E0} + J_{TP}P_{E0}$$
$$I_{T,tot} = J_{TA}(A_{E0} + J_{TP}/J_{TA}P_{E0})$$
$$A_{E,eff} = A_{E0} + \gamma_C P_{E0}$$
$$\gamma_C = J_{TP}/J_{TA}$$

  - Perform standard P/A scaling and calculate γ_C



- Usual characteristics of γ_C
  - Bias independent up to medium current range
    - For high injection, self-heating and external resistances vary for different transistor sizes => will cover variable γ_C

$\Rightarrow$ γ_C approach is valid if observed function is constant for low current range

life.augmented

γ_C approach - consistency with capacitances

- Simplified transfer current description
  - Weight factor h_{jEi} describes low current behavior

$$I_{T,tot} = \frac{c_{10} exp(V_{BEi}/V_T)}{Q_{p0} + h_{jEi} Q_{jEi}}$$

- Scaling of transfer current vs. capacitances
  - Transfer current is scaled with effective emitter area

$$I_{T,tot} = J_{TA} A_{E,eff} \quad \Rightarrow \quad c_{10} = c_{10A} {A_{E,eff}}^2 \qquad Q_{p0} = Q_{p0A} A_{E,eff}$$

  - Capacitances are scaled with actual emitter dimensions (must match AC characteristics)

$$Q_{jEi} = Q_{jEiA} A_{E0}$$

⇒ Will lead to discrepancy for transfer current

- Solution
  - Adjust weight factor h_{jEi} to fulfill scaling of $I_{T,tot}$

$$h_{jEi} = h_{jEiA} \frac{A_{E,eff}}{A_{E0}}$$

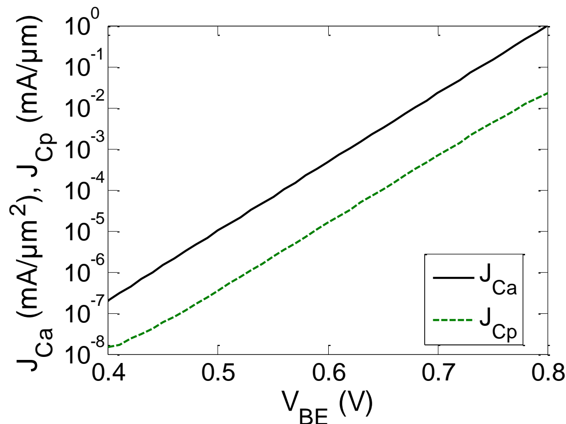
$$I_{T,tot} = \frac{c_{10A} {A_{E,eff}}^2 exp(V_{BEi}/V_T)}{Q_{p0A} A_{E,eff} + h_{jEiA} \frac{A_{E,eff}}{A_{E0}} Q_{jEiA} A_{E0}} = A_{E,eff} \frac{c_{10A} exp(V_{BEi}/V_T)}{Q_{p0A} + h_{jEiA} Q_{jEiA}} = J_{TA} A_{E,eff}$$

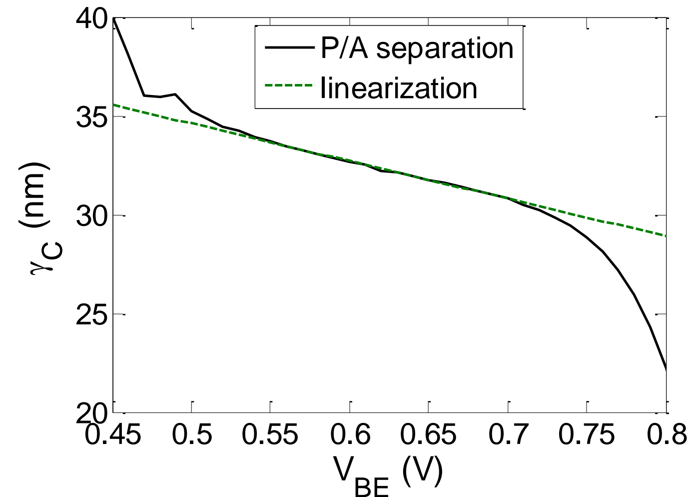
ST life.augmented

I_T for recent technologies

- γ_C approach for measurement data (B55)
  - Exhibits linear bias dependence

  => Standard γ_C approach not applicable





- Possible solution
  - Similar behavior observed for process of IHP [3]
    - Method tries to merge different bias dependence of J_{TA} & J_{TP} by adjusting weight factor h_{jEi}
  - Several prerequisites
    - Similar voltage dependence of Q_{jEp} & Q_{jEi}
    - Similar voltage dependence of h_{jEi} & h_{jEp}
    - Several simplifications in equations

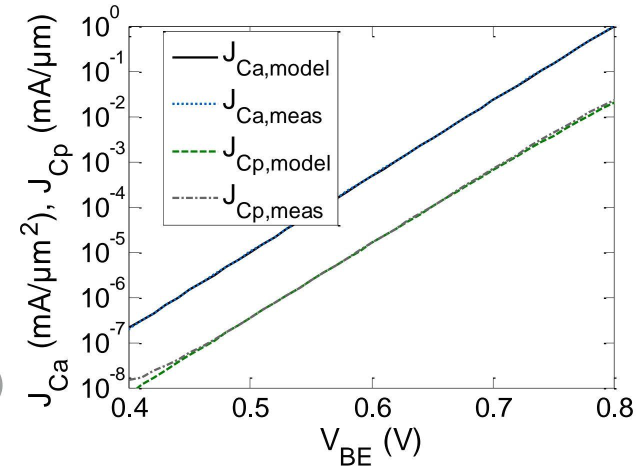
$$I_{T,tot} = \frac{c_{10} exp(V_{BEi}/V_T)}{Q_{p0} + h_{jEi} Q_{jEi}}$$

[3] A. Pawlak et al. « Geometry scalable model parameter extraction for mm-wave SiGe-heterojunction transistors ». Proc. IEEE BCTM, 2013.

life.augmented

Bias dependent γ_C [3]

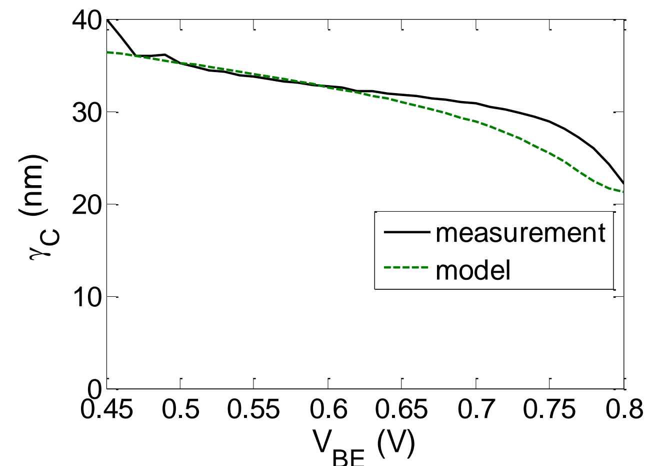
- Methodology
  - Perform standard P/A separation to obtain area and parameter components
  - Run extraction for area component
  - Run extraction for perimeter component
    - Fix $Q_{jEp} = Q_{jEi}$ & fix $a_{hjEi} = a_{hjEp}$ (identical voltage dependence of h_{jEi} and h_{jEp} and charge)



- Scaling
  - Effective h_{jEi}
    - Courtesy of Didier Céli
    - Identical result to [3], but HICUM L2 description

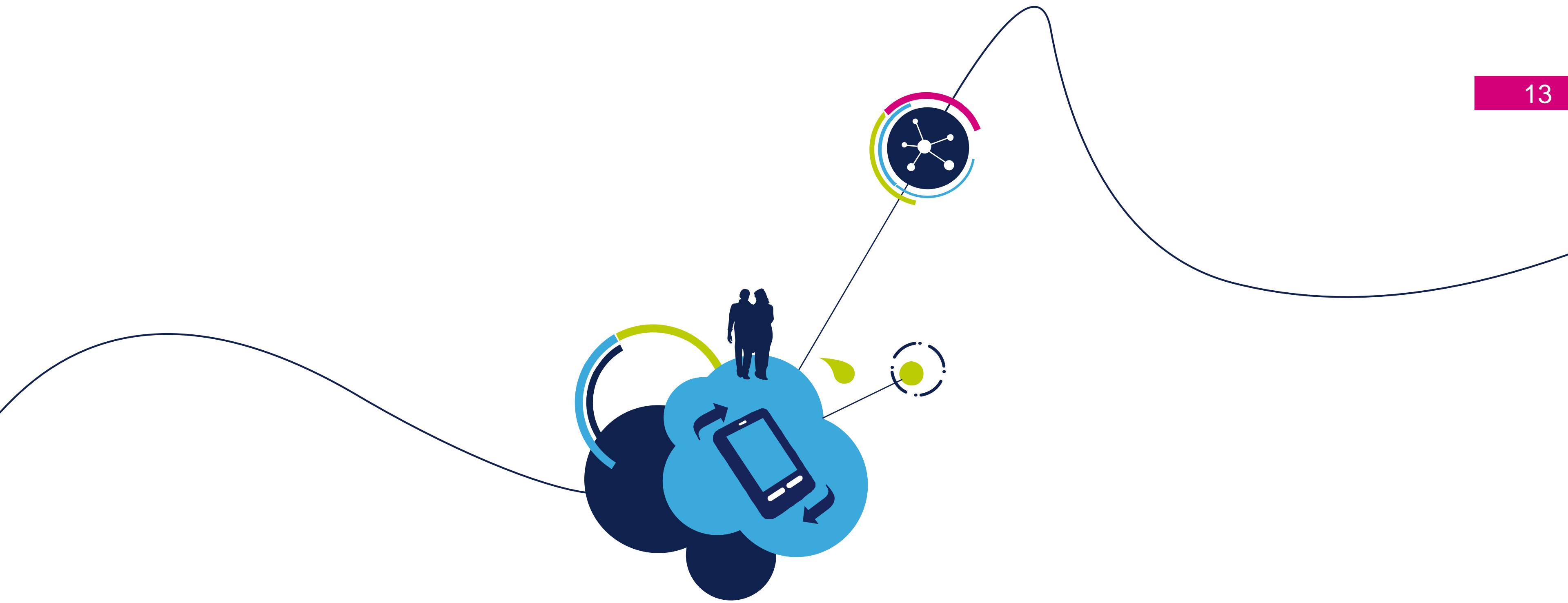
$$h_{jEi,eff} = h_{jEi} \frac{1 + \gamma_{C0} \frac{h_{jEp}}{h_{jEiA}} \frac{P_{E0}}{A_{E0}}}{1 + \gamma_{C0} \frac{P_{E0}}{A_{E0}}}$$

- Verification
  - Run simulations for all transistors considered in extraction
  - Perform P/A separation on synthetic data
  - Compare γ_C



$\Rightarrow$ Reasonable deviation, valid for low currents

life.augmented



Example extraction for B55

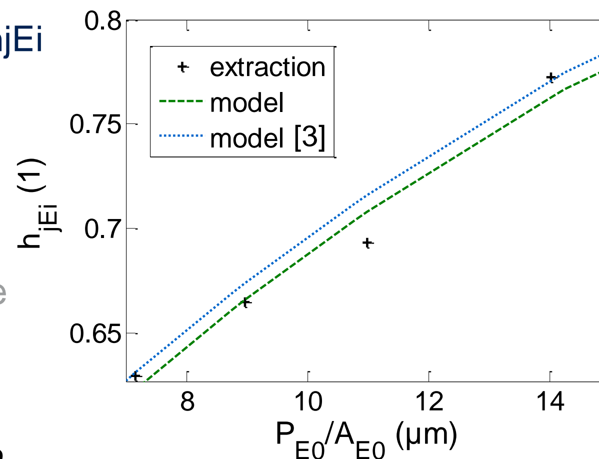
(focusing on selected characteristics)

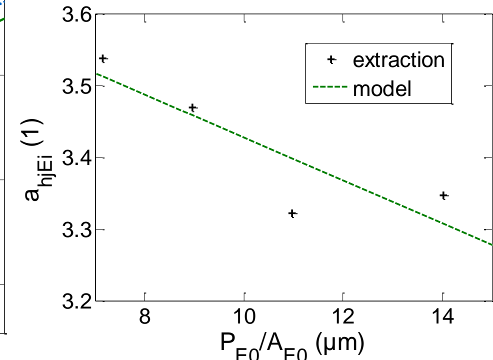
A generic scaling approach

- Methodology
  - Run single transistor extraction for available geometries
  - Check geometry dependence of extracted parameters
- Bias dependent h_{jEi} and a_{hjEi}
  - Weight factor h_{jEi}
    - Dotted line (blue): approach of [3]
    - Dashed line (green): model of [3] applied to single transistor extraction data
  - Assume linear dependence for a_{hjEi}

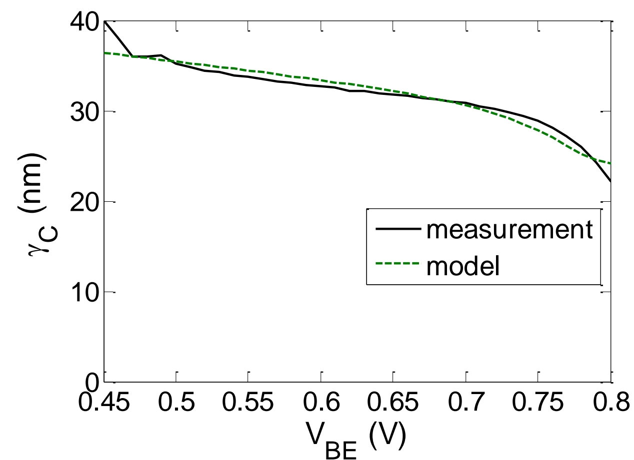
$$a_{hjEi} = a_{hjEi0} + a_{slope} \frac{P_{E0}}{A_{E0}}$$

    - For $P_{E0}/A_{E0} = 0$ the area value is obtained





- Verification
  - Run simulations for all transistors considered in extraction
  - Perform P/A separation on synthetic data
  - Compare γ_C

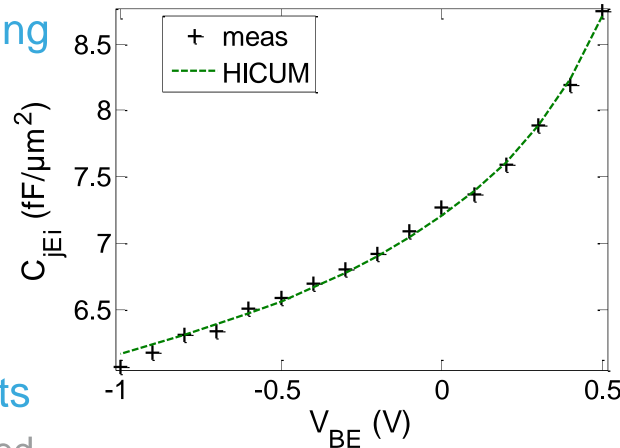


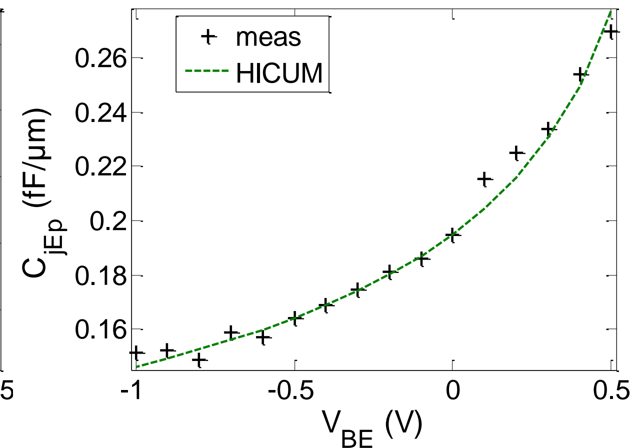
life.augmented

Base emitter capacitance

- Perform standard P/A scaling
  - Capacitance partitioning

$$C_{BE,meas} = C_{jEi}A_{E0} + C_{jEp}P_{E0} + C_{BEpar}P_{E0}$$

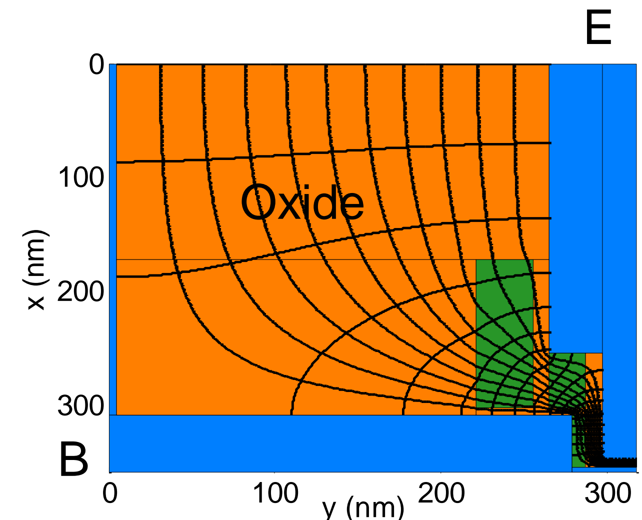




  - Peripheral components
    - Need to be distributed between junction- and spacer capacitance (bias independent)
    - Portions cannot be distinguished from geometry variation

$\Rightarrow$ Perform EM simulation

- Field distribution of BE-spacer
  - Geometry information can be obtained from SEM/TEM pictures
    - Structure consists of Oxide, Nitride and (assumed) ideal contacts for Poly region
  - C_{BEpar} = 0.35 fF/µm



[4] G. Wedel. « POICAPS - A multidimensional numerical capacitance simulator ». CEDIC internal document, 2012.

life.augmented

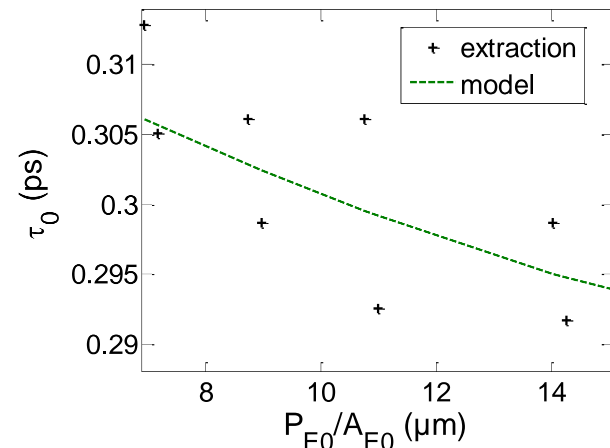
Transit time scaling

- Scaling equation for low current transit time [6]
  - Similar to description of h_{jEi}
  - Performs weighting between internal and peripheral transit time

$$\tau_0 = \tau_{0a} \frac{1 + f_{tpi}\gamma_C \frac{P_{E0}}{A_{E0}}}{1 + \gamma_{C0} \frac{P_{E0}}{A_{E0}}} \qquad f_{tpi} = \frac{\tau_{0p}}{\tau_{0a}}$$

- Various extraction methodologies
  - Usually involve circuit simulation of different transistor sizes
    - Manual fine tuning of parameters
    - Global optimization on selected parameters
  - Alternative
    - Use method of [5] for performing single transitor extraction and use obtained parameter values for scaling
- Result using method of [5]
  - τ_{0a} and f_{tpi} are very sensitive to extracted values of τ_0
  - Variability of τ_0 is very low (~7.5%)

  => Extraction method must be accurate

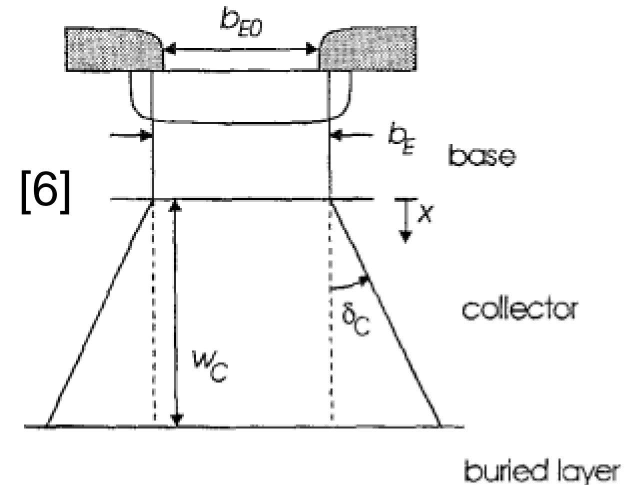


[5] T. Rosenbaum et al. « Automated transit time and transfer current extraction for single transistor geometries ». Proc. IEEE BCTM, 2013.

life.augmented

Internal collector resistance

- Modeling approach [6]
  - r_{Ci0} mainly depends on emitter area
  - Current spreading
    - Is taken into account by current spreading factor



- Basic idea behind current spreading model
  - Linear increase of current path envelope

$$A_C(x) = A_{E,eff}\left(1 + 2\tan(\delta_C)\frac{x}{b_E}\right)$$

  - Integration over $1/A_C(x)$ leads to logarithm

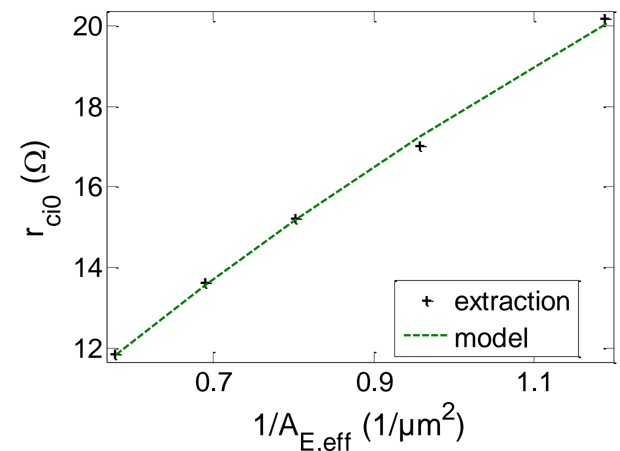
$$r_{Ci0} = \frac{r_{Ci0a}}{f_{cs}A_E}$$

$$f_{cs} = \frac{LAT_b - LAT_l}{ln[(1 + LAT_b)/(1 + LAT_l)]}$$

$$LAT_b = 2w_{Ci}\tan(\delta_C)/b_E$$

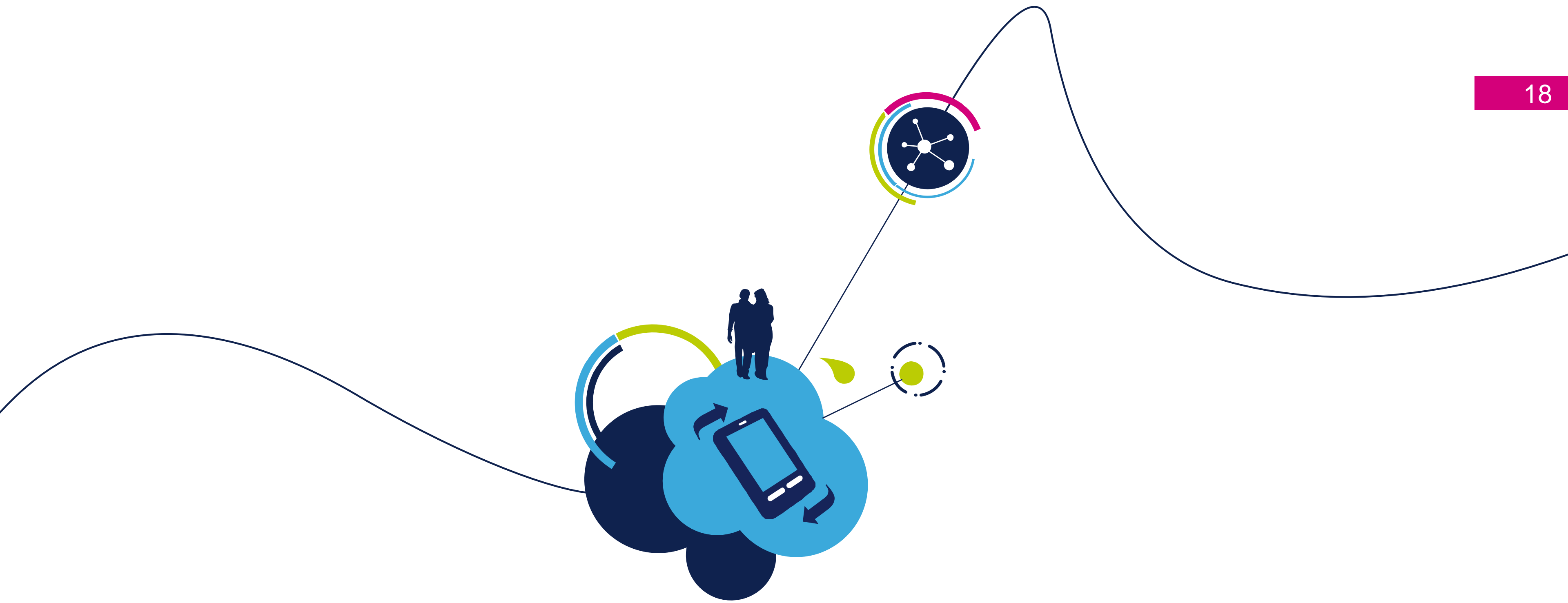
$$LAT_l = 2w_{Ci}\tan(\delta_C)/l_E$$

- Result
  - Perform optimization for r_{Ci0a} & δ_C



[6] M. Schroter et al. « Physical modeling of lateral scaling in bipolar transistors ». IEEE Journal of Solid-State Circuits, 1996.

life.augmented



Results using scalable model

(for selected transistors)

Assessing extraction quality

- Collector current
  - Allows to identify discrepancies at high current region
  - Will not help to evaluate extraction for low currents
- Normalized collector current
  - Is equal to 1 for low currents
  - Allows to assess bias dependent h_{jEi}

$$I_{C,norm} = \frac{I_C}{I_S exp(V_{BEi}/V_T)} = \frac{1}{1 + h_{jEi} Q_{jEi}/Q_{p0}}$$

- Normalized transconductance
  - Similar to $I_{C,norm}$
  - Useful to identify correct modeling of medium/high current fall-off

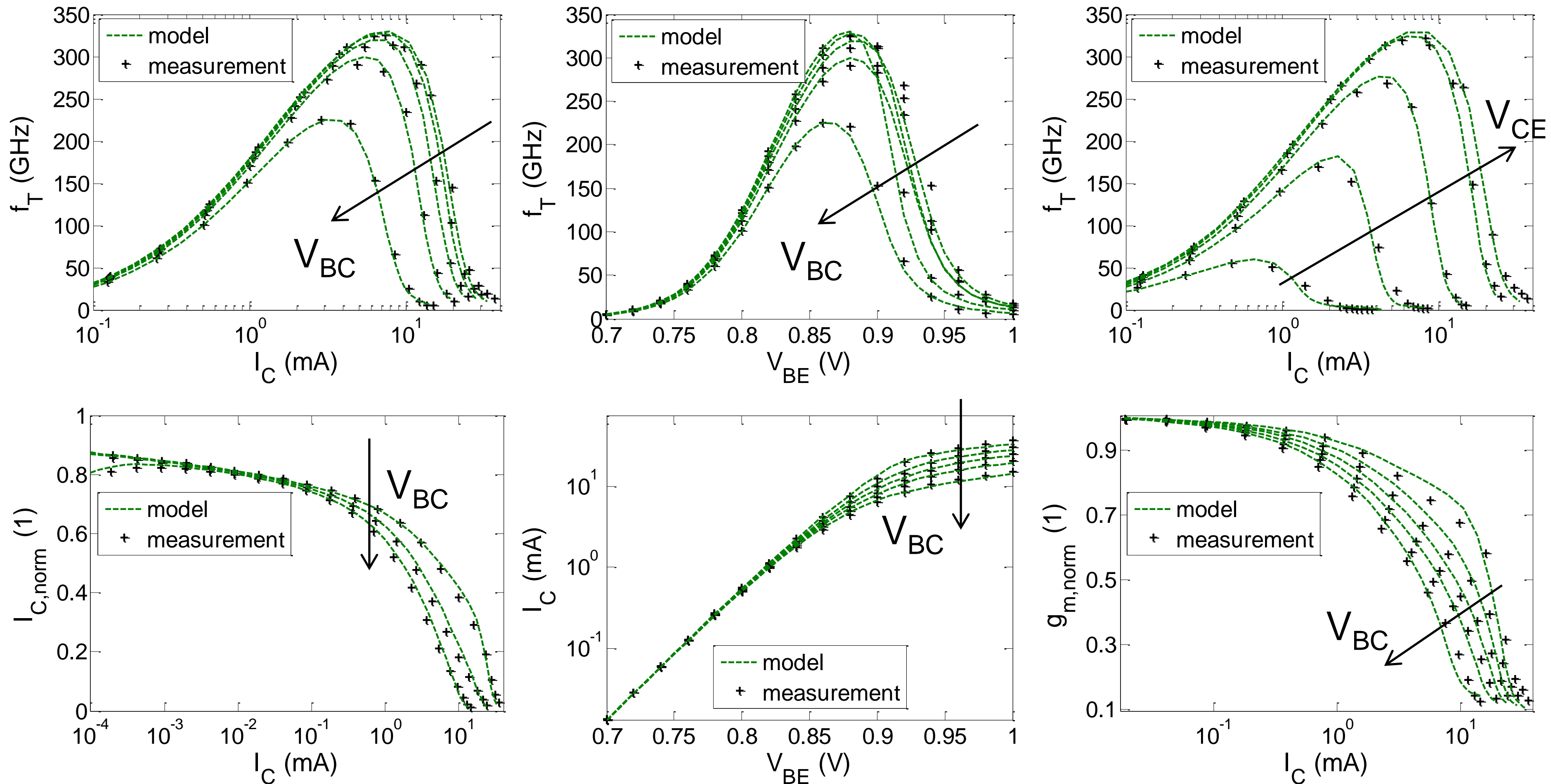
$$g_{m,norm} = \frac{g_m}{I_C} V_T$$

- Transit frequency
  - Allows to assess correct transit time modeling
  - Useful to include measurements at V_{CE} = const
    - Shows model reliability in saturation

life.augmented

Small high speed transistor

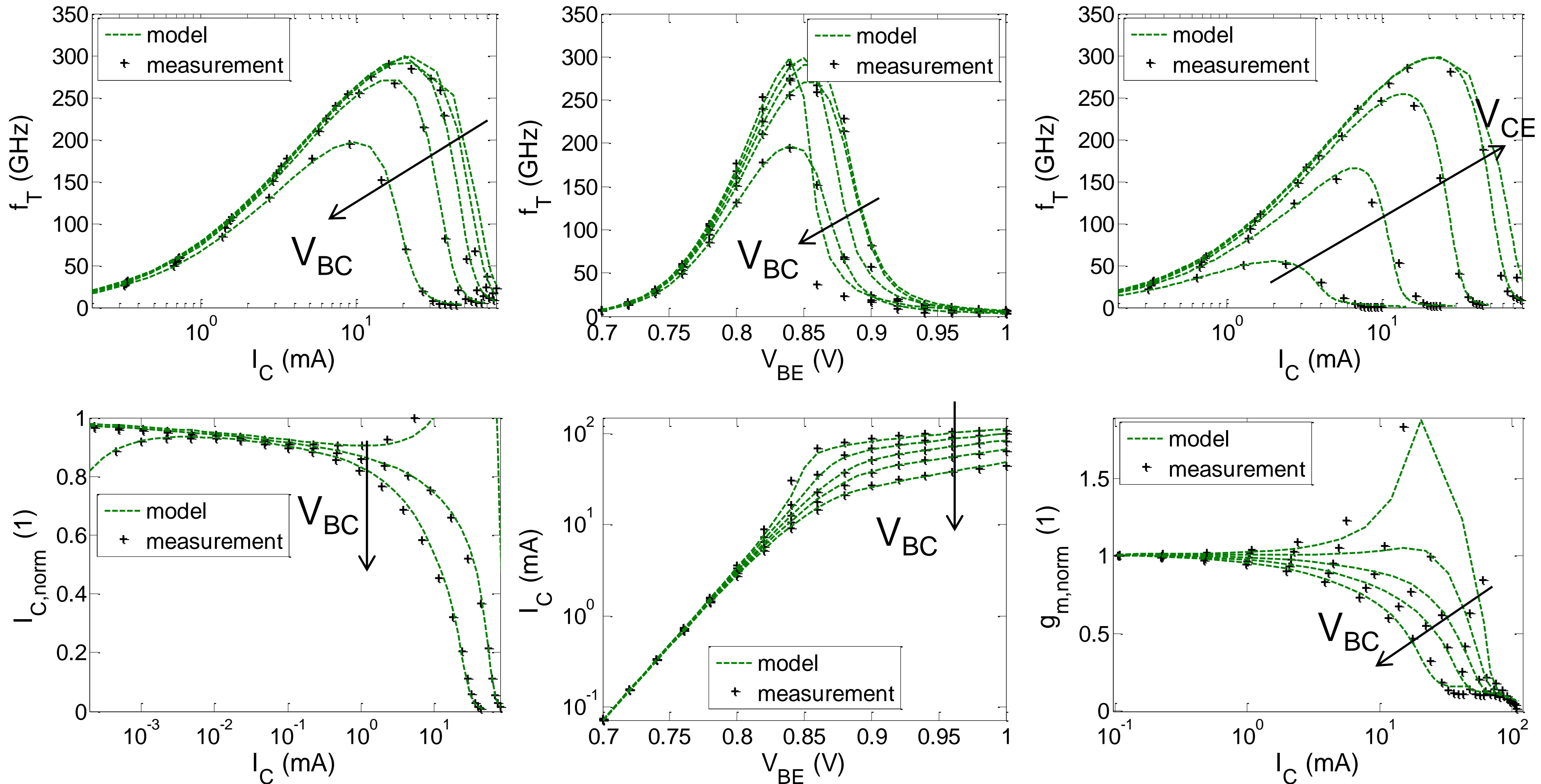
- b_{E0} = 100 nm, l_{E0} = 4.42 µm
  - V_{BC} = [-0.5 -0.25 0.0 0.25 0.5] V, V_{CE} = [0.1 0.25 0.5 1 1.5] V



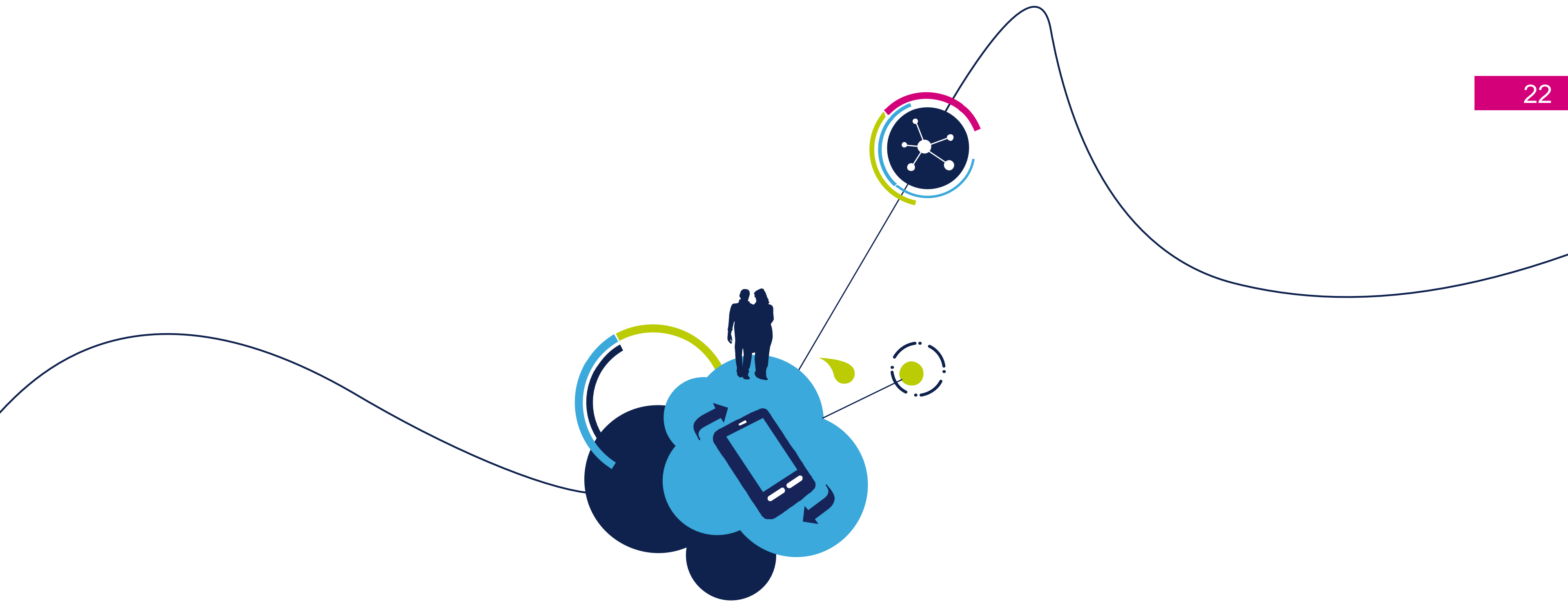
life.augmented

Large high speed transistor

- b_{E0} = 300 nm, l_{E0} = 8.92 µm
  - V_{BC} = [-0.5 -0.25 0.0 0.25 0.5] V, V_{CE} = [0.1 0.25 0.5 1 1.5] V



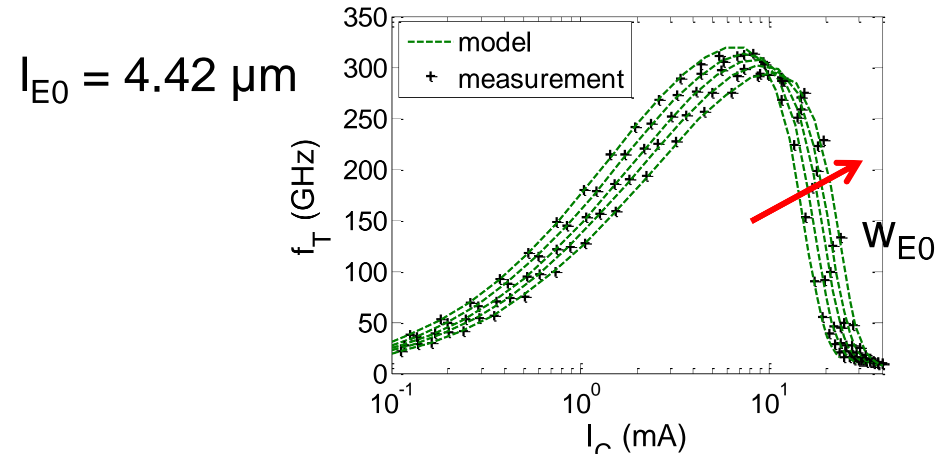
life.augmented

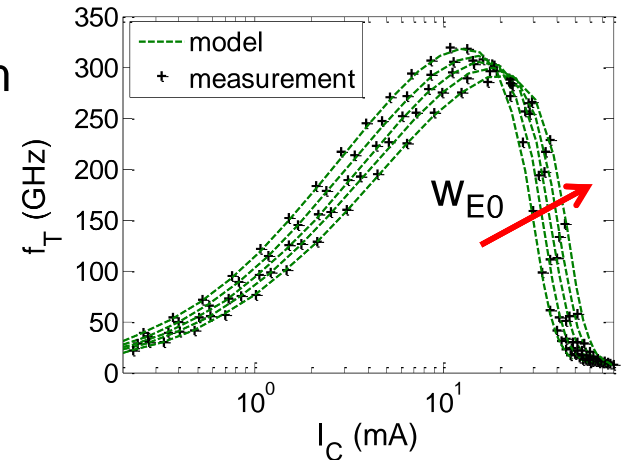


Results overview for V_{BC} = 0 V
(for all transistors)

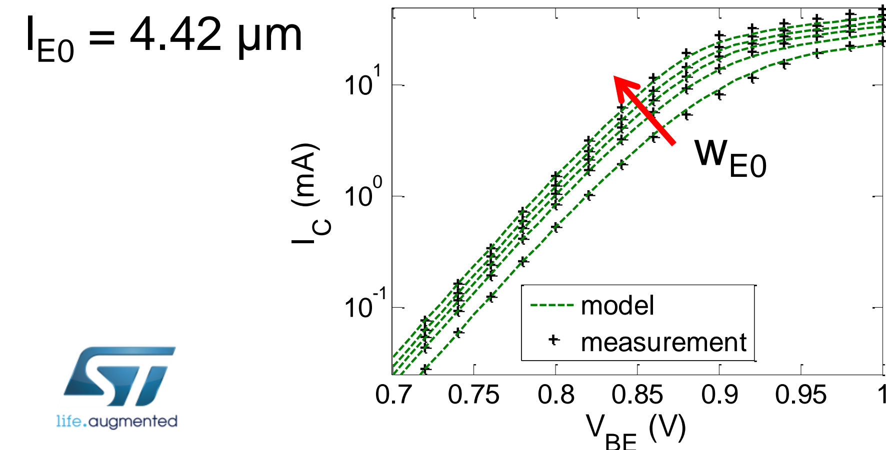
Selected quantities at V_{BC} = 0 V

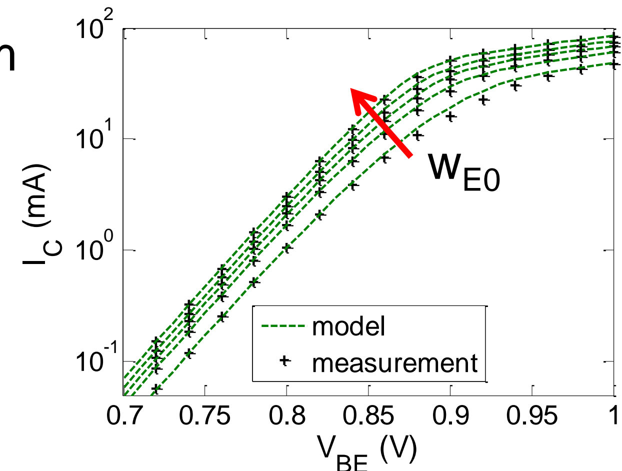
- Transit frequency (V_{BC} = 0 V)
  - w_{E0} = [100 145 190 235 300] nm





- Collector current (V_{BC} = 0 V)
  - w_{E0} = [100 145 190 235 300] nm



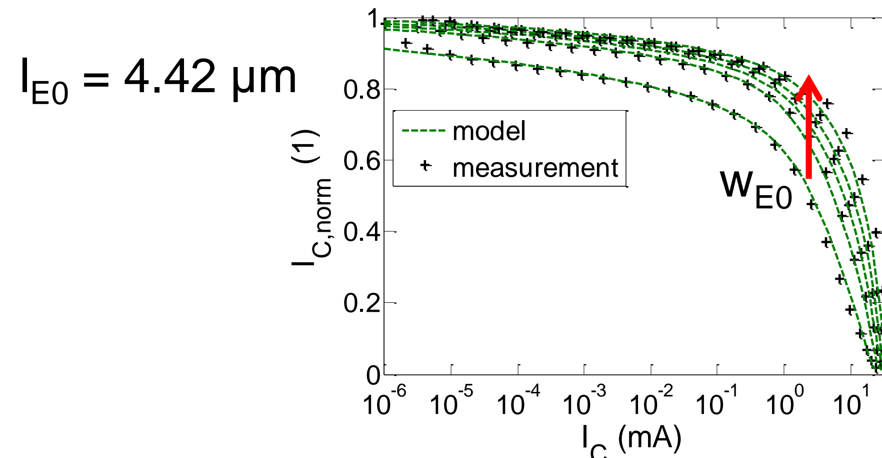


life.augmented

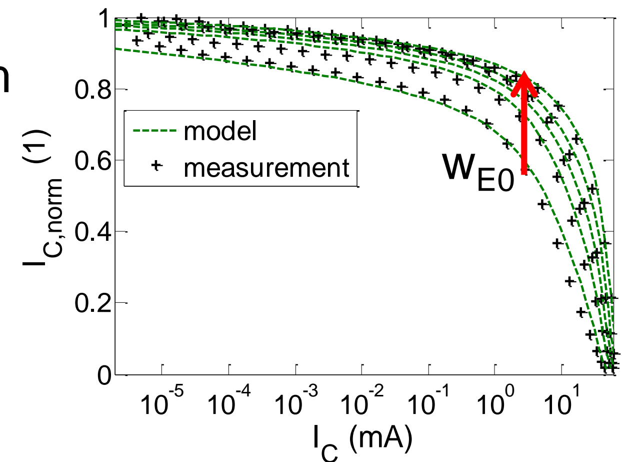
Selected quantities at $V_{BC} = 0$ V

- Normalized collector current ($V_{BC} = 0$ V)
  - w_{E0} = [100 145 190 235 300] nm

$l_{E0} = 4.42$ µm

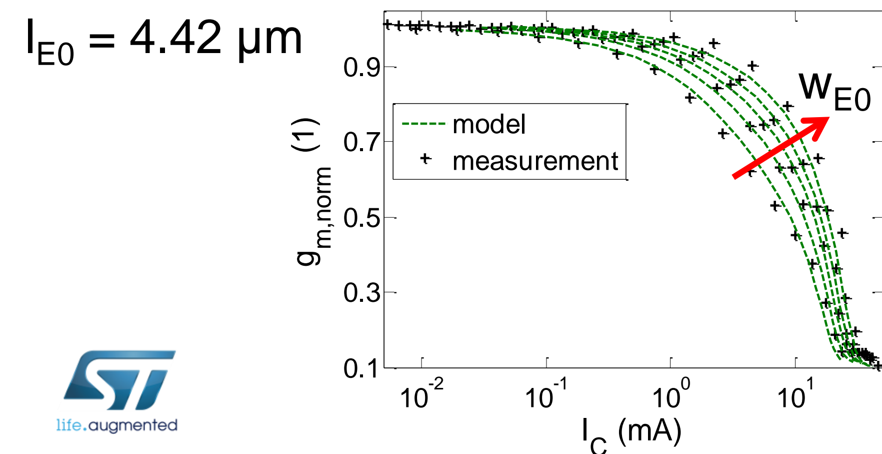


$l_{E0} = 8.92$ µm

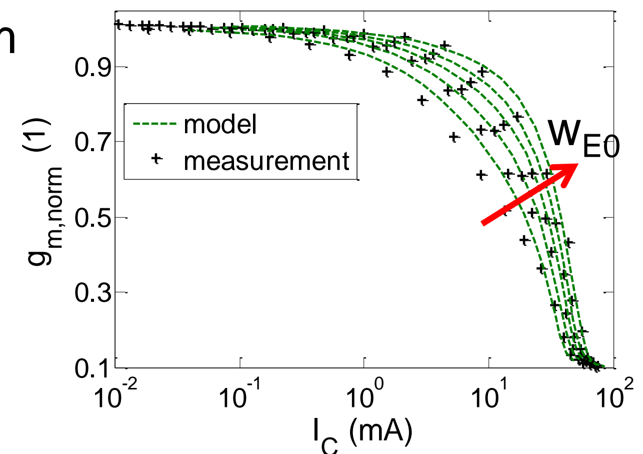


- Normalized transconductance ($V_{BC} = 0$ V)
  - w_{E0} = [100 145 190 235 300] nm

$l_{E0} = 4.42$ µm



$l_{E0} = 8.92$ µm



life.augmented

Conclusion

- Introduction on geometry scaling for HBTs
  - Standard scaling approach (P/A)
    - Remains sufficient for Capacitance modeling
  - Transfer current scaling – γ_C approach
    - Is not suitable anymore for advanced HBTs
    - Voltage dependence of area and perimeter differ too much
  - Enhanced transfer current scaling
    - Enables to model the bias dependence of $\gamma_C(V_{BE})$ by modulating the weight factor h_{jEi}
    - Result can be enhanced by adding a linear geometry dependence for a_{hjEi}
- Example extraction for an advanced SiGe technology [2]
  - Shows excellent agreement for both bias and geometry dependence
    - Bias dependent γ_C can be observed for normalized transfer current
    - Model features single geometry scalable modelcard for all transistors
  - Important conerstones for geometry dependence of f_T
    - Proper geometry modeling of the low current transit time and internal collector resistance

[2] P. Chevalier et al. « A 55 nm Triple Gate Oxide 9 Metal Layers SiGe BiCMOS Technology Featuring 320 GHz fT / 370 GHz fMAX HBT and High-Q Millimeter-Wave Passives ». Proc. IEEE IEDM, 2014.

life.augmented

Thank you for your attention!

References

[1] M. Schroter, A Chakravorty. «Compact hierarchical bipolar transistor modeling with HICUM». World Scientific, 2010.

[2] P. Chevalier et al. « A 55 nm Triple Gate Oxide 9 Metal Layers SiGe BiCMOS Technology Featuring 320 GHz fT / 370 GHz fMAX HBT and High-Q Millimeter-Wave Passives ». Proc. IEEE IEDM, 2014.

[3] A. Pawlak et al. « Geometry scalable model parameter extraction for mm-wave SiGe-heterojunction transistors ». Proc. IEEE BCTM, 2013.

[4] G. Wedel. « POICAPS - A multidimensional numerical capacitance simulator ». CEDIC internal document, 2012.

[5] T. Rosenbaum et al. « Automated transit time and transfer current extraction for single transistor geometries ». Proc. IEEE BCTM, 2013.

[6] M. Schroter et al. « Physical modeling of lateral scaling in bipolar transistors ». IEEE Journal of Solid-State Circuits, 1996.

Appendix

- Bias dependence of h_{jEi}

$$h_{jEi} = h_{jEi0}\frac{exp(u) - 1}{u}$$

$$u = a_{hjEi}\left(1 - \left[1 - \frac{v_j}{V_{DEi}}\right]^{z_{Ei}}\right)$$

  - V_j is the smoothed Base emitter voltage V_{BEi}
    - Range: $0 < V_j < V_{DEi}$