

# LDMOS MODELING USING THE DUAL GATE JFET MODEL JFETIDG

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EXTERNAL USE



SECURE CONNECTIONS  
FOR A SMARTER WORLD

# AGENDA

- ✔ Motivation
- JFETIDG model
- New LDMOS model
- Some Modeling Results
- Q&A

# Motivation

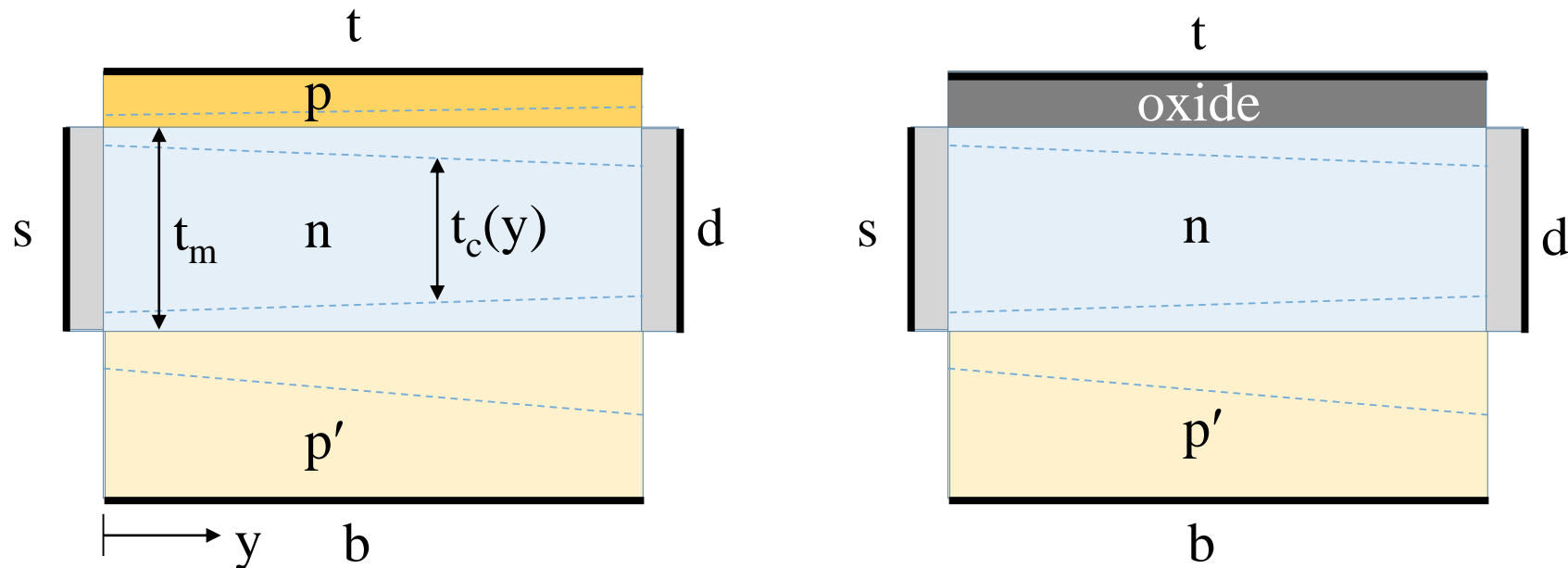
- SPHV is a very good LDMOS model. However, it is not public.
- We want to make a good LDMOS model for everyone.

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# Generalization of JFET Concept

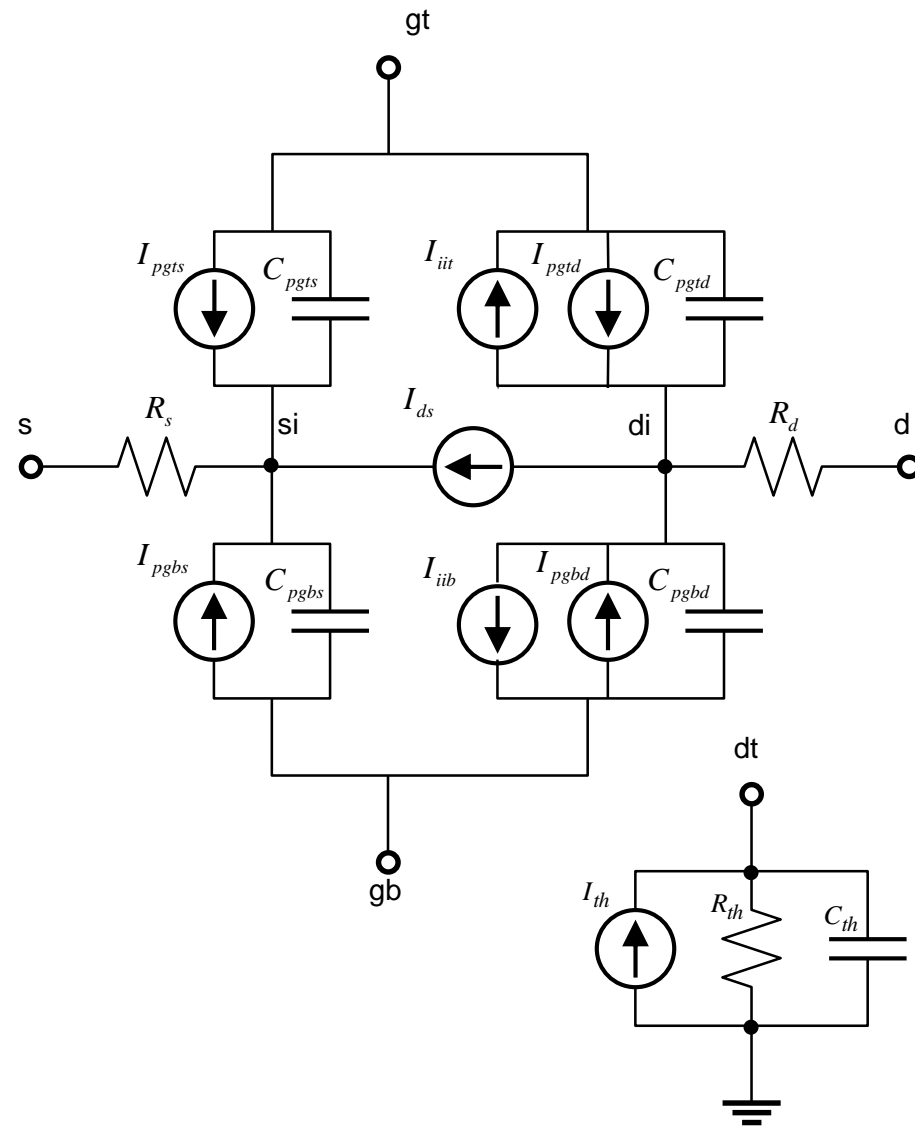
- Traditionally: Gate is pn-junction
- Generalized: Gate can be pn-junction or MOS
- Mathematically, both gate type can be described by
  - depletion factor ( $d_f$ )
  - built-in potential ( $\psi_r$ )



# Applications of Generalized Dual-gate JFET Model

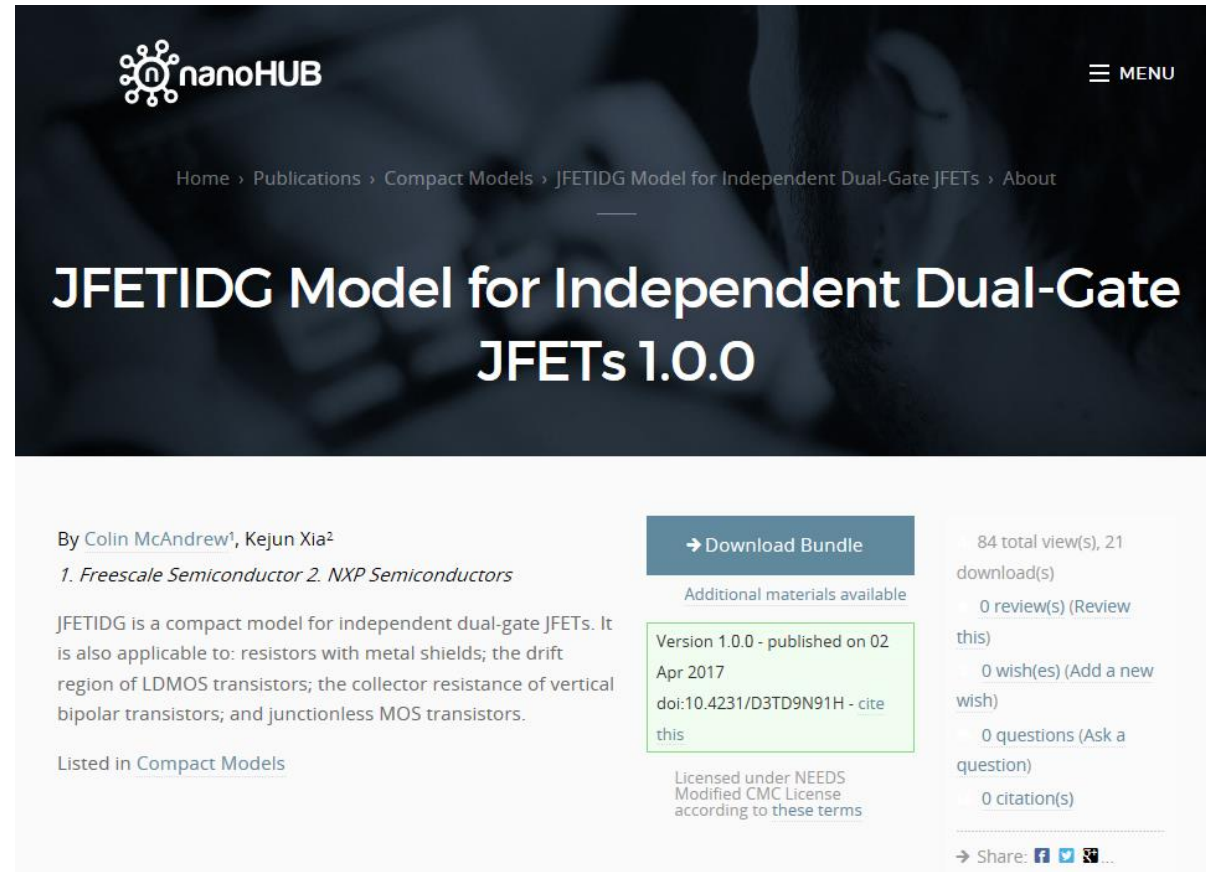
- Case I: 2 pn junction gates
  - Dual-gate JFET per si
  - Collector resistance of 4-terminal vertical bipolar transistors
- Case II: 1 pn junction + 1 MOS gates
  - Resistors (diffused or polysilicon) with metal shields
  - Drift region of LDMOS transistors with field plates (Next page)
- Case III: 2 MOS gates
  - Recently developed junctionless MOSFETs

# Equivalent Circuit of JFETIDG



# Release of the JFETIDG Model

- Ver 1.0.0 (Apr 2, 2017)
  - Public, through NEEDS license
  - Published on nanoHUB



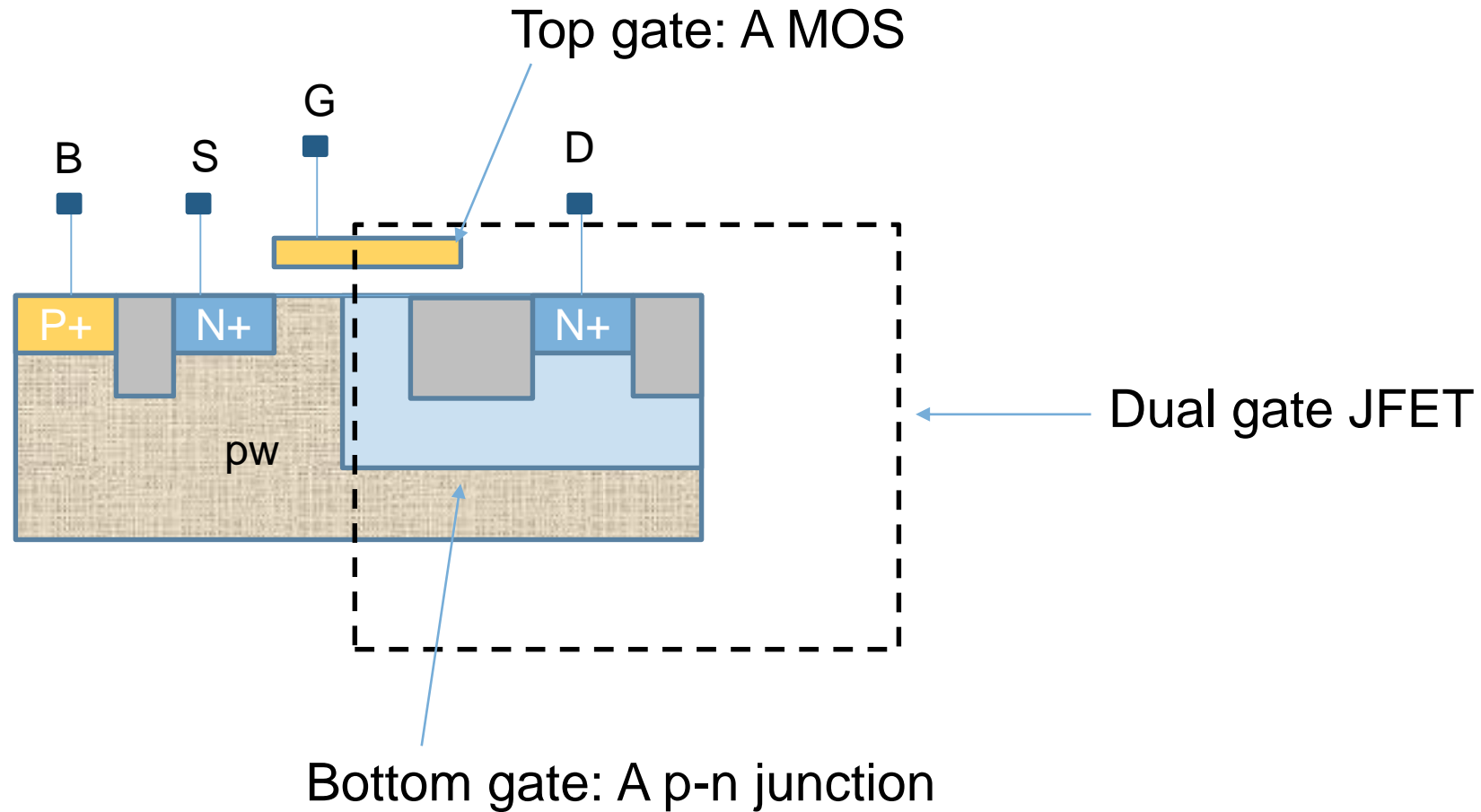
The screenshot shows the nanoHUB website interface for the JFETIDG Model. At the top left is the nanoHUB logo, and at the top right is a MENU icon. Below the logo is a breadcrumb trail: Home > Publications > Compact Models > JFETIDG Model for Independent Dual-Gate JFETs > About. The main title is "JFETIDG Model for Independent Dual-Gate JFETs 1.0.0". Below the title, it says "By Colin McAndrew<sup>1</sup>, Kejun Xia<sup>2</sup>" and lists affiliations: "1. Freescale Semiconductor 2. NXP Semiconductors". A description follows: "JFETIDG is a compact model for independent dual-gate JFETs. It is also applicable to: resistors with metal shields; the drift region of LDMOS transistors; the collector resistance of vertical bipolar transistors; and junctionless MOS transistors." There is a "Download Bundle" button, a note "Additional materials available", and a version box: "Version 1.0.0 - published on 02 Apr 2017" with a DOI link "doi:10.4231/D3TD9N91H - cite this". Below the version box is the license information: "Licensed under NEEDS Modified CMC License according to these terms". On the right side, there are statistics: "84 total view(s), 21 download(s)", "0 review(s) (Review this)", "0 wish(es) (Add a new wish)", "0 questions (Ask a question)", and "0 citation(s)". At the bottom right, there is a "Share" button with social media icons for Facebook, Twitter, and LinkedIn.



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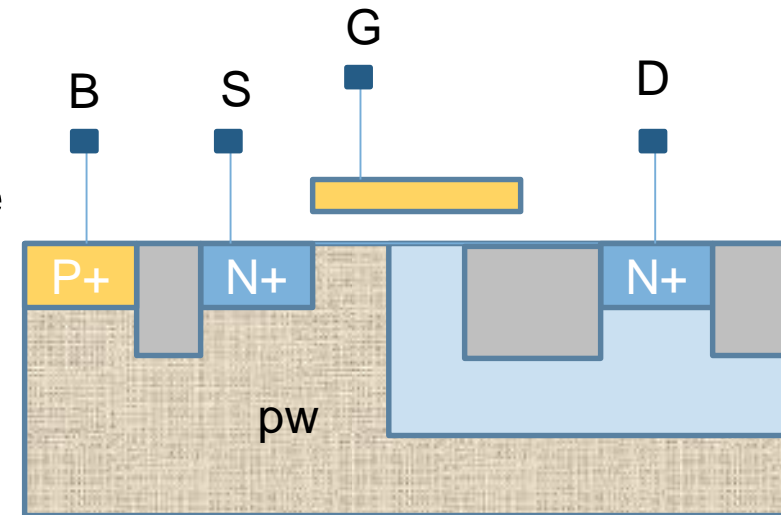
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# Drift Region of LDMOS (HVMOS)

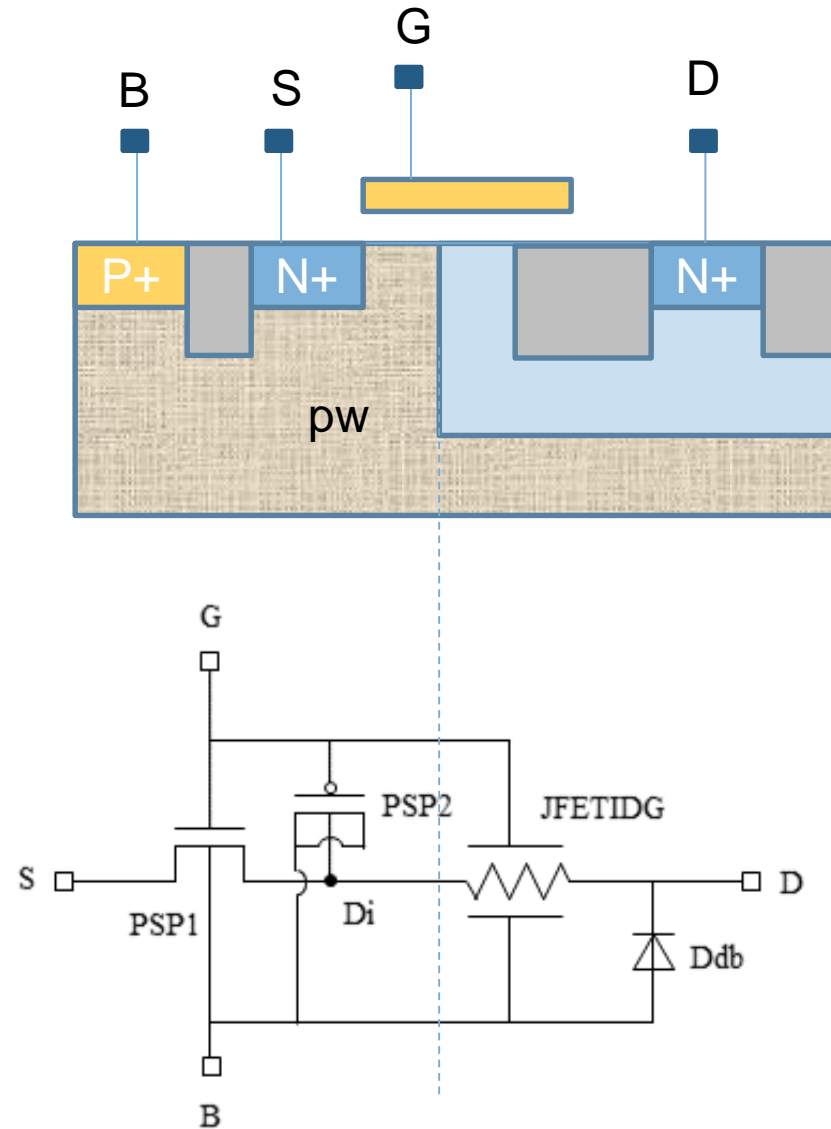


# Key Model Features Suitable for LDMOS modeling

- Velocity saturation.
  - quasi-saturation effect seen in LDMOS transistors can be modeled
- Physically model the dual gate effects
  - Its bottom gate is a p-n junction. The  $V_{db}$  modulation effect on the drift region resistance is modeled.
  - Its top gate is an MOS gate. The  $V_{gdi}$  modulation effect on the drift region resistance is modeled.
- drift region avalanche current
- the avalanche current modulation effect on the drift region resistance
  - The drain current expansion effect can be modeled
- Self-heating
  - modeled via an RC thermal network.



# Equivalent Circuit of LDMOS Model

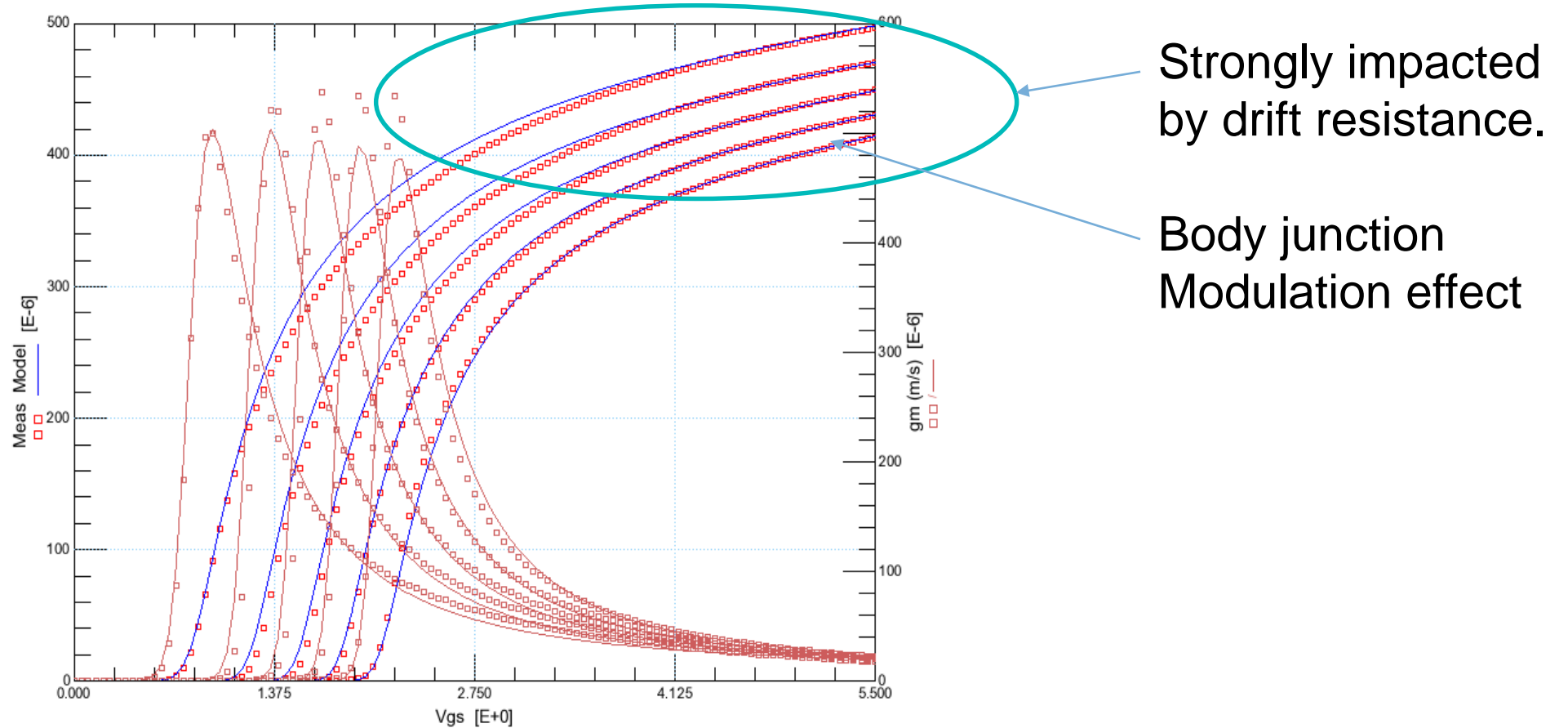


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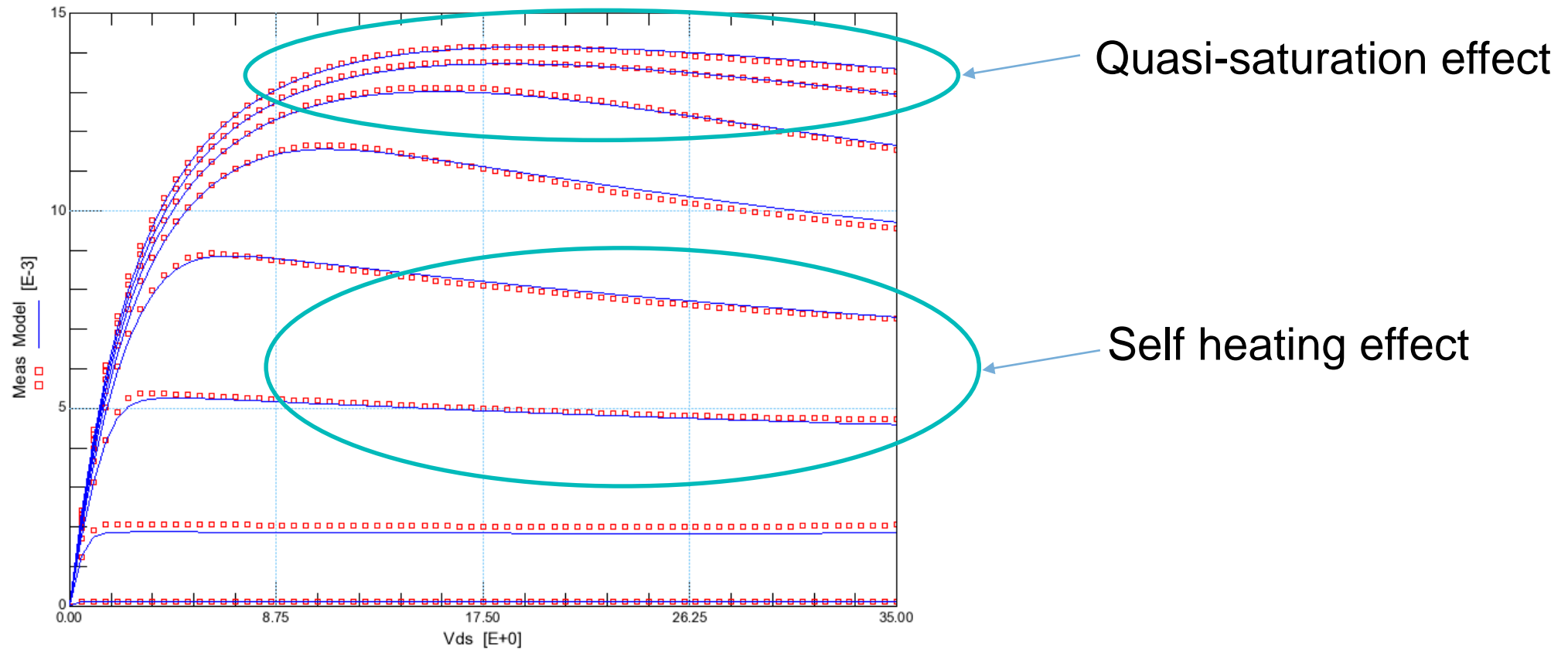
# Case 1: A 45V n-type LDMOS

- IdVg Lin



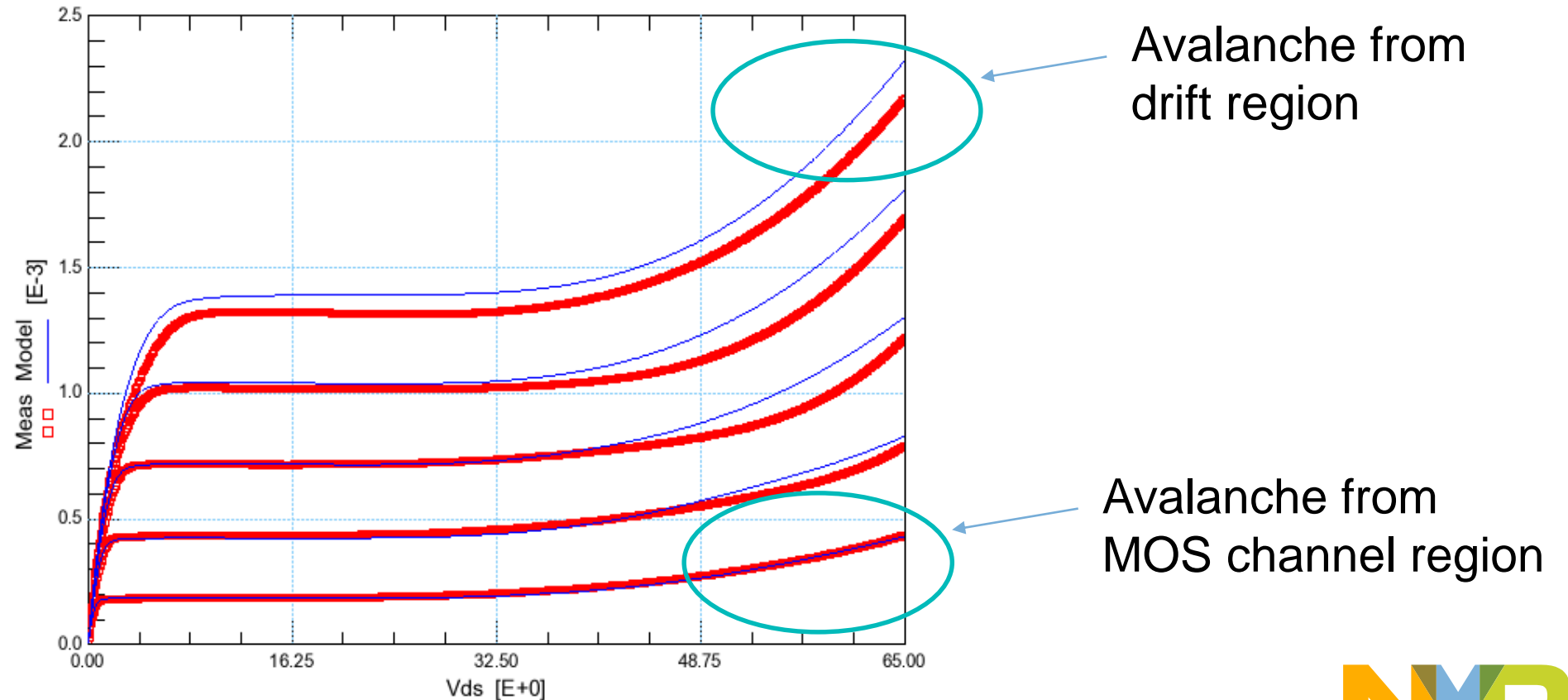
# Case 1: A 45V n-type LDMOS

- IdVd



# Case 2: A 65V n-type LDMOS

- IdVd at middle Vg

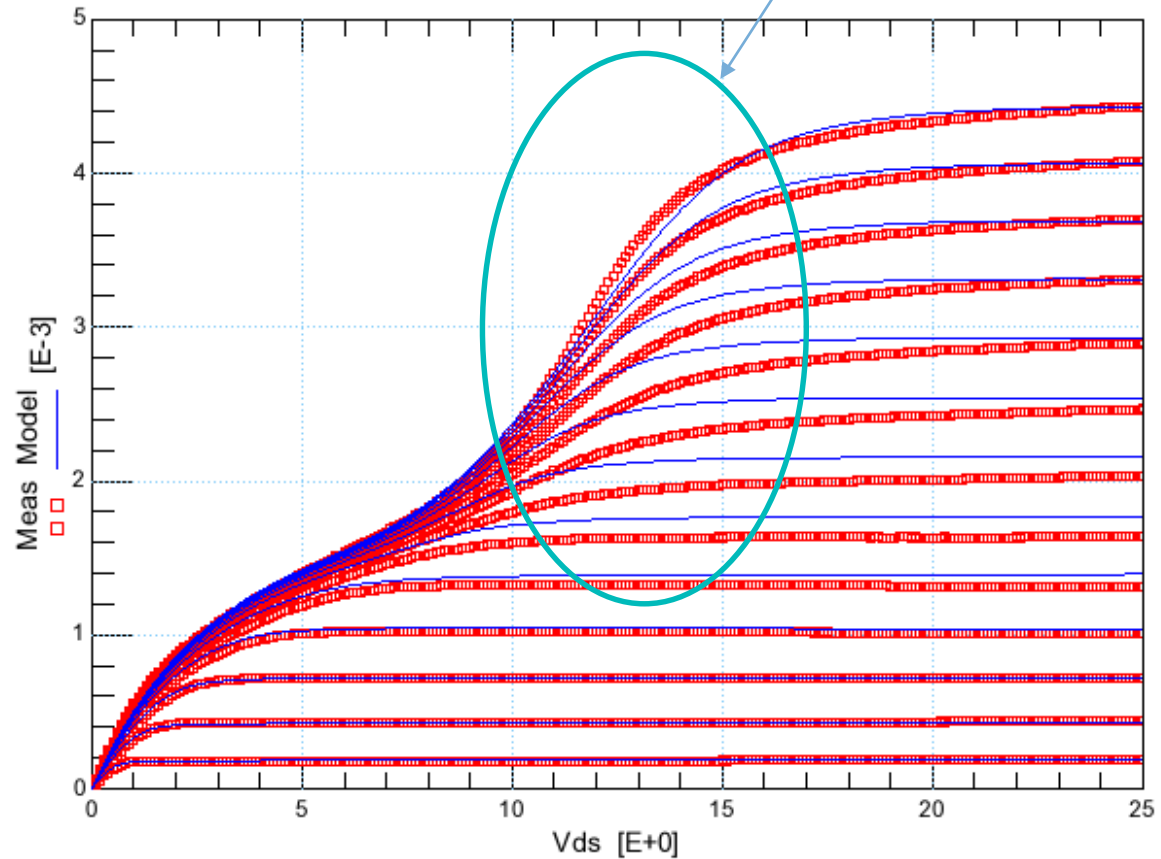




# Case 2: A 65V n-type LDMOS

- IdVd at high Vg

Drain expansion effect



# Convergence Tests

- Exhaustive test at device level
- Circuit level (using buck and boost converters)
- No any convergence issues

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