LDMOS MODELING
USING THE DUAL GATE JFET MODEL JFETIDG

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AGENDA

- Motivation
- JFETIDG model
- New LDMOS model
- Some Modeling Results
- Q&A

Motivation

- SPHV is a very good LDMOS model. However, it is not public.

- We want to make a good LDMOS model for everyone.

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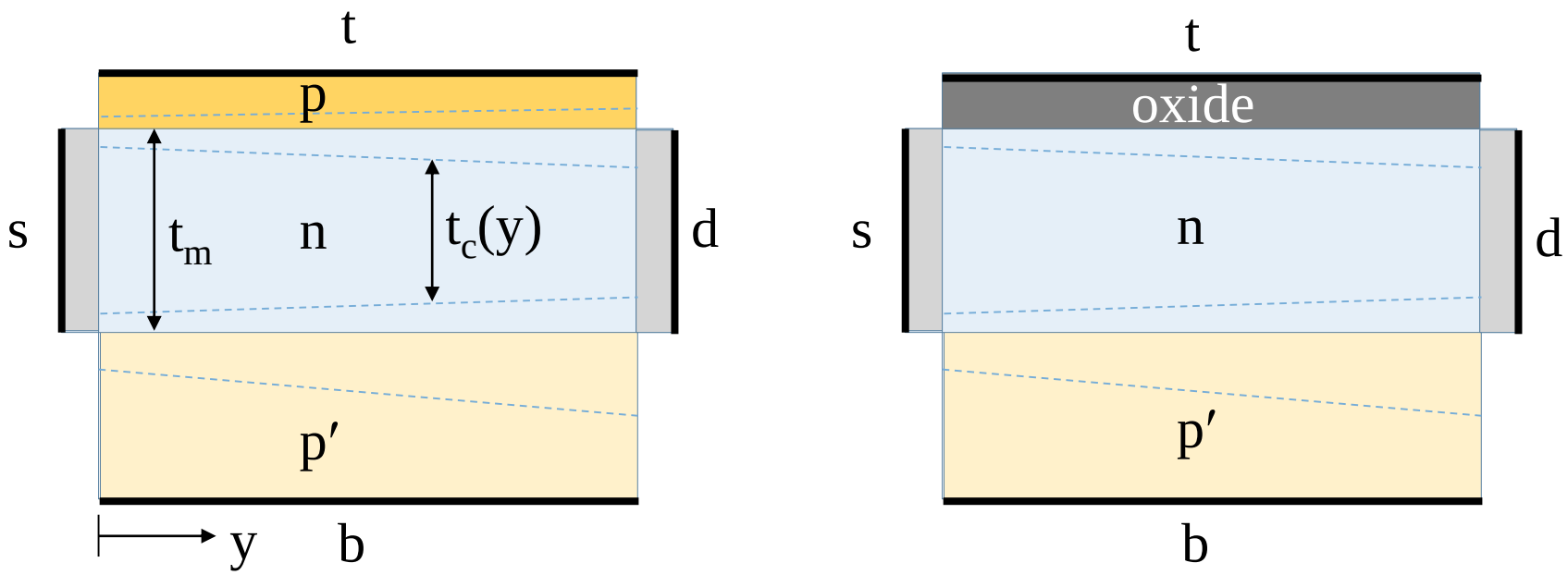
Generalization of JFET Concept

- Traditionally: Gate is pn-junction
- Generalized: Gate can be pn-junction or MOS
- Mathematically, both gate type can be described by
  - depletion factor (d_f)
  - built-in potential (ψ_r)



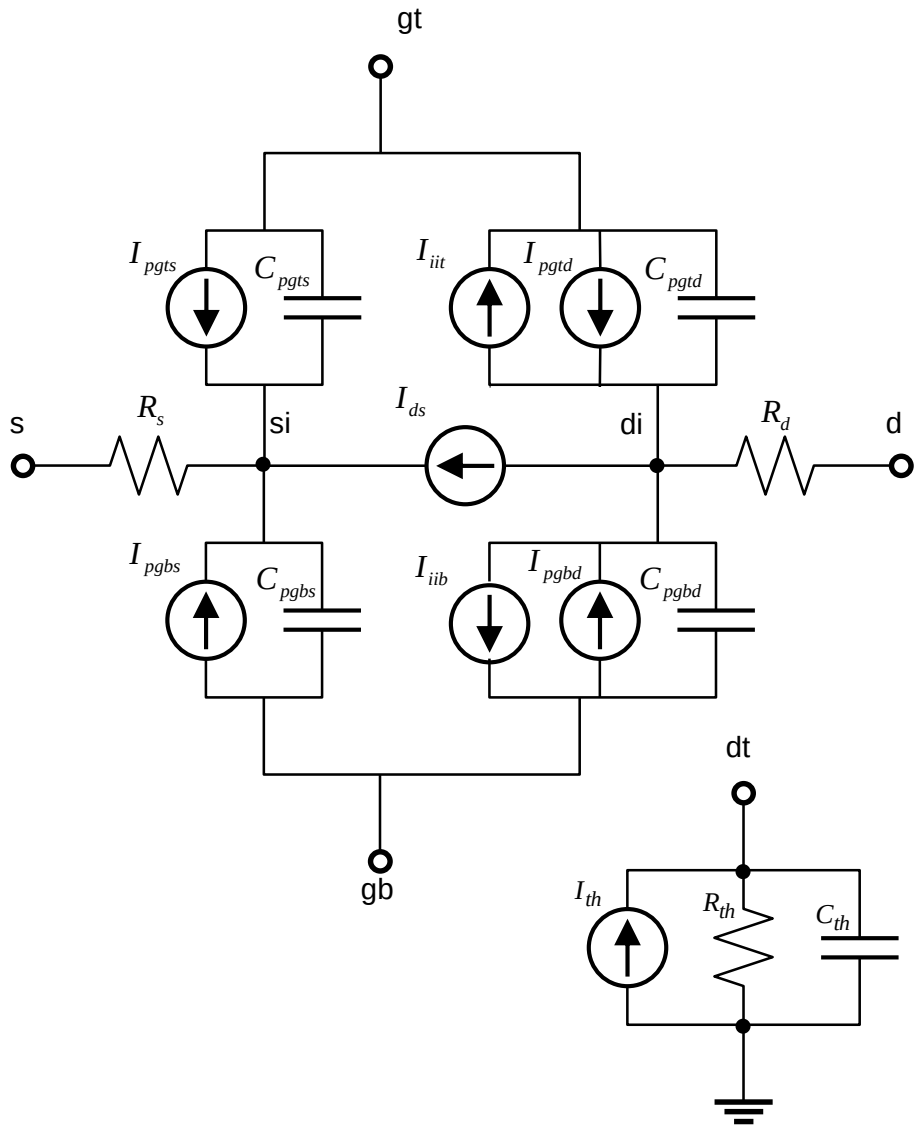
Applications of Generalized Dual-gate JFET Model

- Case I: 2 pn junction gates
  - Dual-gate JFET per si
  - Collector resistance of 4-terminal vertical bipolar transistors

- Case II: 1 pn junction + 1 MOS gates
  - Resistors (diffused or polysilicon) with metal shields
  - Drift region of LDMOS transistors with field plates (Next page)

- Case III: 2 MOS gates
  - Recently developed junctionless MOSFETs

Equivalent Circuit of JFETIDG



Release of the JFETIDG Model

- Ver 1.0.0 (Apr 2, 2017)
  - Public, through NEEDS license
  - Published on nanoHUB

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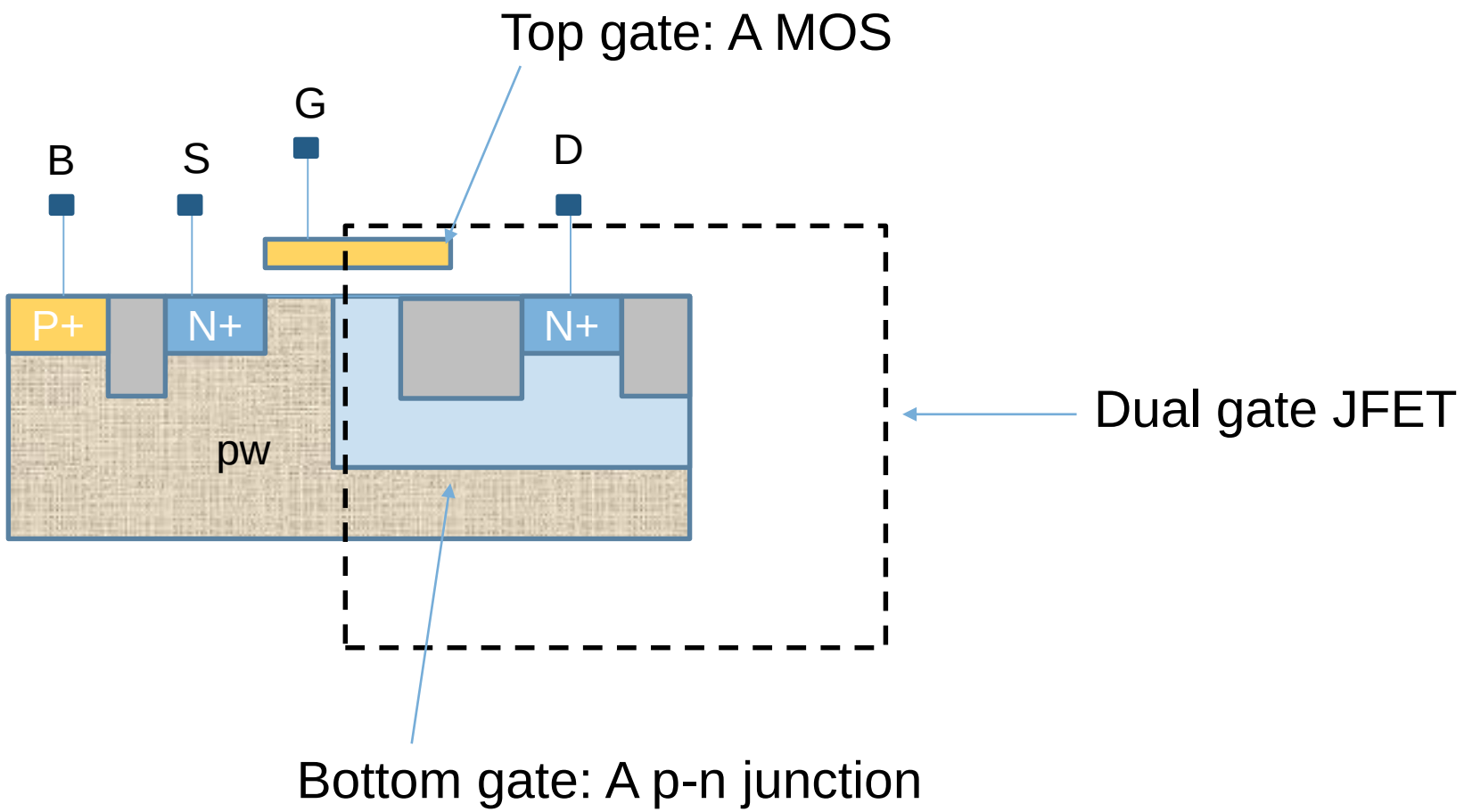
Drift Region of LDMOS (HVMOS)



Key Model Features Suitable for LDMOS modeling

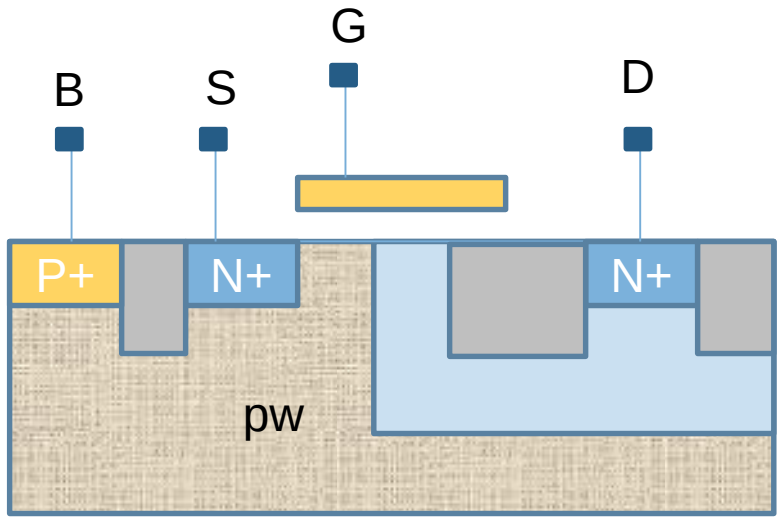
- Velocity saturation.
  - quasi-saturation effect seen in LDMOS transistors can be modeled

- Physically model the dual gate effects
  - Its bottom gate is a p-n junction. The V_{db} modulation effect on the drift region resistance is modeled.
  - Its top gate is an MOS gate. The V_{gdi} modulation effect on the drift region resistance is modeled.

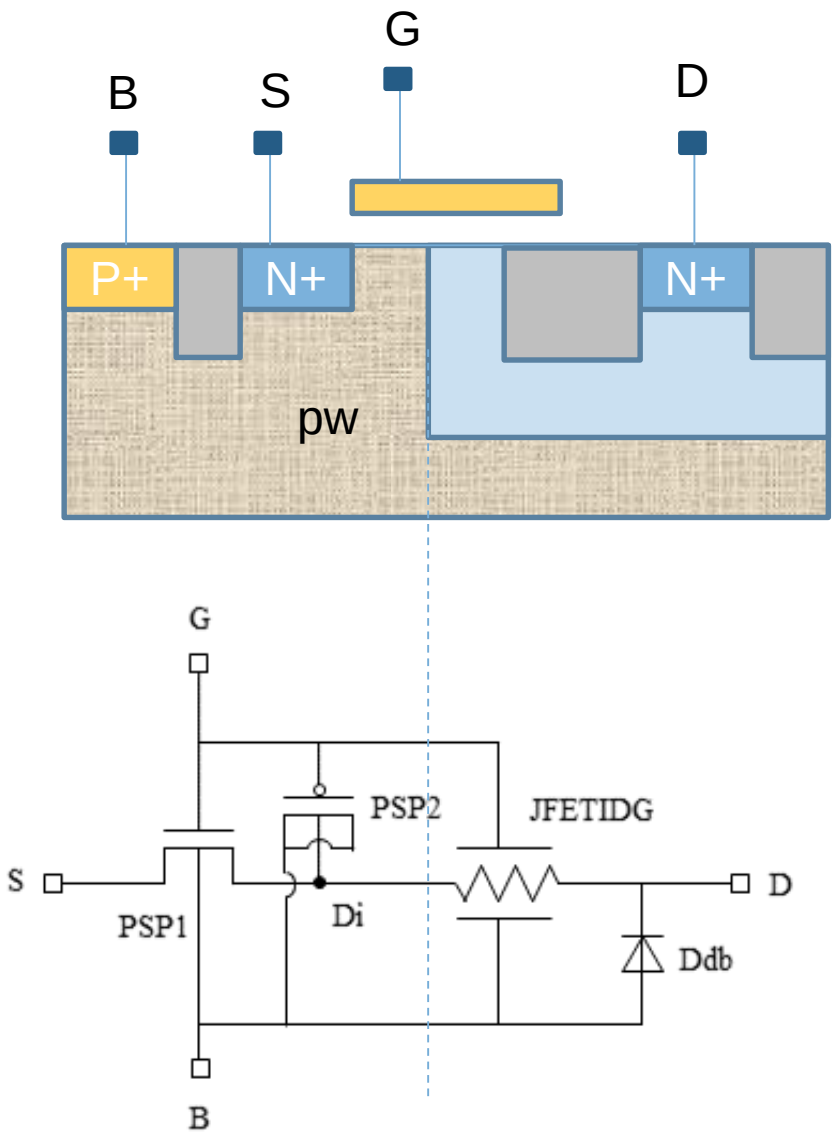
- drift region avalanche current

- the avalanche current modulation effect on the drift region resistance
  - The drain current expansion effect can be modeled

- Self-heating
  - modeled via an RC thermal network.



Equivalent Circuit of LDMOS Model



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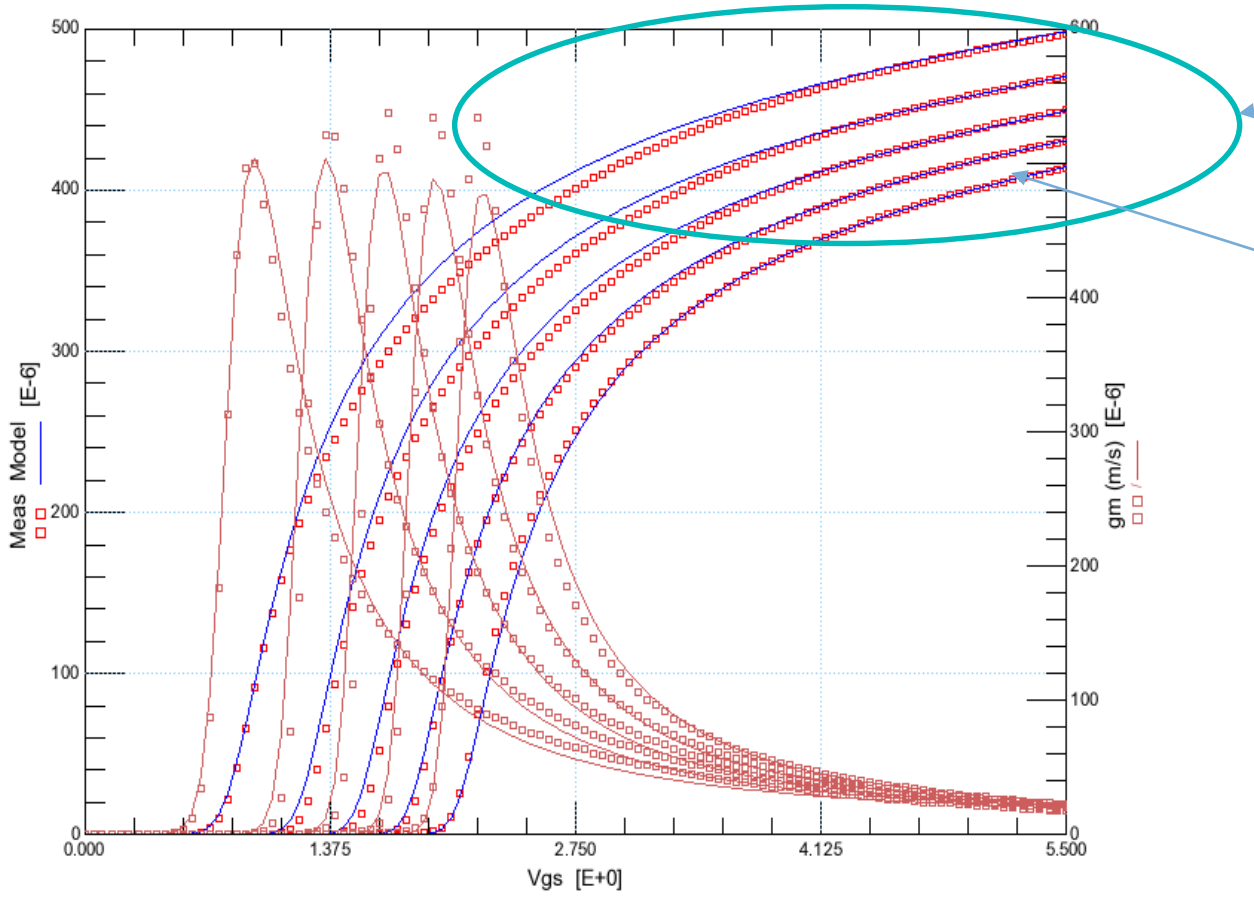
Case 1: A 45V n-type LDMOS

- IdVg Lin

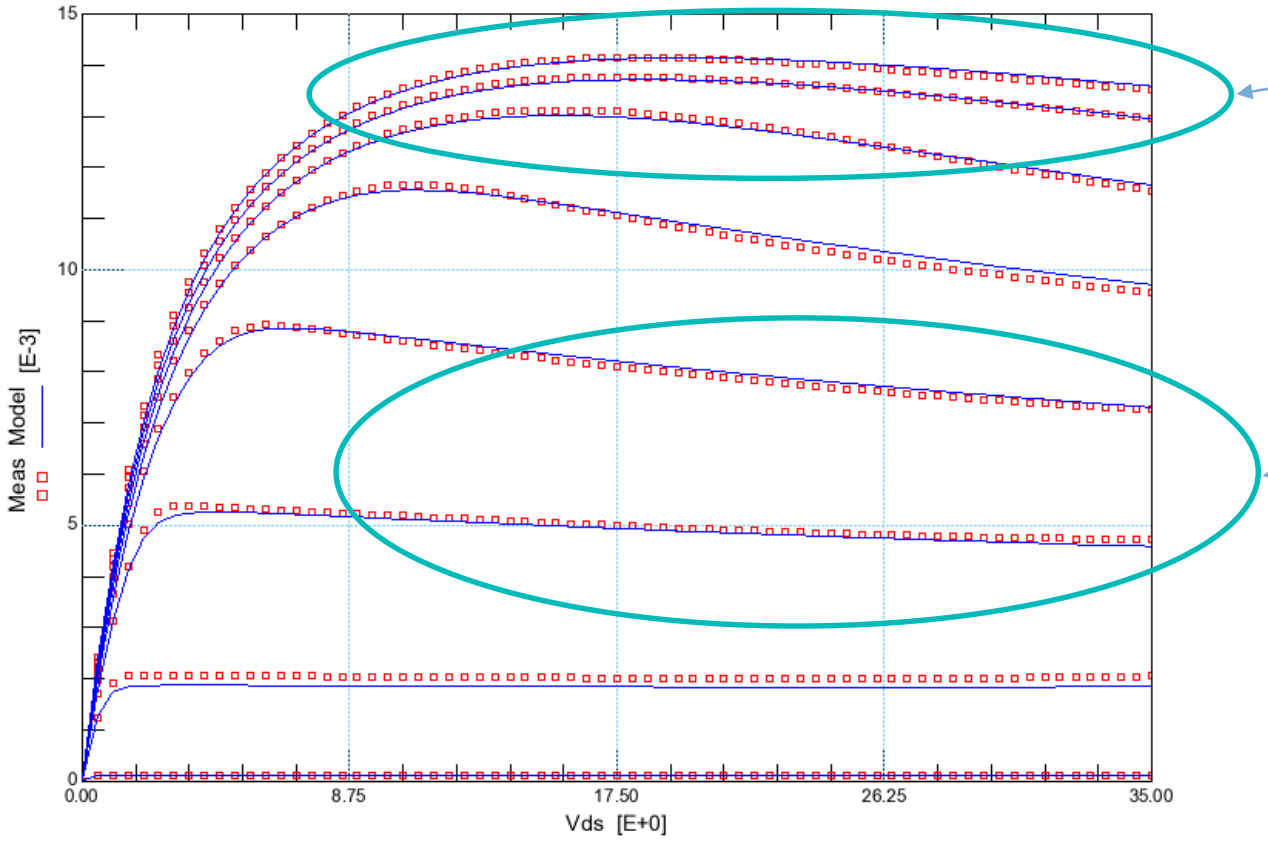


Strongly impacted by drift resistance.

Body junction Modulation effect

Case 1: A 45V n-type LDMOS

- IdVd

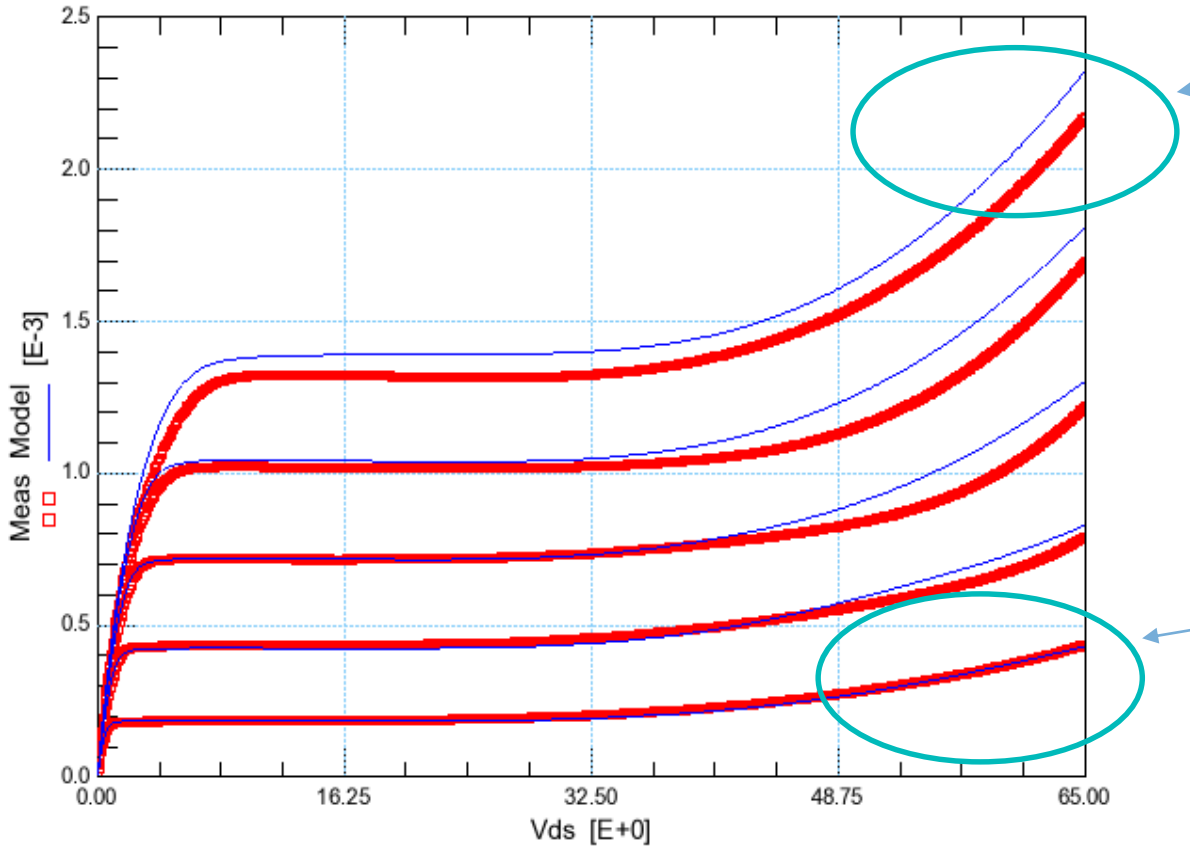


Quasi-saturation effect

Self heating effect

Case 2: A 65V n-type LDMOS

- IdVd at middle Vg



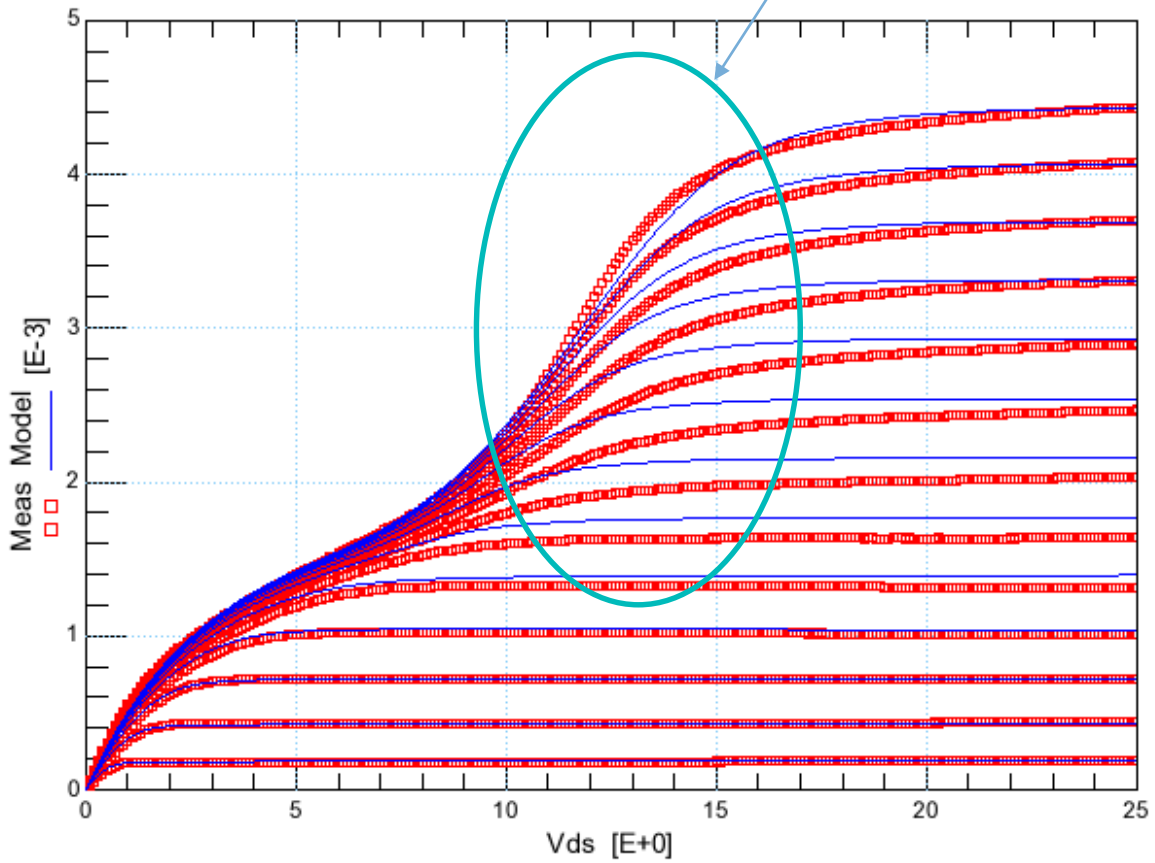
Avalanche from drift region

Avalanche from MOS channel region

Case 2: A 65V n-type LDMOS

- IdVd at high Vg

Drain expansion effect



Convergence Tests

- Exhaustive test at device level
- Circuit level (using buck and boost converters)

- No any convergence issues

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