An Automatic Parameter Extraction Procedure for an Explicit Surface Potential Based Compact Double Gate MOSFET Model

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COMON: COmpact MOdeling Network

- Industrial partners
- Academic partners
- Associate partners

- AIM-software
- UNIK Kjeller

RFMD UK
UCL Louvain-la-Neuve
UdS Strasbourg
EPFL Lausanne
Dolphin Integration Grenoble
URV Tarragona
FH Giessen
TUI Ilmenau
Melexis Ukraine
ITE Warsaw
AdMOS
Infineon Munich
Austria Microsystems
TUC Chania

COMON is a consortium of 15 European universities and companies funded by the European Union.

The goal of the project is to transfer the scientific and technological knowledge in compact device modeling from academia to industry and vice versa.

The coordinator of this team is Prof. Benjamin Iniguez, from University Rovira i Virgili.

More information available on: http://www.compactmodelling.eu
Introduction

Relation inside the COMON project:

- Parameter Extraction Technique has been applied for Multiple-Gate MOSFETs within the framework of workpackage WP1 (COMON/D1.7).

- The parameter extraction relies on a commercial software with collaboration between AdMOS company in Germany and University of Rovira i Virgili from Spain.

- Developed core model is for DG MOSFET, and the model can be adapted for DG FinFET and Trigate MOSFETs as well.
Device Structure

- The core model is developed for Double Gate (DG) MOSFET

- The model can be modified and adapted for DG FinFET structure

- The results and details are published:
  
  
In this work we have adapted the core model for Trigate MOSFET.

We have used Trigate MOSFET measurements in order to extract the model parameters.

Comparison of the model calculations using extracted parameters and measurements for Trigate MOSFET will be shown in the next slides.
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Core Model

The CORE MODEL for symmetric doped Double-Gate MOSFETs has the following features:

✓ The Model is explicitly surface potential based (not charge based)

✓ Regarding the silicon layer (channel) doping concentration:
  The model works from undoped silicon layer to highly symmetric doped silicon layer (up to Na=2x10^{18} cm^{-3})

✓ The core model is for long channel and does not include short channel effects

✓ Mobility is constant and not variable and does not take into account short channel effects.
Surface Electrical Field

Charge density inside the Si layer as a function of the potential is equal:

$$\rho = q(p-n-Na) = q \left( \frac{\phi_{FP} - \phi}{\phi_t} - n_i e \frac{\phi - \phi_{Fn}}{\phi_t} - n_i e \frac{\phi_{FP}}{\phi_t} \right)$$

The electric field at the surface of the silicon layer is calculated using Poisson equation:

$$E_s = \frac{2qNa \phi_t}{\varepsilon_s} \sqrt{\left( \frac{\phi_s - \phi_0}{\phi_t} \right) + \left( 1 - e^{-\frac{(\phi_s - \phi_0)}{\phi_t}} \right) \cdot e^\frac{\phi_s - 2\phi_{FP} - V}{\phi_t}} = \frac{Q_{sem}}{\varepsilon_s} = \frac{1}{\varepsilon_s} \left( Q_n + \frac{Q_b}{2} \right)$$

The surface electric field is obtained as a function of potential at the surface ($\phi_s$) and at the center of the Silicon layer ($\phi_0$).

Potential along the channel is equal: $$V = \phi_{Fn} - \phi_{FP}$$ and $$\phi_{FP} = \phi_F$$
Surface Electrical Field

Using our surface electric field equation calculations with numerical simulations (Silvaco ATLAS) show good agreement:

Model and ATLAS simulation of the surface electric field at the Si-SiO$_2$ interface into SiO$_2$ as a function of gate voltage at $V_d=0V$.  

Model and ATLAS simulation of the surface electric field at the SiO$_2$-HfO$_2$ interface into HfO$_2$ as a function of gate voltage at $V_d=0V$.  

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Surface Potential

Using the principal branch of Lambert function LW, the surface potential of the Si layer corresponding to the below threshold condition:

\[
\phi_{S_{bt}} = V_G - V_{FB} - \phi t \frac{q_b}{2} - \phi t \cdot \text{Lamb} \left( \frac{q_b}{4} e^{\frac{V_G - V_{FB} - 2\phi_F - \phi q_b}{2\phi}} \right)
\]

The surface potential of the Si layer corresponding to the above threshold condition:

\[
\phi_{S_{at}} = V_G - V_{FB} - 2\phi t \cdot \text{Lamb} \left( \frac{1}{2} \sqrt{\frac{q_b}{2}} \sqrt{1 - e^{-\alpha}} \frac{V_G - V_{FB} - 2\phi_F - V}{2\phi} \right)
\]
Surface Potential

Merging the solutions for the surface potential in the below and above threshold regimes the complete expression for the surface potential becomes:

\[
\phi_s = \phi_{s_{bt}} \frac{1}{2} \left[ 1 - \tanh \left( 20 \cdot (V_G - V_T) \right) \right] + \phi_{s_{at}} \frac{1}{2} \left[ 1 + \tanh \left( 20 \cdot (V_G - V_T) \right) \right]
\]

The surface potential calculations show good agreement with the numerical simulations (Silvaco ATLAS).

Model and ATLAS simulation of the surface potential at the Si-SiO₂ interface as a function of gate voltage at \(V_d=0\) V.
Drain Current for Long Channel

Total drain current considering both surfaces (gates)

\[ I_{DS} = 2 \frac{W}{L} \mu C_{ox} \phi t \int_{V_S}^{V_D} q_n(V) dV \]

For Long channel device (without short channel effects)
For \( \mu = \text{constant} \)
and using the relation between \( dV \) and \( dq_n \) \( (dq = cdV) \)
calculation of the integral gives:

\[ I_{DS} = \left( 2 \frac{W}{L} \mu_0 C_{ox} \phi t^2 \right) \left[ \frac{q_{ns}^2 - q_{nd}^2}{2} + 2(q_{ns} - q_{nd}) - q_b \ln \left( \frac{q_{ns} + q_b}{q_{nd} + q_b} \right) \right] \]

- \( q_{ns} \) - Normalized mobile charge at source as function of \( V_G \) at \( V_D = 0 \) V
- \( q_{nd} \) - Normalized mobile charge at drain as function of \( V_G \) and \( V_{Deff} \)
- \( q_b \) - Normalized total fixed charge in the silicon layer
Short Channel Effects

Model with variable mobility and short channel effects (SCE) taken into account:

- $V_T$ variation with channel length reduction ($V_T$ roll-off) and DIBL effect;
- Velocity saturation effects;
- Effect of series resistance $R$ as a function of the external voltage;
- Effect of electric field along the channel on channel shortening;
- Subthreshold slope degradation.


Drain Current including Short Channel Effects

\[ I_D = \frac{1}{\left(1 - \frac{\Delta L}{L}\right)} \left\{ 1 + \left(\frac{E_{MS}}{E_1}\right)^{P_1} + \left(\frac{E_{MS}}{E_2}\right)^{P_2} \right\} \left\{ 1 + \left(\frac{\mu_S V_{Def}}{v_{sat} L}\right)^2 \right\}^{\frac{1}{2}} + \left[ 2K \cdot R \cdot |V_{GT} - \beta \cdot V_{Def}| \right] \]

\[ K = \frac{W}{L} C_{ox} \mu_0 \]
\[ \mu_S = \frac{\mu_0}{1 + \left(\frac{E_{MS}}{E_1}\right)^{P_1} + \left(\frac{E_{MS}}{E_2}\right)^{P_2}} \]
\[ \mu_{eff} = \frac{\mu_S}{\sqrt{1 + \left(\frac{\mu_S V_{ef}}{v_{sat} L}\right)^2}} \]

- We are using this expression in order to calculate drain current and extract the model parameters.
The Model Parameters

This model has only 9 adjusting parameters

(6 Mobility parameters):
- \( \mu_0 \) - Maximum mobility
- \( E_1 \) - Critical electric field
- \( P_1 \) - Exponent 1
- \( P_2 \) - Exponent 2
- \( E_2 \) and \( E_{2V} \) - Critical electric field
- \( E_2 = E_{20}(1 - E_{2V} \times V_{def}) \)

(3 other parameters):
- \( T \) or \( \text{vsat} \) - Adjust of saturation voltage
- \( R \) - Series resistance
- \( \lambda \) - Channel shortening parameter

Transistor dimensions = Instance Parameters

- \( L \) - Channel length
- \( W \) - Channel width

Technological parameters

- \( t_s \) - Silicon layer thickness
- \( N_a \) - Doping concentration
- \( t_{ox} \) - Dielectric layer thickness
- \( \varphi_{ms} \) - Metal work function
- \( N_{SS} \) - Interface states
Model Parameters Extraction Methods

- **Transistor dimensions:** CAD System / Circuit designers

- **Technological parameters** are obtained from the laboratory or factory which produces the transistor.

- **Model adjusting parameters** are extracted from measured current-voltage characteristics: transfer characteristic in the linear region; transfer characteristic in saturation and output characteristic.

  We have implemented automatic parameter extraction techniques.
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Model in Verilog A Code

- The presented model based on surface potential which was developed within the EU-funded COMON project is coded in Verilog-A.

- The model is linked through a Verilog-A capable simulator to the parameter extraction software.

- The implementation of automatic parameter extraction techniques (DC Extract) is presented for the model (in Verilog-A code).
Parameter Extractions

Parameter extractions are organized in an extraction flow. Users can select extraction steps from a pool of available functions:

- direct extractions
- optimizers
- manual tuners

The extraction function templates cover:

- Intrinsic transistor effects
- Transistor capacitance
- Diode: DC and capacitance effects
- High frequency parameters
The data handling routines of the Modeling Tools together with a flexible graphic driven optimizer allows the user to set up any kind of optimization or fine tuning task taking into account all kind of measured data.
Definition of User Specific Extractions

Knowing the physical effects of a model, modeling engineers can define a set of powerful extractions functions taking into account:

- One or more device(s) with different dimensions
- Data from different operating regions
- Model parameter(s)
- Typical PCM like data for a MOSFET like $V_t(L), I_{dsat}(L, W, ..)$

These functions reflect the knowledge how to extract certain parameters and can be re-used by other team members.

Furthermore, companies can put their Intellectual Property about parameter extraction into these customized functions without having the need to share it with the software provider.
This is an example of an extraction step, which takes into account various operating regions of a device showing currents and conductances.
### Extracted Parameters

The table shows the list of extracted model parameters:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MWF</td>
<td>4.679</td>
</tr>
<tr>
<td>MM0</td>
<td>1.550K</td>
</tr>
<tr>
<td>P1</td>
<td>3.054</td>
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<tr>
<td>E1</td>
<td>4.134G</td>
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<tr>
<td>P2</td>
<td>4</td>
</tr>
<tr>
<td>E2</td>
<td>6.923MEG</td>
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<tr>
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<td>FDVT0</td>
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<td>80.00m</td>
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<tr>
<td>SIGMA</td>
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<td>VSAT</td>
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<td>TAU</td>
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<td>R</td>
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<td>RD</td>
<td>218.4u</td>
</tr>
<tr>
<td>RS</td>
<td>955.3u</td>
</tr>
</tbody>
</table>
Results with Extracted Parameters

The drain current calculations as a function of drain voltages for different gate bias is shown using the values of extracted parameters.

The model calculations and experimental measurements of the drain current as a function of gate voltage in linear and logarithmic scales at $V_D = 0.05$ (V) and $V_D = 1$ (V) are shown for the extracted parameters.
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Conclusion

1) We presented an explicit surface potential based compact Double Gate MOSFET model including short channel effects, adapted to Double Gate FinFET and Trigate MOSFETs.

2) The implementation of the model in the commercial software package has been done using the verilog-A model description.

3) The accuracy of the simulated curves, incorporating the extracted parameters in our compact analytical model for obtaining accurate electrical simulation is verified with real Trigate MOSFET measurements.

4) A very good agreement between simulation and measurements is achieved, confirming the validity of the proposed model.
Thank you