Compact Model Extensions for Realistic Circuit Simulation: a Perspective from Industry

MOSAK Workshop

Jaypee Institute of Information Technology (JIIT)

Noida, 16th March 2012
While CMOS Technology scaling has been steadily pursued to offer deca-nanometer devices, Circuit Design Community has benefited from successful development of core compact models able to capture important aspects of MOSFET electrical behavior in Circuit simulation tools. While BSIM4 models is still widely used within Industry for planar Bulk and SOI CMOS technologies, new MOSFET model generation (PSP, HiSIM…) has enabled high accuracy for Analog-Rf Circuits Design. Moreover, innovative modeling solutions are coming to Industry for new devices like planar FDSOI or 3D Finfet transistors.

Beyond the successful development of core models from Academia, model extensions are still needed to be developed in Industry for a bunch of Technology and Design dependent effects, in close interaction with the Design tool providers to enable continuity of Design flow.

Presentation will highlight model extensions developed in Industry to account for realistic Layout of single devices met due to circuit integration; examples of applications dealing with modeling of MOSFET Parasitics and Layout Proximity effects will be highlighted. The presentation is intended to bring circuit designers and compact modelers with a survey of such effects through their potential impact, and examples of methodology implementation.
Contents

• MOSFET Compact Model Extensions for Realistic Circuit Simulation: A Perspective from Industry

• Objective

• Parasitic capacitances

• Layout Proximity effects

• Reliability aware Design

• Summary and Perspective
Objective

- **Core** models account for Bias, Geometry (W/L/NF) and Temperature, Noise

- **Extensions** account for Parasitics, Layout effects, Process Variations, and Ageing

- **Circuit simulation methodologies** need to be adapted concurrently and made compatible with Design flow

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MOSFET Parasitics
MOSFET Parasitic effects

• Extrinsic Parasitic capacitances

• Dependences to Layout

• Modeling/Simulation approach

• Perspective and ITRS
MOSFET Parasitic Capacitances

- Even for Planar Mosfets, Parasitic Capacitances surrounding gate is a 3D problem

- $C_{gg}$ @ $L_{nom}$ almost x2 through lateral coupling between Gate and SD regions

- $C_{gg}$ depends on W/L, S/D cts number/pitch, distance between gate and S/D cts
Scaling of MOSFET Capacitance partitioning on gate length

- \( L_{\text{scaling at } W_{\text{mean}} \text{ mean}} \)
  - \( L_{\text{min}}: 40\% \text{ C}_{\text{gg}} \text{ is extrinsic} \)
    - Gate to S/D diffusion
    - Gate to S/D contacts
  - \( L_{\text{min} \times 10}: 90\% \text{ C}_{\text{gg}} \text{ is extrinsic} \)
Scaling of MOSFET Capacitance partitioning on gate W

- **W scaling @Lnom**
  - **W large:** 40% $C_{gg}$ is extrinsic
    - Gate to S/D diffusion
    - Gate to S/D contacts
  - **W Narrow:** up to 53%
    - Corner capacitances

J. Mueller, SSE 2006

W dependence @Lmin

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MOSFET capacitances in real Design (S/D Contact Position vs Gate)

- Extrinsic Capacitances depend on
  - SD contact distance to gate (left)
  - Number of contacts (right)

- Solutions:
  - Core models: limited layout assumptions => suited for Pre-Layout simulation
  - PEX tool: adaptative to Layout style => suited for Post-Layout simulation
  - Number of netlist instance parameters required minimum for large circuit simulation

Scaling Capacitances vs distance S/D Cts to Gate

Semi-regular Std cell layout (Example)
MOSFET capacitances in real Design
(Adaptative simulation flow)

- Pre-layout simulation (default layout)
- Post-layout simulation (real layout)

contains:
- network
- device instantiation
- device parameters 
  (As/Ad/Sa/Sb/…)
  for default layout
- Mosfet R C parasitics for default layout, computed by SPICE model

contains:
- network
- device instantiation
- device parameters 
  (As/Ad/Sa/Sb/…)
  computed from layout
- device parameters can be
  “geometrical” or “electrical”

Addition of R C parasitics, computed from layout
Applies to MOSFET devices and interconnect

Simulation results

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Verification DOEs: Impact on RO frequency

- F increase vs dgc: benefit of extrinsic capacitance reduction
- Efficient CAD accuracy monitoring methodology.

<table>
<thead>
<tr>
<th>RO</th>
<th>dgc</th>
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</thead>
<tbody>
<tr>
<td>FEX09</td>
<td>Min</td>
</tr>
<tr>
<td>FEX10</td>
<td>X 1.43</td>
</tr>
<tr>
<td>FEX11</td>
<td>X 2.5</td>
</tr>
<tr>
<td>FEX12</td>
<td>X 5</td>
</tr>
</tbody>
</table>

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MOSFET Parasitics vs ITRS roadmap

- From ITRS, we have for each year and each device structure the following parameters:
  - \( L \)
  - \( \text{CPP (contacted gate pitch)} \)
  - \( t_{\text{inv}} \)
  - \( x_j \) for Bulk devices
  - \( t_{\text{si}} \) for FDSOI or multigate devices

- Structural parameters are derived =>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Evaluation</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{sp} )</td>
<td>(CPP-L)/3</td>
</tr>
<tr>
<td>( H_g )</td>
<td>( 2L )</td>
</tr>
<tr>
<td>( W_{\text{ext}} )</td>
<td>( L )</td>
</tr>
<tr>
<td>( W )</td>
<td>( 3\times\text{CPP} )</td>
</tr>
<tr>
<td>( dL )</td>
<td>( L/4 )</td>
</tr>
<tr>
<td>( t_{\text{ox}} )</td>
<td>( 2t_{\text{inv}} )</td>
</tr>
<tr>
<td>( W )</td>
<td>( 3\times\text{CPP} )</td>
</tr>
<tr>
<td>( H_{\text{si}} )</td>
<td>( 3x t_{\text{si}} )</td>
</tr>
<tr>
<td>( \text{FP} )</td>
<td>( t_{\text{si}} + H_{\text{si}} )</td>
</tr>
<tr>
<td>( N_{\text{fin}} )</td>
<td>( W/\text{FP} )</td>
</tr>
<tr>
<td>( t_{\text{mask}} )</td>
<td>( t_{\text{si}} )</td>
</tr>
</tbody>
</table>

- Parasitics impact have been evaluated for each year for the following devices: Bulk, FDSOI, planar DG and FinFET (J.Lacord, SSDM 2011)
MOSFET Parasitics vs ITRS roadmap

Bulk FET cross-section

FinFET cross-section

FinFET top view

Courtesy of J. Lacord, SSDM 2011
MOSFET Parasitics vs ITRS roadmap

Total Gate + Parasitics over Gate cap. Ratio

- ITRS Parasitics weight and evolution below FS simulation
- Planar DG presents a lower $\frac{C_{tot}}{C_{gc}}$ ratio than FinFET

![Graph showing MOSFET Parasitics vs ITRS roadmap](image)

Courtesy of J. Lacord, SSDM 2011

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MOSFET Layout Proximity Effects
Layout Proximity effects

- Overview
- Modeling approach
  - STI example
- Modeling Accuracy dilemma
- Simulation flow
- CAD Accuracy
Layout Proximity effects: STI example

STI stress effect on Mobility (RA Bianchi, IEDM 2002)

STI stress effect on Mobility and VT (Tsuno, VLSI 2007)

- Regular Layout: Mobility impacted by Stress, VT impacted by SD diffusity (modulated by stress)
- Handling Complex Layout in Design flow requires approximations:
  - Implementation shared by Netlisting (Geometrical parameters) and Model (Electrical parameters)
  - Accuracy verification is challenging
## MOSFET Layout Proximity effects overview

<table>
<thead>
<tr>
<th>Effect</th>
<th>Contributions</th>
<th>Critical distance</th>
<th>Post-Layout Per Instance parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPE</td>
<td>Ion scattering on well photoresist</td>
<td>&gt;1um</td>
<td>SCA, SCB, SCC</td>
</tr>
<tr>
<td>STI(LOD)</td>
<td>STI Stress SD diffusion</td>
<td>1um Local</td>
<td>SA, SB</td>
</tr>
<tr>
<td>STI (OD2OD)</td>
<td>Litho and Etch STI stress</td>
<td>Context 1um</td>
<td>VT and Mu correction</td>
</tr>
<tr>
<td>Active corner rounding</td>
<td>Litho and Etch</td>
<td>Local</td>
<td>Wreff correction</td>
</tr>
<tr>
<td>Gate pitch</td>
<td>Litho and Etch CESL Stress SD diffusion</td>
<td>Context context up to 1 um Local</td>
<td>VT and Mu correction</td>
</tr>
<tr>
<td>Gate corner rounding</td>
<td>Litho and Etch</td>
<td>Local</td>
<td>Leff correction</td>
</tr>
<tr>
<td>Contacts position</td>
<td>SD Rseries Channel stress</td>
<td>Local</td>
<td>Rs and Cs correction</td>
</tr>
<tr>
<td>Others …</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- A bunch of Design dependent effects related to distances between Well, Gate, Active, Contact layer patterns and related density context
- Different physical effects interplay; impact, amplitude are technology dependent
- Each transistor sensitivity to each effect also depends on instance W/L

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MOSFET proximity effects: Accuracy dilemma

- A bunch of effects with 1-10% impact of performance (Low Power technology), and more (High Power technology, where Stress effect is dominant)

- **Characterization dilemma: Layout DOEs**
  - WPE: 4W x 4L x 6 distances x 2 orientations x 2 N/P devices = 394 DUTs
  - Overall about 2K DUTs per N/P device, not considering interaction between effects!

- **CAD Netlisting dilemma: Post Layout extraction**
  - Nb Geometrical instances > 100, loss of simulation efficiency
  - Pre-processing of geometrical/ electrical parameter variation through LVS: a must!

- **Modeling:**
  - Compact modeling of all effects with interactions is not experimentally applicable
  - Focus on first order layout effects and their dependence with W/L
  - Monitoring of CAD + Models accuracy through test structures offering efficient test methods

Layout example

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MOSFET capacitances in real Design
(Adaptative simulation flow)

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contains:
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Addition of R C parasitics, computed from layout
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Simulation results

Simulation results

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MOSFET Layout Proximity effects: CAD Accuracy

- Example of Monitoring Gate Pitch effects with Ring Oscillator: CAD to Silicon mismatch can be depicted.
Reliability Aware Design
Reliability Aware Design

- Reliability aware design
- Results: Std Cells
Reliability-aware design

DEVICE LEVEL

CIRCUIT LEVEL

All degradation modes impact?

Reliability impact on circuits is a function of
- operating modes of circuits,
- operating conditions faced by devices as a combination of these modes and the various input stimuli
- sensitivity of the performance of the circuit in the context of its place in design hierarchy
  E.g., a small shift in differential pair could affect the product, while a big shift in transistors in a power-down control block may affect nothing

Design-in Reliability (DiR) =
set of methodologies and tools enabling quantitative reliability assessment at design-level

- Translate device reliability information for use by circuits
  - Library reliability information is requested by system designers
- Identify potential reliability problem conditions
  - Take into account the actual operating conditions of a design library
    - mode, stimuli, ambient conditions
- Secure without over-design

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Reliability-aware modeling – Std cells results

- Reliability CAD values must be compared to drifts observed during HTOL test campaigns on library qualification testchips.

Source: N. Ruiz, CICC 2011
Summary

• Mosfet parasitics are performance limiting factors
  • Extrinsic cap may exceed ~x2 intrinsic cap for coming device generations

• Impact of Layout effects is difficult to estimate for coming technologies (as long as impact of each individual effect is less than 10 %).
  • The experimental methodology learnings to account for these effects in current technologies will help

• Reliability aware Design is coming
  • Requires a set of methodologies and tools enabling quantitative life-time assessment at circuit-level

• In Industry, those subjects will keep attention from the Modeling and Reliability expert communities from now and through the coming years.
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