1. Introduction:
- FinFET: Promising multi-gate structure
- Mathematical models for FinFET device are under investigation and study
- Look-up Table (LUT) approach does not require physical description of device
- Process, voltage, and supply (PVT) variations can be considered in automatic circuit design

2. \( I_D - V_G \) Template based LUT Approach:
- Difficult to model moderate inversion region
- \( I_D - V_G \) at \( V_{DS} = V_{DS_{max}} \) is taken as a template
- \( I_D - V_G \) at other \( V_{DS} \) is normalized with template
- Normalized data is easily fitted with cubic splines
- \( I_D - V_G \) template based approach accurately models moderate inversion region and does not require non-uniform grid points

3. Automatic Circuit Design Platform:
- \( I_D - V_G \) template based LUT approach is implemented in SEQUEL circuit simulator
- Particle Swarm Optimization (PSO) algorithm is used for circuit optimization
- Optimizer is integrated with SEQUEL circuit simulator for automatic circuit design for given specification
- PSO algorithm mimics behavior of birds flocking in search of food and reported to be efficient in solving multimodal optimization problem

4. Design of op-amp based FinFET Circuits:
- \( I_D - V_G \) at other \( V_{DS} \) is normalized with template
- Optimizer is integrated with SEQUEL circuit simulator for automatic circuit design for given specification
- PSO algorithm mimics behavior of birds flocking in search of food and reported to be efficient in solving multimodal optimization problem

5. Impact of Process Variations Study:
- A LUT represents a device with a particular geometry
- Process variations study requires large number of LUTs
- LUT interpolation scheme is used to generate sufficiently large number of LUTs (41) from a small number of LUTs (5) for the process parameters: \( L, T_{FIN}, \) and \( EOT.\)
- LUTs generated at \( T = 27, 70 \) °C
- Variations in \( L, T_{FIN}, \) and \( EOT \) considered equal to \( \pm 2 \) nm, \( \pm 1 \) nm, and \( \pm 0.1 \) nm to generate LUTs at process corners
- \( V_{DD} \) variation is taken \( \pm 10 \% \) of 1 V
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References: