Infrastructure underpinning advanced nanoelectronics design

Tyndall team: Nicolas Cordero, Julie Donnelly, Jim Greer, Graeme Maxwell, Paul Roseingrave

Imec team: Thomas Chiarella, Jerome Mitard, Abdelkarim Mercha, Valentina Terzieva

Leti team: Olivier Faynot, David Holden, Gilles Reimbold

Funded by the European Union

Overview

- A changing business and design costs
- The problem statement
- ASCENT: the offering
- Where we are now
- Looking further ahead

Is that a supercomputer in your pocket?

"Today, your cell phone has more computer power than all of NASA back in 1969, when it placed two astronauts on the moon."
Michio Kaku, Physics of the Future:
How Science Will Shape Human Destiny and Our Daily Lives By the Year 2100

mobile phone
$200 - $800

~ 80 Billion operations per second

Memory: 2 Billion words

Power: 2 - 6 W

Weight: 150 grams

Makes phone calls

Cray - 1
$9,000,000

~ 160 Million operations per second

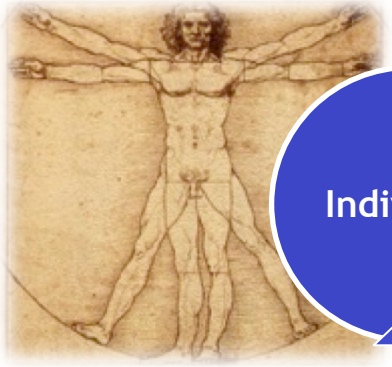
Memory: 1 Million words

Power: 115 kW

Weight: 5.5 tons

Doesn't make phone calls

The infrastructure is in place

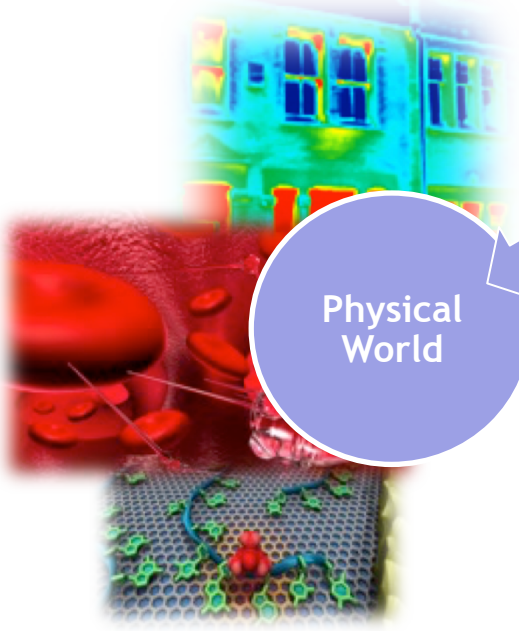


Individual

Smart Device

Physical World

Cloud



> 25,000,000,000 connected devices by 2020 (Gartner report) - or approx. 3 devices for every man, woman and child on earth

'Internet of Things'

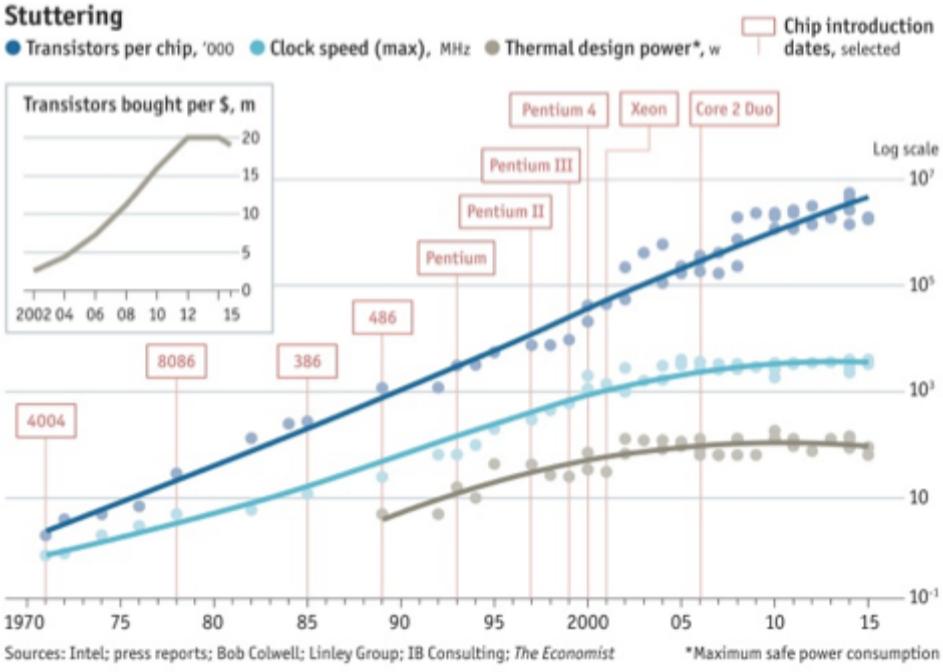
Funded by the European Union

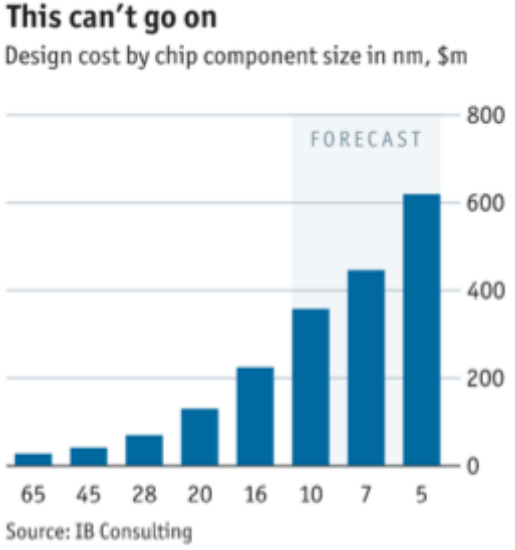
The Challenge

The Economist
Technology Quarterly
March 12, 2016

Cost/performance returns by scaling diminishing

Cost to achieve tape out on new nodes increasing



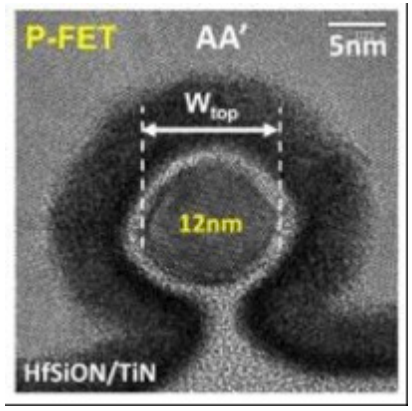


Funded by the European Union

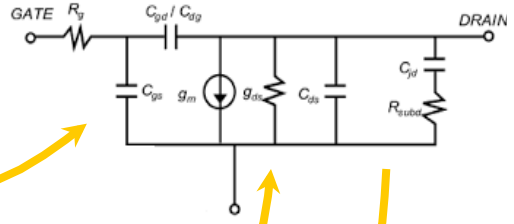
A part of the solution …

… an infrastructure for the **global** nanoelectronics modeling, characterization, and design communities

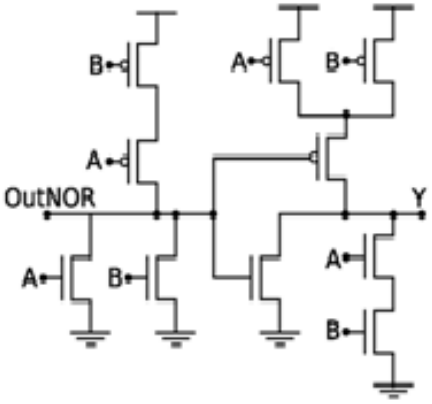
Process & Technology

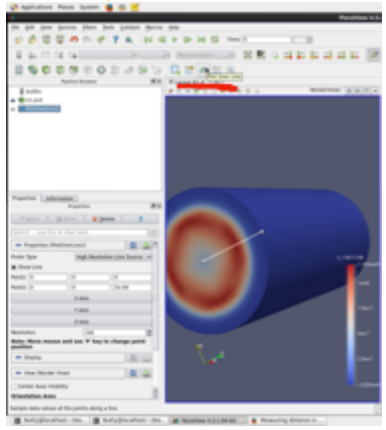


Compact Models



Circuit & System Design



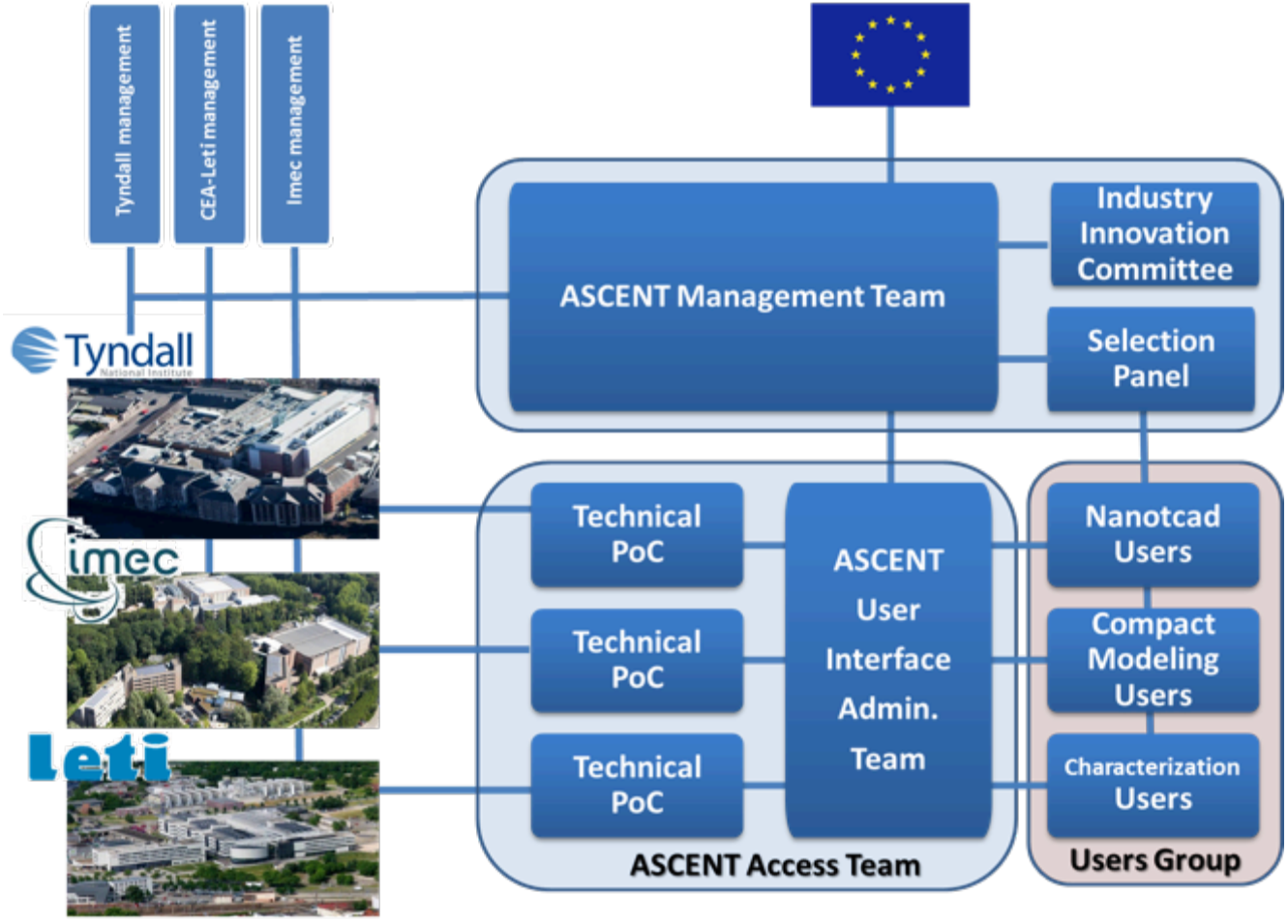


Technology Computer Aided Design

Funded by the European Union

The infrastructure

The combined resources of Tyndall, Imec and CEA-Leti nanofabrication capabilities and electrical characterization facilities integrated into a single research infrastructure present a truly unique opportunity



Funded by the European Union

Objectives

ASCENT will:

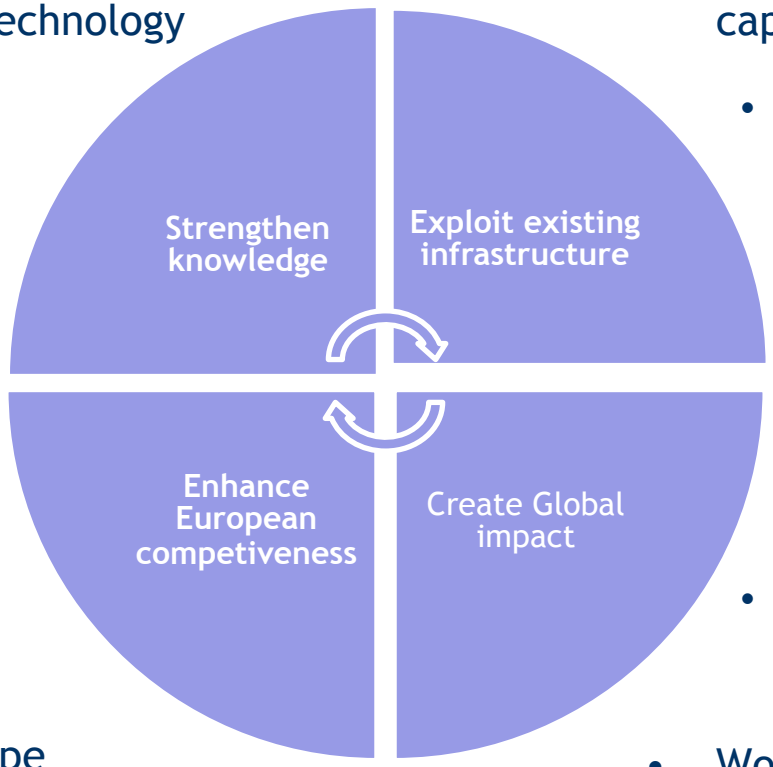
- **Leverage Europe's Unique advantage in nanofabrication to strengthen modeling and characterisation research community**
- **Accelerate development of advanced models at scales of 14nm and below**
- **Provide characterisation community with access to advanced test chips, flexible fabrication and advanced test and characterisation equipment**
- **Make project outputs available and easily accessible to nanoelectronics research community**

ASCENT offers simplified access
to
advanced technology and research infrastructure

Funded by the European Union

Impacts

- Enable researchers to realise innovative ideas at forefront of technology
- Benchmarking new developments against state-of-the-art technology



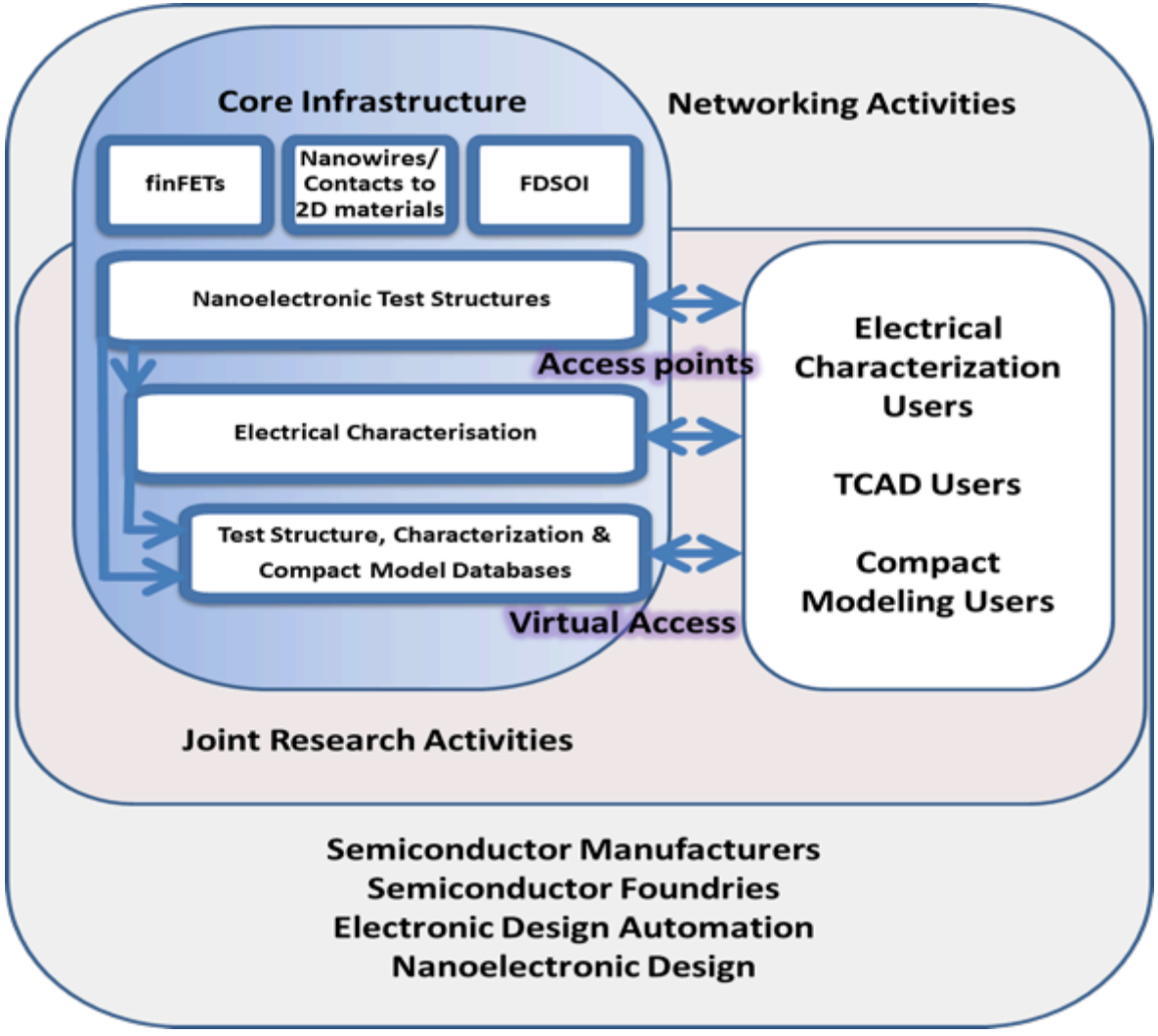
- Exploit over €2 billion capital investment
  - Assemble critical mass of people, knowledge and investment

- Anchor advanced modelling, design and manufacturing in Europe
- Enables delivery of first-mover advantage

- Ambition to maintain world leadership
- World-wide open door and dissemination policy

Funded by the European Union

ASCENT Network



Funded by the European Union

Committee Membership

Users Committee

- George Angelov
  - TU Sofia
- Asen Asenov
  - Uni Glasgow
- Olivier Faynot
  - CEA
- Francisco Gamiz
  - Uni Granada
- Benjamin Iñiguez
  - Uni Rovira i Virgili
- Andreas Schenk
  - ETH

Innovation Committee

- Bernie Capraro
  - Intel
- Patrick Drennan
  - Qualcomm
- Ronald Gull
  - Synopsys
- Dominique Thomas
  - ST Microelectronics

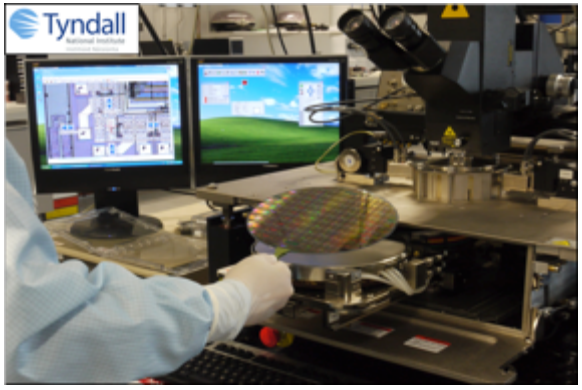
Funded by the European Union

The Access Providers

State-of-the-art 14 nm bulk FDSOI CMOS

Advanced transistor and interconnect test structures

Electrical & nano-characterization platforms



Fabrication facilities for nanowires & 2D materials

Advanced nanowire and nano- electrode test structures

Electrical & nano-characterization platforms

State-of-the-art 14 nm FinFET CMOS

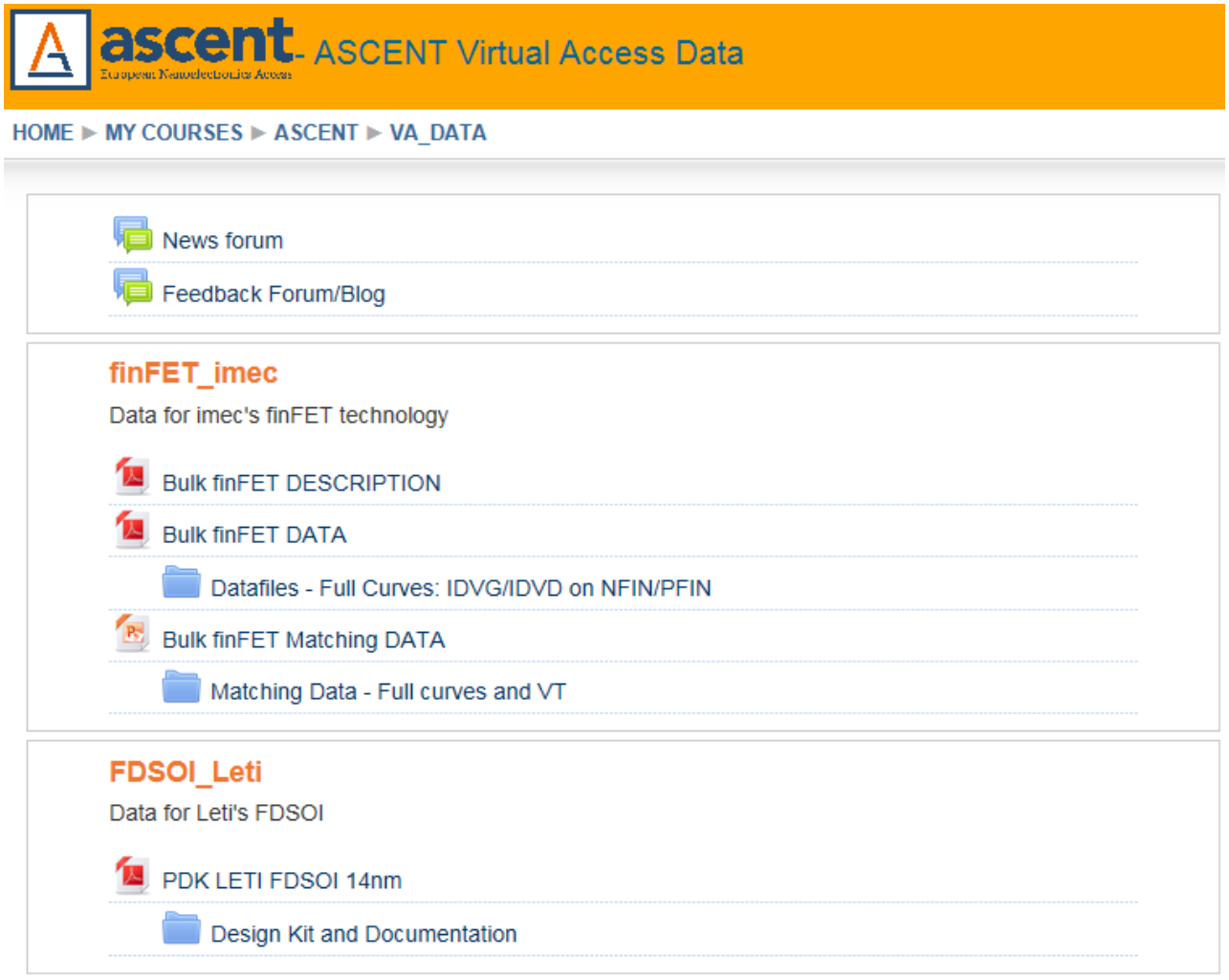
Advanced transistor and interconnect test structures

Electrical & nano-characterisation platforms

www.ascent.network

Funded by the European Union

Virtual Access (VA) Data



Funded by the European Union

Launched in November 2015

Sign up and find out more

149 registered users in 34 countries

50 project enquires

8 in discussion & review

16 projects supported to date

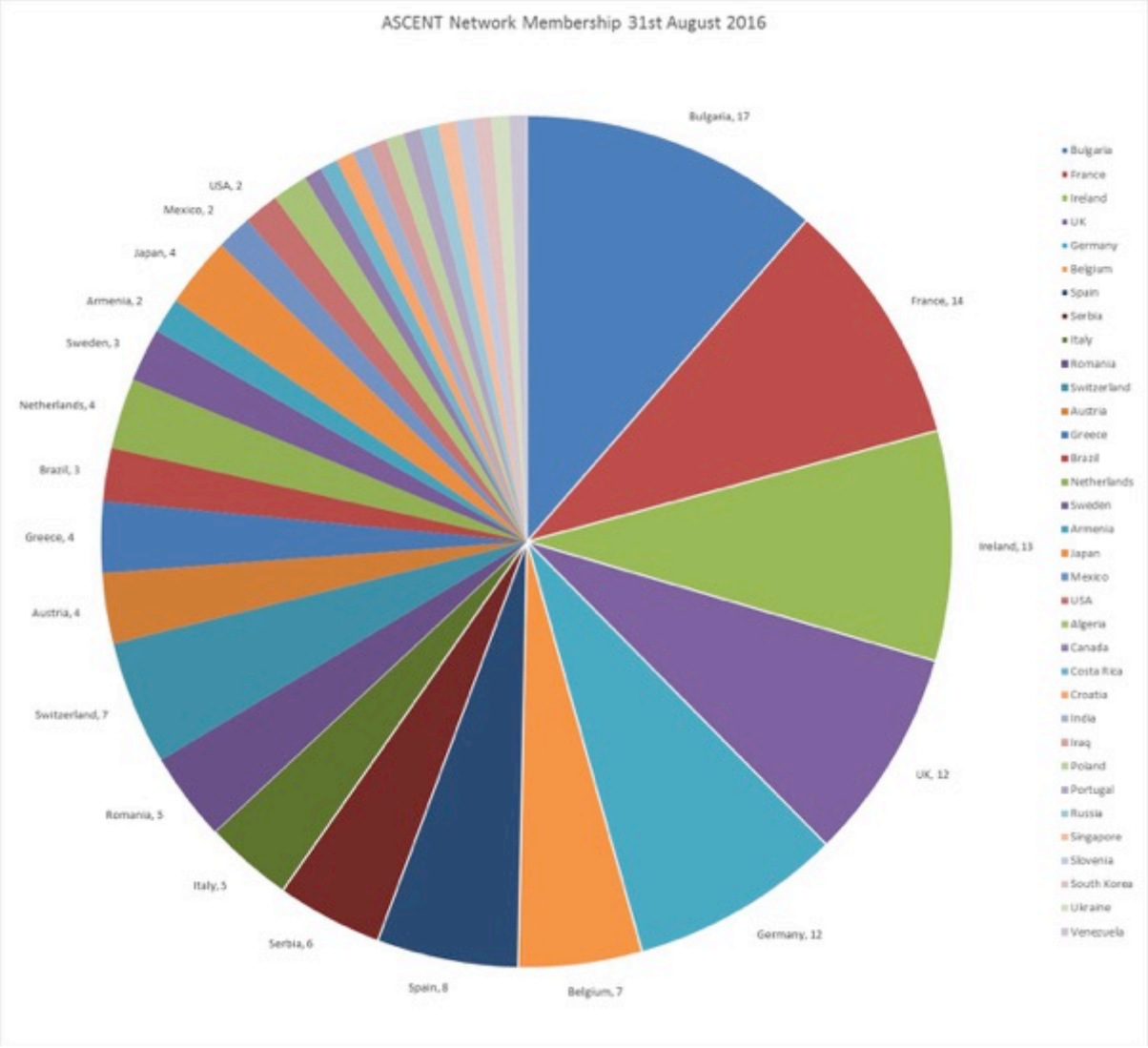
Sign up on-line

-or-

Fill out a card
We'll sign you up
login information will be sent to you

Funded by the European Union

149 members of ASCENT Network



Funded by the European Union

ascent
European Nanoelectronics Access

Easy Access!

Sign Up

- Free sign up as member
- Discuss with coordinator / technical POC

Apply

- Apply for access to data, chips or equipment
- Selection Panel decides on access

Access

- Access world-leading nanoelectronics technology
- Contribute to Joint Research Activities

Funded by the European Union

Tyndall National Institute

imec

cea leti

7 Transnational Access Projects

ASCENT Project-011 [Access to imec]

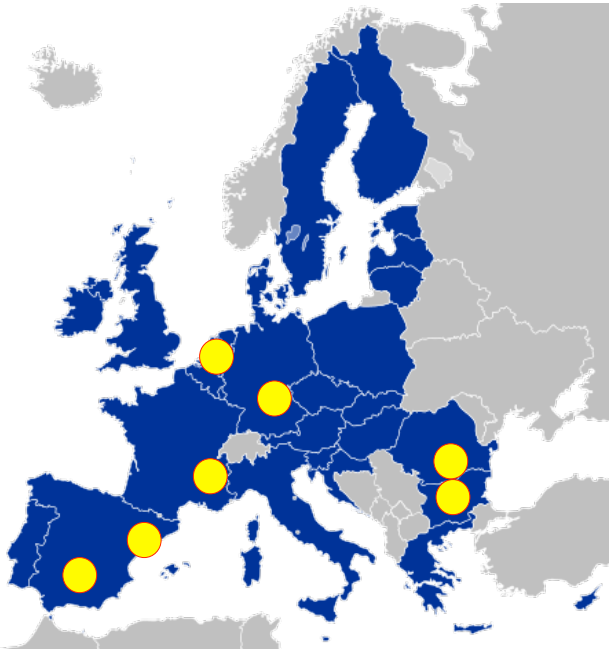
- Prof. Ghibaudo, IMEP Grenoble, France
- Wafers for parameter extraction/characterisation
- Facilities: Fully processed FinFET device wafers
- Effort/usage: 3 person.day

ASCENT Project-023 [Access to Tyndall]

- Prof. Dragoman, IMT Bucharest, Romania
- Thin/smooth metal deposition for MIM devices
- Facilities: Metal deposition + AFM
- Effort/usage: 11 person.day

ASCENT Project-029 [Access to Tyndall]

- Ling Ye, MESA, Univ. Twente, Netherlands
- Nanowires for monolayer doping
- Facilities: e-beam lithography, elec. Characterisation
- Effort/usage: 9 person.day



ASCENT Project-030 [Access to Tyndall]

- Prof. Miranda, Univ. Aut. Barcelona, Spain
- Characterisation of 2D MESFETs (high-k under electrical stress)
- Facilities: Electrical testing
- Effort/usage: 10 person.day

Funded by the European Union

7 Transnational Access Projects

ASCENT Project-034 [Access to Tyndall]

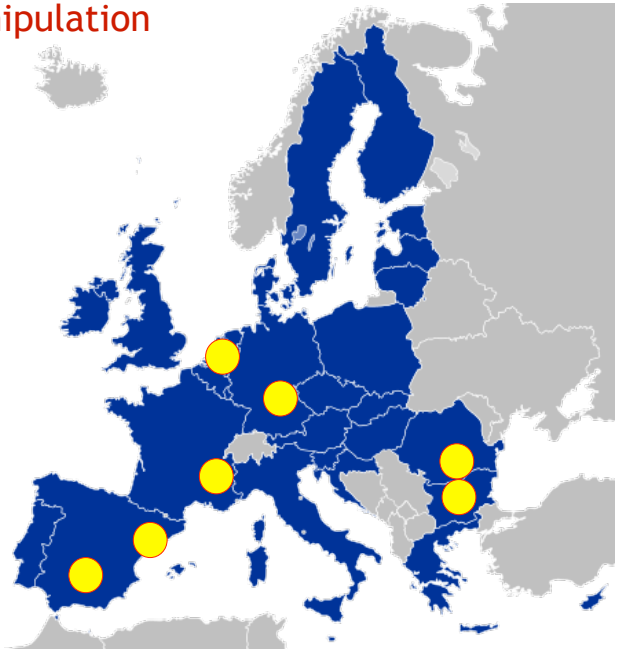
- Prof. Rusev, TU Sofia, Bulgaria
- Fabrication of acoustic tweezers for nanoparticle manipulation
- Facilities: Fabrication facilities
- Effort/usage: 9 person.day

ASCENT Project-042 [Access to Leti]

- Prof. Gamiz, University of Granada, Spain
- Simulation & characterization of SOI devices
- Facilities: Fully processed FDSOI wafers
- Effort/usage: 15 person.day

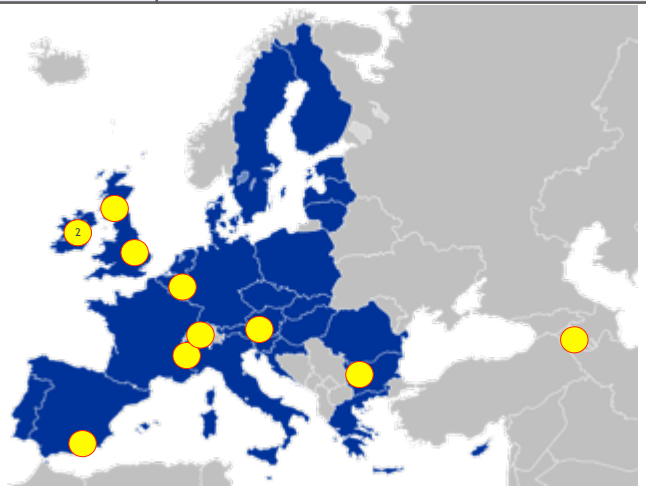
ASCENT Project-050 [Access to Leti]

- Peter Schüffelgen, Forschungszentrum Jülich
- TEM investigation of topological insulators
- Facilities: TEM
- Effort/usage: 10 person.day



11 Virtual Access Projects

Ref	User	Institute	Country
002	G. Angelov	Technical University of Sofia	Bulgaria
006	G. Fatin	University of Maynooth	Ireland
008	A. Durgaryan	Synopsys	Armenia
022	A. Nejadmalayeri	Phoelex Ltd (SME)	UK
031	X. Wang	University of Glasgow	UK
035	K. Miyaguchi	IMEC	Belgium
036	G. Ghibaudo	IMEP-LAHC/INPG	France
037	F. Gamiz	University of Granada	Spain
043	M. Karner	Global TCAD Solutions GmbH	Austria
045	T. Kelly	EOLAS Designs	Ireland
047	A. Pezzotta	EPFL ICLAB	Switzerland



Sample VA User Profiles

Researcher		Institute	Researchers topics/interests	What will you use the CMOS datasets for?
Dr X. Wang		University of Glasgow, UK	Nanoscale MOSFET devices, TCAD and atomistic modeling and numerical simulations Intrinsic parameter fluctuations due to statistical variability and reliability	Develop advanced MOSFET architecture and compact models Currently developing novel statistical compact models
Dr Gholamreza Zare		NUI Maynooth, Ireland	RFIC blocks for a transceiver targeting the next generation of the wireless communications systems High speed data converters, millimetre wave integrated circuits and phased array circuits	I was interested to be able to design with these advanced transistors (FDSOI and FinFET) and investigate their circuit characteristic. I am working on RFIC design and want to know their performance in this design field. This was the main reason to request for access. I am also interested in characterisation of these transistors (chips).
Dr Gerard Ghibaudo		IMEP-LaHC, Grenoble, France	Electronics transport, oxidation of silicon, MOS device physics, fluctuations and low frequency noise and dielectric reliability	Internal needs for PhD students and comparison to other technologies (FDSOI).
Prof. Francisco Gamiz		University of Granada, Spain	Numerical simulators of advanced semiconductor devices Implementation of new transport models, and scattering mechanisms	Calibration and tuning of semiconductor TCAD and home-made simulators.
Prof. George Angelov		Technical University of Sofia, Bulgaria	Device physics; bioelectronics; electrical engineering; multi-physics & control systems; electric vehicles and batteries; renewable energy sources systems; energy efficiency	Matching simulations based on compact models to experiment data.

Joint Research Activities

JRA1: Development of Device Forensic Techniques for<14nm CMOS devices

- Develop new techniques for device forensics of <14nm devices
- Provide data on contaminant impact on device fabrication for <14nm devices and highlight unacceptable materials.
- Recommend test vehicles to enable assessment of new material compatibilities.

JRA2: Standard e-test data and format for VA access

- Engage with user community to discuss and make available standard content for VA
- Work with partners to develop a standardised format for both FDSOI and FINFET technologies for the VA data

JRA3: Benchmarking of electrical characterization methods on new materials

- Develop new techniques for novel material and devices electrical characterization.
- Benchmark methods and results used on the 3 sites for a given set of wafers.
- Recommend most appropriate methods to be used for 5nm nodes and below

Fin shape evolution

	22nm	14/16nm	10nm	7nm
Channel length	25	22	19	16
Fin width	10	9	8	7
Fin height	34	42	~50	50+
Aspect ratio	3 : 1	5 : 1	6 : 1	7 : 1

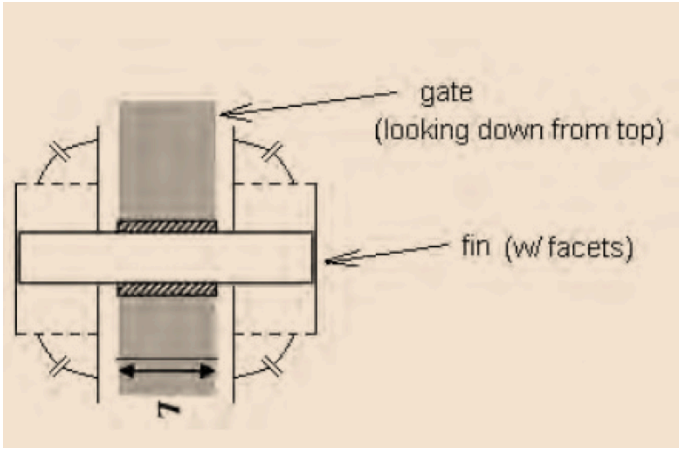
L/W ratio ~2.5

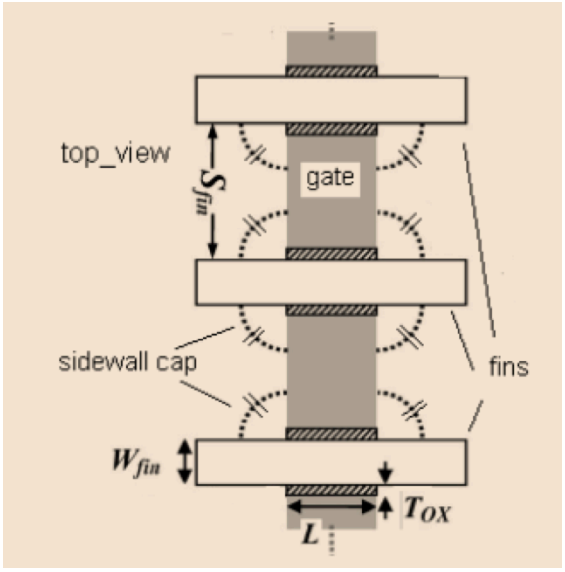
ISPD 2016, Santa Rosa, California

SYNOPSYS

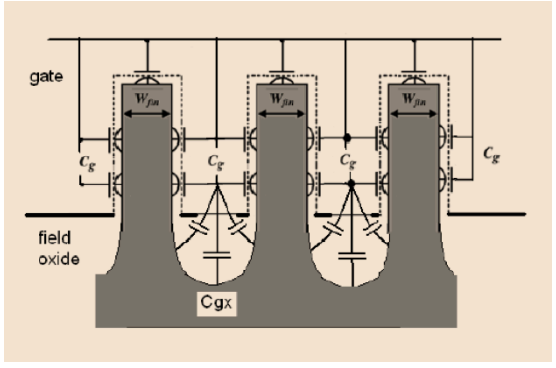
Funded by the European Union

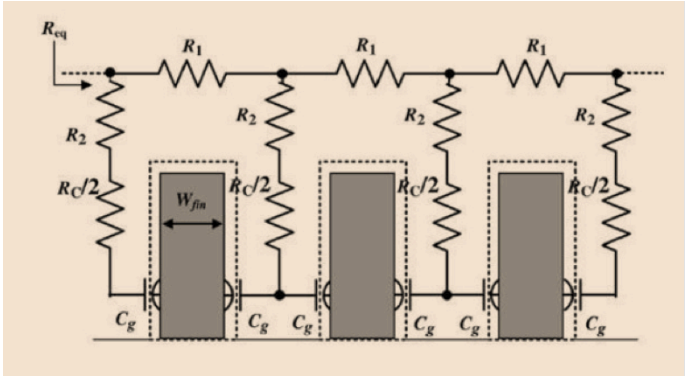
New challenges: parameter extraction





Gate to source/drain sidewall capacitance



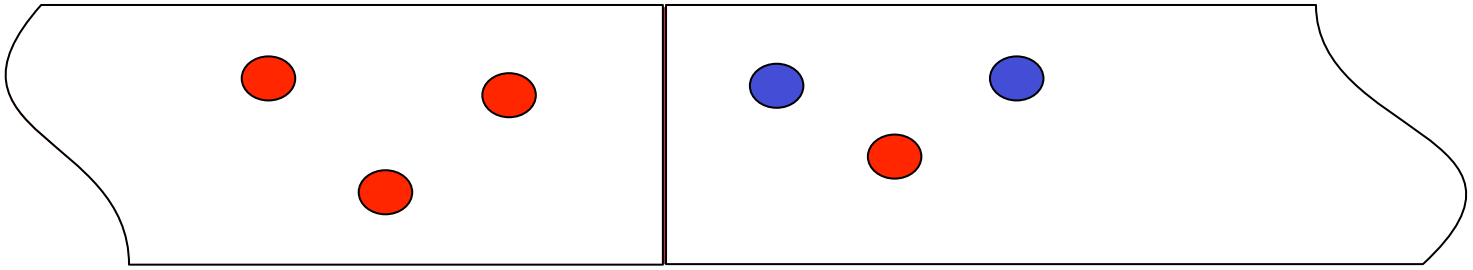


Gate access resistance

Funded by the European Union

Physical & materials obstacles

NW dimensions/ nm^3	Atoms/ nanowire volume	Atoms/ nanowire length	Dopant atoms/ nanowire
60x20x20	1,200,000	222	1200
30x10x10	150,000	111	150
15x5x5	18,750	55	?20
6x2x2	1,200	22	?1



p^+ n

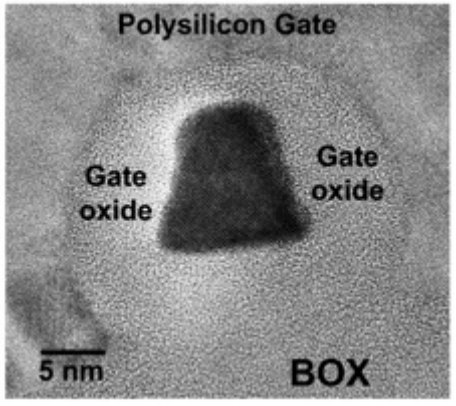
Funded by the European Union

Junctionless transistor

- ✓No junctions, no doping gradients
- ✓Gate lengths 50nm, 20 nm, 3 nm fabricated!

The cross-section of the channel needs to be small enough gate can entirely **deplete the heavily doped channel** to turn the device off

... and requires ***high doping concentration*** for good "current drive"



nature nanotechnology
ARTICLES
PUBLISHED ONLINE: 21 FEBRUARY 2010 | DOI: 10.1038/NNANO.2010.15

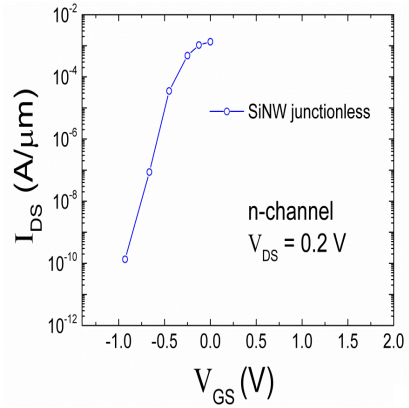
Nanowire transistors without junctions

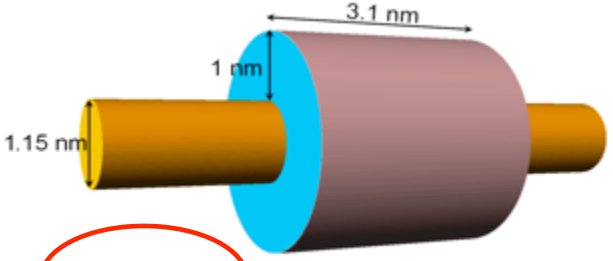
Jean-Pierre Colinge*, Chi-Woo Lee, Aryan Afzalian†, Nima Dehdashti Akhavan, Ran Yan, Isabelle Ferain, Pedram Razavi, Brendan O'Neill, Alan Blake, Mary White, Anne-Marie Kelleher, Brendan McCarthy and Richard Murphy

All existing transistors are based on the use of semiconductor junctions formed by introducing dopant atoms into the semiconductor material. As the distance between junctions in modern devices drops below 10 nm, extraordinarily high doping concentration gradients become necessary. Because of the laws of diffusion and the statistical nature of the distribution of the doping atoms, such junctions represent an increasingly difficult fabrication challenge for the semiconductor industry. Here, we propose and demonstrate a new type of transistor in which there are no junctions and no doping concentration gradients. These devices have full CMOS functionality and are made using silicon nanowires. They have near-ideal subthreshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage and temperature than classical transistors.

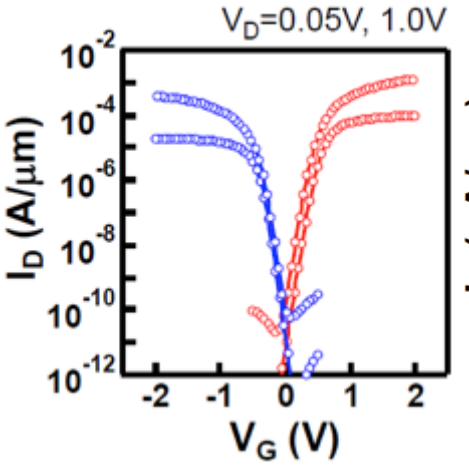
Funded by the European Union

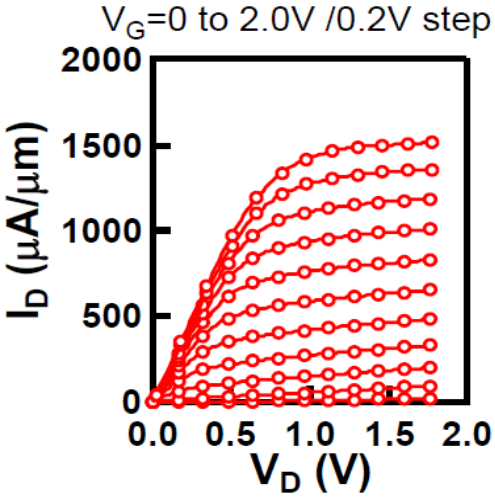
Accelerating simulation to validation

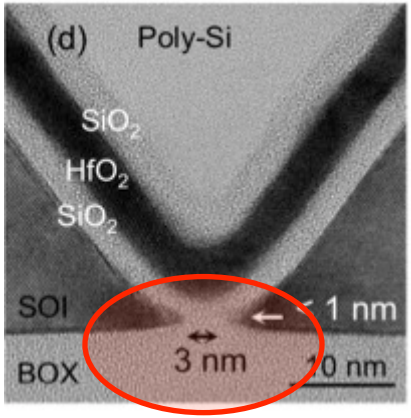


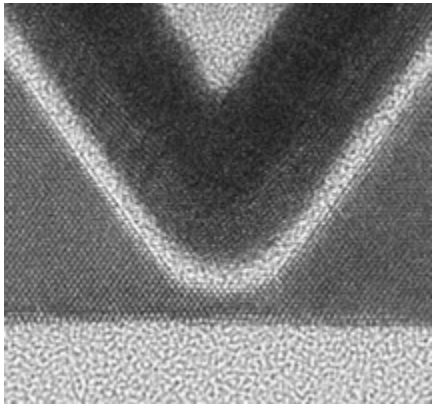


L. Ansari et al., Applied Physics Letters, **2010**
L. Ansari et al., Solid State Electronics, **2012**









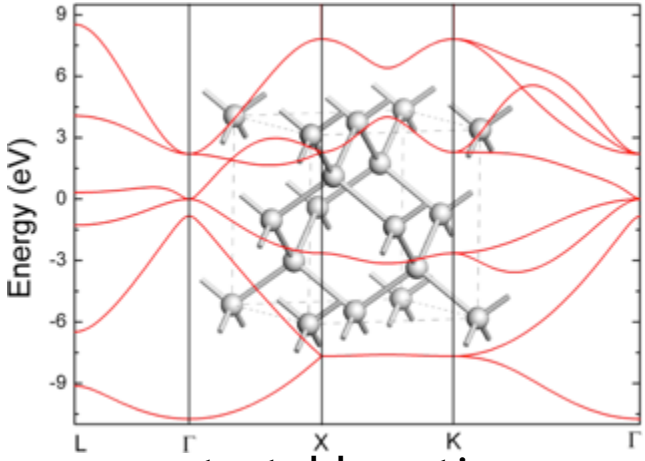
Fabrication and Demonstration of 3-nm-Channel-Length Junctionless Field-Effect Transistors on Silicon-on-Insulator Substrates Using Anisotropic Wet Etching and Lateral Diffusion of Dopants

Shinji Migita*, Yukinori Morita, Meishoku Masahara, and Hiroyuki Ota

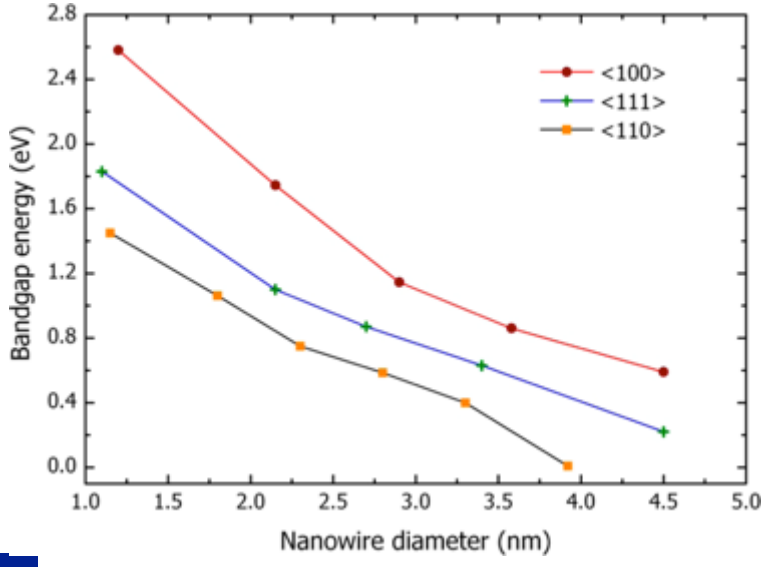
Japanese Journal of Applied Physics 52 (2013)

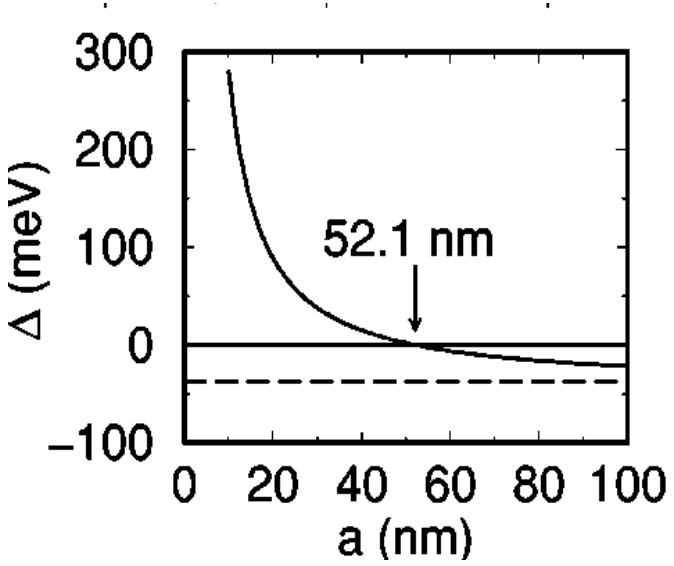
Funded by the European Union

Quantum alchemy: semimetal to semiconductor transition



metastable α-tin

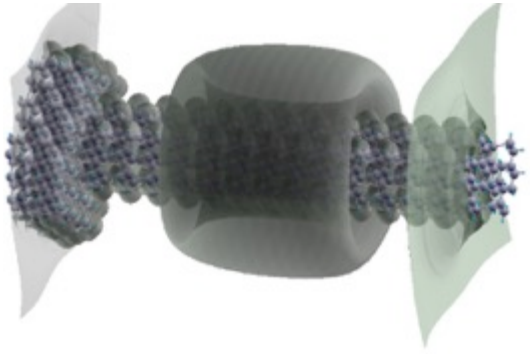


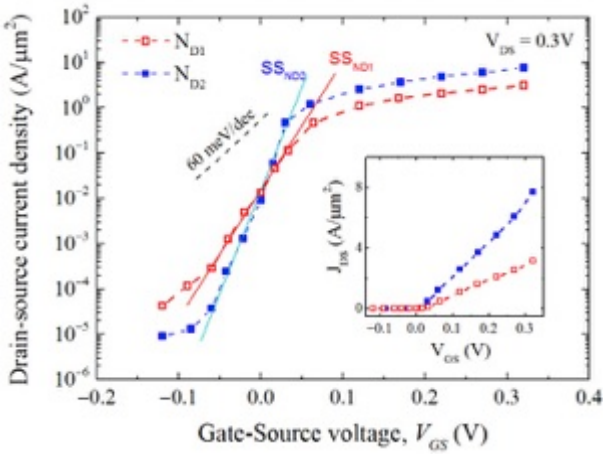


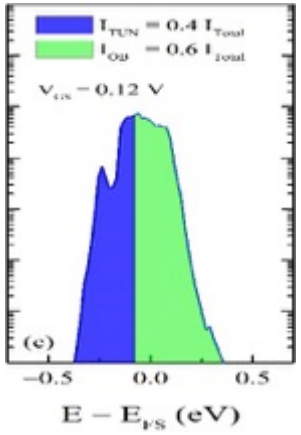
Theoretical description for bismuth:
Sin, Zhang, Dresselhaus,
Appl. Phys. Letters 1999

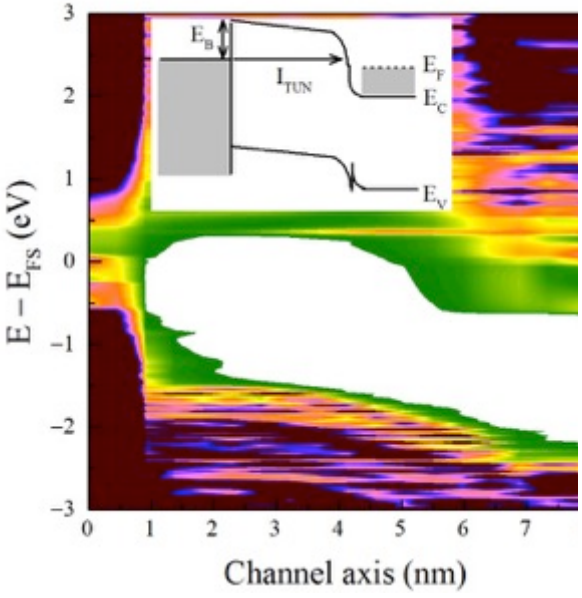
Instead of fighting quantum effects, can we make them work for us?

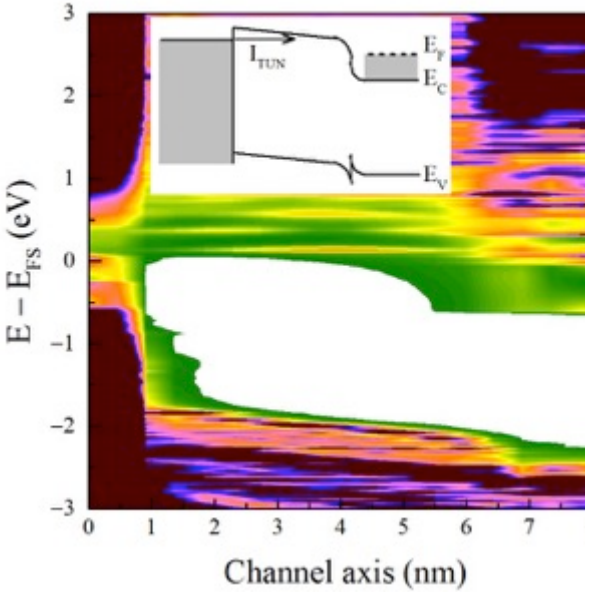
Overcoming Boltzmann's tyranny

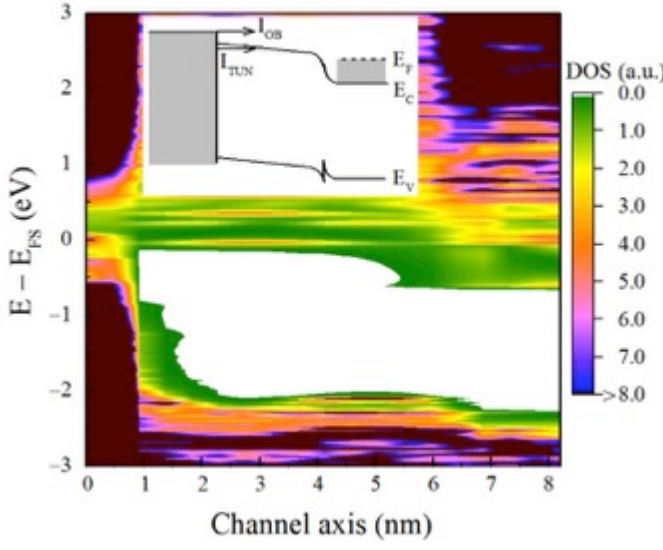






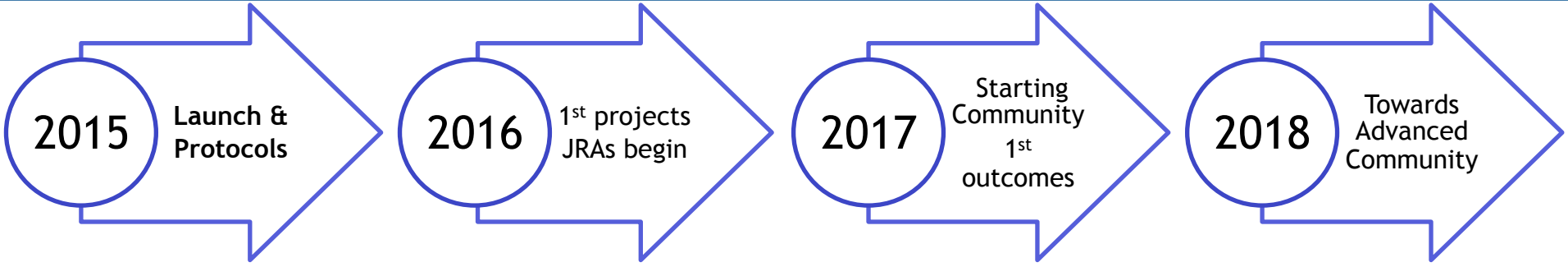






Funded by the European Union

ASCENT timeline



Explore an access proposal

- Advanced CMOS: 14 nm FinFET and planar FDSOI
- Nanowire & Novel devices
- Novel materials and processes

Open to commercial (ma & pop, SMEs, MNCs), RTOs, universities
Worldwide!

Costs for approved access projects covered

Funded by the European Union

Access Team will Support You

Overall Access Team Objectives:

- Define an easy access model for the User Community
- Generate data libraries, test-chips, equipment access capability
- Establish access route through single point of contact
- Establish & manage Selection Process – 1 week turn around!
- Provide logistical support for virtual and transnational access
- Analyse user profiles, requirements, outputs and impacts

Funded by the European Union

Next step

We will follow up with all registered attendees after the Workshop and invite you to sign up as members of ASCENT

www.ascent.network

or email

or phone

Paul Roseingrave: +353-21-2346168

and join with us in this exciting opportunity for nanoelectronics research

ascent
European Nanoelectronics Access

Thanks to teams at Imec, Leti, Tyndall

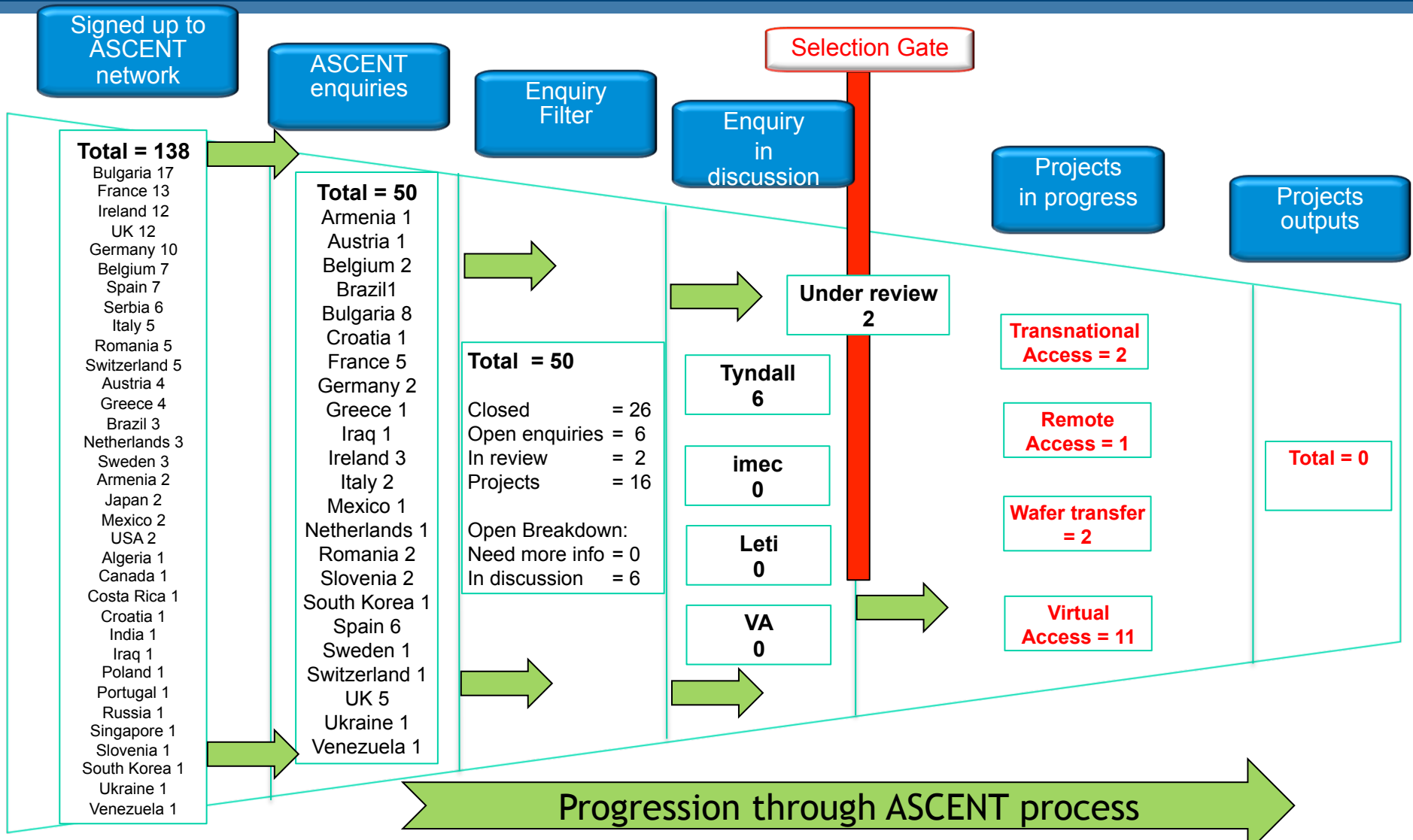
Funded by the European Union

Tyndall National Institute

imec

cea leti

Activity pipeline 29/07/16



Design & development challenges

- Structure generation and physical characterisation of test structures
- Ab initio simulation time: months
  - yet TCAD typically hours or overnight
- Electrical characterization and relate to device to device variability
- Capture new physics and device variability in compact models