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Optimal geometry selection for Hall sensors integrated in CMOS technological process

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Summary

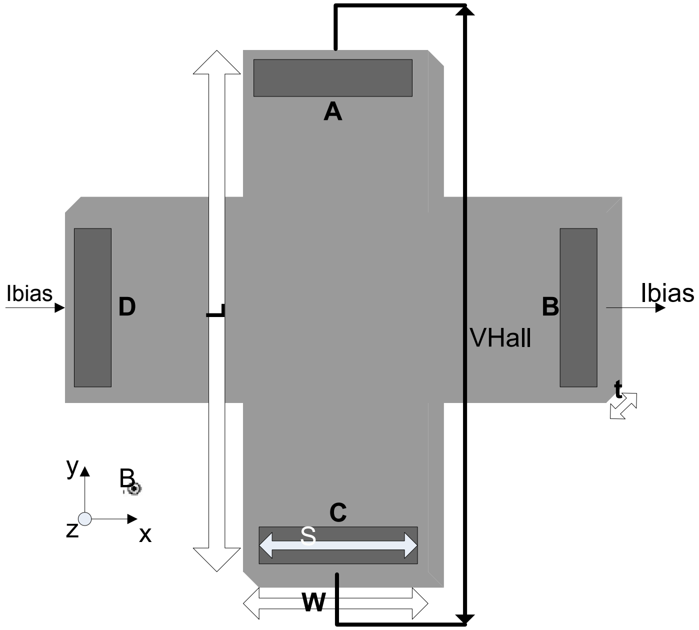
- Different Hall cells have been integrated in regular bulk CMOS technology (XFAB CMOS XH 0.35 µm) and analyzed in terms of their specific parameters.

- Geometry plays an important role in Hall cells performance. The focus of this work is on Basic and L Hall cells.

- Accurate single and multi-phase offset numerical estimations have been provided for the Basic Hall cell.

- The most important parameters of the Hall cells, based on regular bulk structure, are also evaluated through three-dimensional physical simulations.

Hall Effect Sensors



$$\boxed{V_{HALL} = S_A B} \quad (1)$$

$$\boxed{S_A = \frac{Gr_H}{nqt} I_{bias}} \quad (2)$$

- low-power applications
- current sensing
- position detection & contactless switching

Hall Cells Design Selection

- Different 3D Hall sensors were integrated in regular bulk CMOS technology.

- They are all symmetrical and orthogonal structures.

- The geometry plays an important role in the sensors performance.

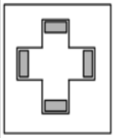
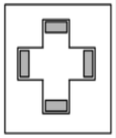
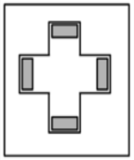
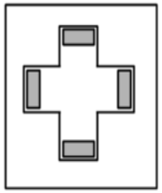
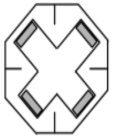
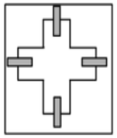
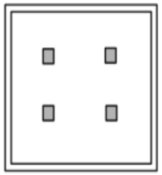
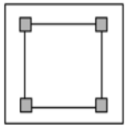
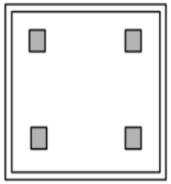
$$\boxed{G \cong 1 - \frac{16}{\pi^2}\exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\left[1 - \frac{8}{9}\exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\right]\left(1 - \frac{\theta_H^2}{3}\right)} \qquad (3)$$

valid if $0.85 \leq L/W < \infty$ and $0 \leq \theta_H \leq 0.45$

Hall Effect Sensors Measurements

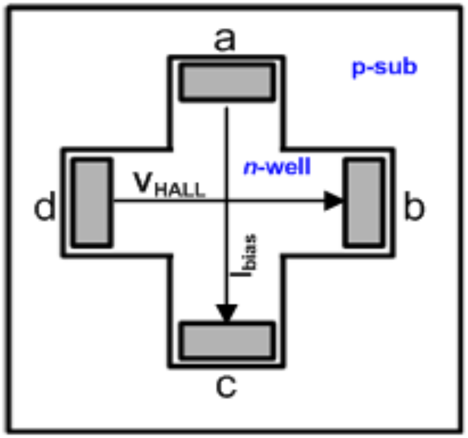
- Measurements results on nine different Hall Effect sensors in regular bulk CMOS

*Objectives: offset @*T=300 K **< ±30 μT** & *offset drift* < ±**0.3 μT/°C**

Geometry Type	*Basic*	*Low-doped*	*L*	*XL*	*45 Deg*	*Narrow Contacts*	*Borderless*	*Square*	*Optimum*
Integrated Shape (CMOS 0.35 μm)									
R_0(kΩ) @ T=300 K, B=0 T	2.3	5.6	2.2	2.2	2.1	2.5	1.3	4.9	1.5
S_A (V/T) @ I_{bias}=1 mA	0.0807	0.3392	0.0804	0.0806	0.0807	0.0822	0.0325	0.0884	0.0635
Offset drift (μT/°C) (4-phase current spinning)	0.409	0.067	0.264	0.039	0.373	0.344	0.526	0.082	0.328
L, *W* (μm) of the Active Area (N-well)	L=21.6	L=21.6	L=32.4	L=43.2	L=21.64	L=21.6	L=50	L=20	L=54
	W=11.8	W=11.8	W=17.8	W=22.6	W=11.8	W=9.5	W=50	W=20	W=54
L/W	1.83	1.83	1.82	1.91	1.83	2.27	1	1	1
s (μm) for Sensing Contacts	11	11	16	20.7	11	1.5	2.3	2.3	5.4
Geometrical Correction Factor (*G*)	0.913	0.913	0.912	0.924	0.913	0.87	0.76	0.73	0.74

Single Phase and Residual Offset

- Cell polarization and the corresponding phases



Greek-cross cell polarization

Phases	I_{bias}	V_{HALL}
Phase 1	a to c	b to d
Phase 2	d to b	a to c
Phase 3	c to a	d to b
Phase 4	b to d	c to a

- Single phase offset and residual offset

$$\boxed{V_{out} = V_{HALL}(B) + V_{offset}} \qquad (4)$$

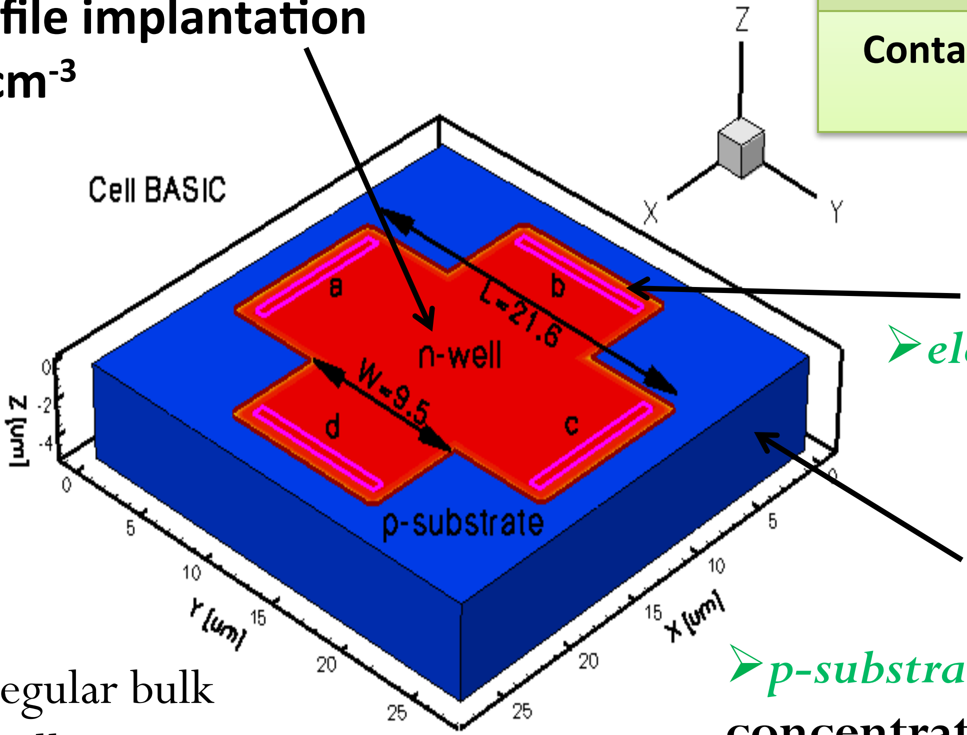
$$\boxed{Offset_{residual\ (4\,phase)} = \frac{V_{P1} - V_{P2} + V_{P3} - V_{P4}}{4}} \qquad (5)$$

The 3D Simulation of regular bulk Hall Cells

- **The Basic Hall structure follows the XFAB XH 0.35 fabrication process.**

Parameter	Value
L (µm)	21.6
W (µm)	9.5
Contacts dimension s (µm)	8.8

- ***active n-well region:*** **Arsenic doping**
  - ✓ **Gauss profile implantation**
  - ✓ **$1.5*10^{+17}$ cm^{-3}**



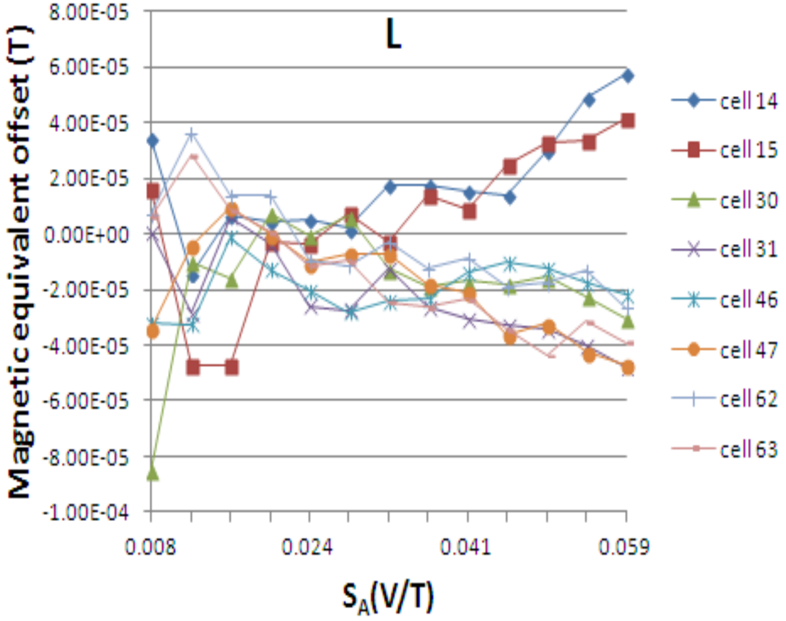
- *electrical contacts*

- *p-substrate:* **Boron doping concentration of 10^{+15} cm^{-3}**

The 3D model of regular bulk Basic Hall cell

Hall cells magnetic equivalent 2- and 4-phase offset

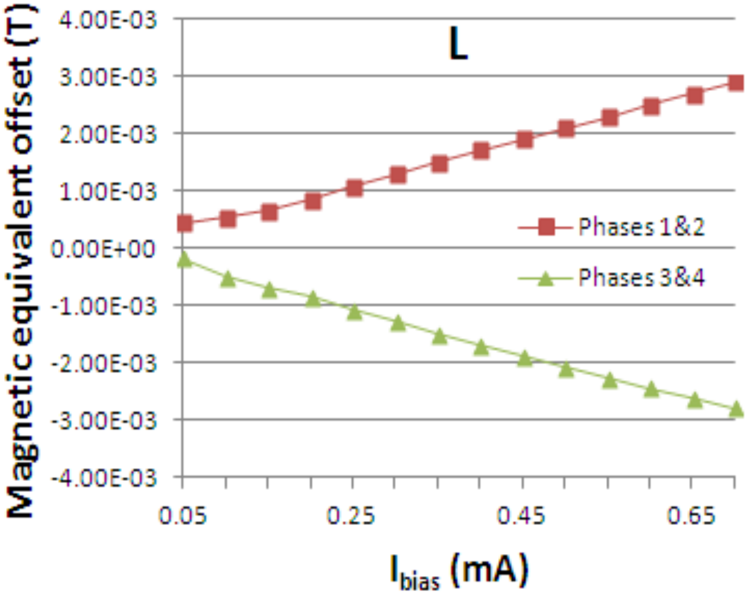
- DC setup was used again
- Each cell was tested 8 times on the chip
- Lowest offset level on XL cell



- DC setup was used

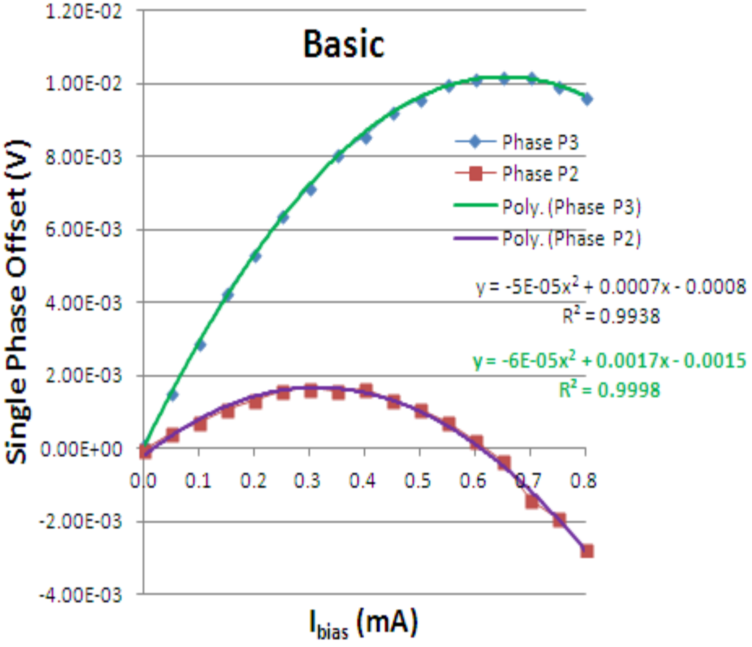
$$B_{offset,1\&2} = \frac{1}{100}\frac{V_{P1}+V_{P2}}{2}\frac{1}{S_A} \qquad (6)$$

$$B_{offset,3\&4} = \frac{1}{100}\frac{V_{P3}+V_{P4}}{2}\frac{1}{S_A} \qquad (7)$$



Offset measurements (I)

- Single phase offset was measured by an automated measurements setup
- Quadratic behaviour of the single phase offset with the biasing current was proven

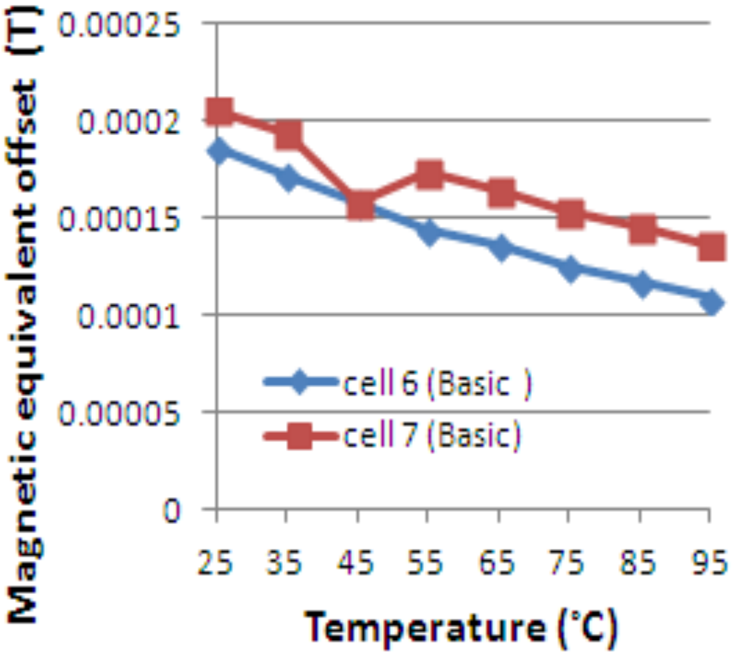


Measured single phase offset (V) versus I_{bias} for Basic Hall cell

Coefficients	Basic Cell	
	Phase P2	Phase P3
a (V/mA)	0.0007	0.00017
$b(V/m^2A^2)$	-5E-5	-6E-5
R^2	0.9938	0.9998

Offset measurements (II)

- Magnetic equivalent offset temperature variation was investigated
- Measured for Basic Hall cell in regular bulk CMOS



Measured magnetic equivalent offset (T) versus the temperature, for the Basic Hall cell

- Offset temperature drift is important.
- Temperatures from 25 to 95 °C were considered, by the means of a Temptronic oven.
- The same Basic cell was tested twice.

Averaged Offset Drift
for Basic Hall cell:
0.409 *$\mu T/$ °C*

Conclusions

- This work was intended to analyze the behaviour of Hall cells in regular bulk CMOS fabrication process.
- Different offset numerical estimations (single phase, multi phase offset voltage, residual offset, magnetic equivalent offset, post-encapsulation offset) were investigated.
- Special attention was given to prove the quadratic behaviour of the offset with the biasing current.
- The variation of the magnetic equivalent offset with the temperature was also performed for the CMOS Basic Hall cell, for a 25 to 95 °C range.

References (selective list)

***[1]* Paun, M.A**, Udrea, F., *"SOI Hall cells design selection using three dimensional physical simulations",* Journal of Magnetism and Magnetic Materials, Volume 372, Issue 12, December 2014, pp. 141-146.

***[2]* Paun, M.A.**, Sallese, J.M., Kayal, M.*, "Evaluation of characteristic parameters for high performance Hall cells",* Microelectronics Journal, Volume 45, Issue 9, September 2014, pp. 1194-1201.

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***[4]* Paun, M.A.**, Sallese, J.M., Kayal, M.*, "Offset and drift analysis of the Hall Effect sensors. The geometrical parameters influence"*, Digest Journal of Nanomaterials and Biostructures (DJNB), vol. 7, pp. 883-891, 2012.

***[5]* Paun M.A.**, *Hall Cells Offset Analysis and Modeling Approaches*, PhD Thesis, EPFL, Switzerland, 2013.

Thank you for your

kind attention!