Unified charge-based Transistor Model including Degradation Mechanisms

MOS-AK Workshop

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Lausanne - March 2017
Motivation

Specifications: Lifetime, Gain, Latency, ...

Process: Doping, Dimensions, Materials, ...

Overview

Process Variation

Physics → Transistor → Circuit → System

Specifications

Voltage, Temperature, Age
Transistor Degradation

Transistor Model

1. $V_{th}$
2. $Q_i$
3. $\Phi_s$

Influences

- Process
- Temperature
- Voltage
- Age

Consideration

- Monte Carlo
- SPICE
- RelXpert

Conclusions drawn?

No propagation of interdependencies within modeling
FEOL Aging Mechanisms

**Hot Carrier Injection**

**Bias Temperature Instability**

\[ \tau = 10^{-12} \ldots 10^8 \text{ s} \]

**Different Stress Conditions**

**Inverter**

\[ Q_i = Q_0(P,V,T) + Q_{age}(t) \]

**Transistor Aging Models**

\[ V_{th} \text{ BSIM4:} \]

\[ V_{th} = V_{TH0} + \left( K_{ox} \cdot \sqrt{\Phi_i - V_{th}} - K_1 \cdot \sqrt{\Phi_i} \right) \sqrt{1 + \frac{L_{PEB}}{L_{eff}}} - K_{2ox} \cdot V_{th} \]

\[ + K_{1ox} \left( \sqrt{1 + \frac{L_{PE0}}{L_{eff}}} - 1 \right) \sqrt{\Phi_i + \left( K_3 + K_3B \cdot V_{th} \right)} \cdot \frac{TOXE}{W_{eff}} \cdot \frac{W_0}{\Phi_i} \]

\[ - 0.5 \cdot \left( \frac{DVT0W}{\cosh\left(\frac{DVT1W \cdot \frac{L_{eff}}{L_{ox}}}{L_{ox}} - 1 \right)} + \frac{DVT0}{\cosh\left(\frac{DVT1 \cdot \frac{L_{eff}}{L_{ox}}}{L_{ox}} - 1 \right)} \right) \cdot \left( V_{bi} - \Phi_i \right) \]

\[ - \frac{0.5}{\cosh\left(\frac{D\cdot SUB}{2} - 1 \right)} \cdot \left( ETA0 + ETAB \cdot V_{th} \right) \cdot V_{ds} - n_v \cdot \ln \left( \frac{L_{eff}}{L_{eff} + DVTP0 \cdot \left( 1 + e^{-DVTP1 \cdot V_{ds}} \right)} \right) \]

\[ - \left( DVT1 + DVT2 \cdot \frac{L_{eff}}{L_{eff}} \right) \cdot \cosh\left(DVT3 \cdot V_{ds} \right) \]

\[ Q_{age}(t) = C_{age} \cdot \Delta V_{th} \]

- Unclear age-dependencies
- Unwanted interferences

- Standard
- Non-Uniform Doping
- Pocket Implant
- SCE
- DIBL
- DITS
- Narrow Width

Hillebrand et al. Charge-based stochastic aging analysis of CMOS circuits. IIRW 2015
Threshold Voltage Measurement

- **Lin.** and **Sat.**
- Mean of $V_{th}$ in V
- Variability of $V_{th}$
- Length 50, 600 units
- Method 1, 6

**Table**

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**Graphs**

- Mean of $V_{th}$ in V
- Variability of $V_{th}$
- Length 50, 600 units
- Method 1, 6

Without knowledge of method and region, $\Delta V_{th}$ can be misleading.
Charge Based Aging Model

- Charge based model
- EKV, BSIM6
- PVTA within Model
- Verilog-A

Shift of $V_{th}$: Consequence not Cause

$$Q_i = -\gamma' \cdot C_{ox} \cdot \sqrt{V_t} \left[ \sqrt{\frac{\psi_S}{V_t}} + e^\frac{\psi_{g'-2\phi_F-V_{th}}}{V_t} \right] - Q_{age}(t)$$

- Shift of parameters are calculated within the transistor model
- No need for additional simulation environment
Overview

Process Variation

Physics → Transistor → Circuit → System

Voltage, Temperature, Age

Specifications

4/4/2017
Circuit Design Method

$g_m/I_D$ - Method

- Operation Mode
  \[ IC = \frac{l_D}{l_0 \frac{W}{L}} \]
- Speed / Area
  \[ L \]
- Power / Speed
  \[ I_D \]

Hillebrand et al. Design and Verification of Analog CMOS Circuits Using the gm/ID-Method with Age-Dependent Degradation Effects, VARI 2016
Miller OTA

- Input needs bias
- Biasing circuit must be taken into account for PVTA investigation

Expensive Redesign

**System**
- Constraints
- Specification

**Circuit**
- Topology
- Requirements

**Transistor**
- Dimensions
- Feasibility
Beta Multiplier: Reference Voltage

PTA influences on circuit level resulting in voltage change on system level.

Divide and Conquer for PVTA

Hillebrand et.al. Online Monitoring of NBTI and HCD in Beta-Multiplier Circuits, IOLTS 2016
Overview

Process Variation

Physics → Transistor

Circuit

System

Specifications

Voltage, Temperature, Age
PVTA Interdependencies

- Time dependent distribution function
  - transistor-, circuit and/or system performances
- Full PVTA at once
- Enables sophisticated system analysis

Time dependent distribution function

\[ B(t, x) = \frac{(\beta_k t^k + \gamma_k)(\beta_c t^c + \gamma_c)}{\beta_\alpha t^\alpha + \gamma_\alpha} \left( \frac{x}{\beta_\alpha t^\alpha + \gamma_\alpha} \right)^{\beta_c t^c + \gamma_c - 1} \]

Hillebrand et.al. Stochastic analysis of degradation and variations in CMOS-Transistors, ZUE 2015
Charge Based Stochastic CMOS Design

Test Bench for N-, PMOS

- \( W, L \)
- Temp. \( Vdd, Vgs, Vds \)
- Process degradation

Equations for Circuit Performance

\[
z = \frac{x}{y} \quad \Rightarrow \quad \sigma_z/\mu_z = \frac{\sigma_x}{\sigma_y} \Rightarrow f(x, y)
\]

\[
f_X(x) = \int_0^\infty \frac{y}{2\pi\sigma_x\sigma_y\sqrt{1-r^2}} \exp \left[ -\frac{1}{2(1-r^2)} \left( \frac{y^2z^2}{\sigma_x^2} \right) \right] dy
\]

Pdf of transconductance

Sampled distribution functions, e.g.

\[
IC = \frac{l_D}{l_0 W/L} \quad \frac{g_m}{l_D}
\]

Hillebrand et.al. Stochastic LUT-based Reliability-Aware Design Method for Operation Point Dependent CMOS Circuits MIXDES 2016

Hellwege et.al. An Aging-Aware Transistor Sizing Tool Regarding BTI and HCD Degradation Modes, MIXDES 2015
Summary

Unified Transistor Model

- Charge-based
- No $V_{th}$
- PVTA

Metrics

- Consistent Environment
- Combination of analyses

Circuit

- No extrapolation
- Arbitrary mission profile