ON Semiconductor

Modeling and Analysis of Full-Chip Parasitic Substrate Currents

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Outline

• Objectives
• Challenges
• SPX solver
• Solutions
  ◦ Compact Modeling (ONSEMI)
  ◦ Quasi-neutral Region Model: 1D case
  ◦ The AUTOMICS Approach (EPFL/MC univ)
  ◦ TCAD-inspired (MAGWEL)
• **Latch-up is a prominent risk in HV processes**
  – The methodology prescribes passing LU tests
  – Today only empirical guidelines and DRC rules are available to help designers reduce this risk

• **Parasitic bipolars challenge the isolation**
  – High-impedance nodes pick-up unwanted signals
  – The traditional approach with parasitic BJT models fails (“layout dependency of the $\beta$ gain”)

• **There is a need for a layout-based tool simulating carrier transport at full-chip level**
Typical smart-power IC contains 100+ pockets
- and 10+ power domains
- Standard TCAD tools require
- sub-μm meshing (~ 10nm) and can not
- cope with chip complexity and dimensions
- Simulation of carrier transport effects at the full-chip level requires simplifications:

- Apply a divide and conquer approach (sub-domains)
- Replace the (TCAD) equations set to be solved by simplified and compact versions (approximations)
The current gain “β” is not invariant
• with respect to “boundary conditions”
  – Consider two N-type tubs on a P substrate
  – Bias one as an injector, the other as a collector
  – The current gain varies depending on the presence of additional collectors
• **Target usage:**
  - Find weak spots for LU or parasitic BJT coupling
  - Let the designer home-in and solve them
  - Interaction of circuit and substrate to be simulated

• **Modalities:**
  - Co-simulation: too complex and slow → excluded!
  - Annotation of schematics with substrate models

• **Need for a new multi-terminal model for carrier transport in the substrate...**
  - The substrate is inherently multi-emitter/collector
  - and **can not be reduced** to simple BJT models
• Introduce dual-carrier ports allowing to:
  – *Split the chip in quasi-neutral regions*
  – *Handle depletion regions as boundary conditions*
  – *Reconstruct an abstract model of the substrate with carrier transport in the circuit simulator*
Solutions : 2 Reduced Equations Set

Full Set for Carrier Transport in a Semiconductor

\[ \vec{E} = -\nabla V \quad \text{\{ electric \}} \]
\[ \epsilon_{Si} \nabla \cdot \vec{E} = q(p - n - N_A + N_D) \]
\[ \vec{J}_n = q \mu_n n \vec{E} + q D_n \nabla n \]
\[ \vec{J}_p = q \mu_p p \vec{E} - q D_p \nabla p \]

\[ \partial_t n - \frac{1}{q} \nabla \cdot \vec{J}_n = -R(p, n) \]
\[ \partial_t p + \frac{1}{q} \nabla \cdot \vec{J}_p = -R(p, n) \]

- Coupled system of equations
- Iterative solution strategy
- Junctions simulated in detail

Simplified Set for Quasi-Neutral Regions

\[ \vec{E} = -\nabla V \quad \text{\{ electric \}} \]
\[ \epsilon_{Si} \nabla \cdot \vec{E} = 0 \]
\[ \vec{J}_n = q \mu_n n \vec{E} + q D_n \nabla n \]
\[ \vec{J}_p = q \mu_p p \vec{E} - q D_p \nabla p \]

\[ \frac{1}{q} \nabla \cdot \vec{J}_n = R(p, n) \]
\[ \frac{1}{q} \nabla \cdot \vec{J}_p = -R(p, n) \]

- Depletion regions domain
- Steady-state only
- Solution in single forward pass (Decoupled' system)
- Junctions are boundary conditions
Basic QNR resistor
- Zero applied E-field
- Canonical solution of
- the 1D equations:
  \[ \delta n = \delta p = A_{\pm} \exp(\pm x/L_{DA}) \]
- Any solution is a linear combination of
- Quasi-Fermi level differences
- \( \rightarrow \) total excess carrier densities at the ports
- Excess profiles for electron and holes coincide
- An internal electric field equalizes the gradients
- (“ambipolar” diffusion) \( \rightarrow \) \( J_n \) and \( J_p \) are exactly opposite
• As the base of a BJT
  – $A_+$ is positive
  – $A_-$ is negative

  $n(x_2) = 0$
  $\delta n(x_2) = -n_0$

  – A small electric field must compensate the majority diffusion currents at the edges of the depletion regions
Applications of the QNR Resistor Model

- For P/N diodes (*)
- For arbitrary structures:
  - Crossing makes a junction straight for same type
  - Possibility to mesh using 1D elements

(*) models valid in moderate till the onset of high injection
Generalization to the Multi-port Case

- **Key principles:**
  - Use linear combinations of “diode-mode” solutions
  - Characterize diode modes using transfer coefficients
    \[ \alpha_{ij} = \frac{\delta n_i}{\delta n_j} \quad J_n(P_i) = J_p(P_i) = 0 \]
  - Build carrier-balance equations to determine \( A_j \)

\[
F(U_{Fn}(P_i) - U_{Fp}(P_i)) = \sum_j \alpha_{ij} A_j
\]

- Diffusion currents
  \[ J_{diff} = \pm qD \frac{d\delta c}{dz} = \pm qD \delta c \frac{(P_i)}{L_{DA}} \quad c = p, n \]

- Drift currents
  \[ J_{drift}(i) = \sum_j Y_{ij} (V_j - V_{Dmbj}) \]
Basic Claim of the QNR Mesh Model

- The complete carrier transport behavior of a multi-terminal bipolar can be reconstructed from “diode-mode” characteristics only!

Diode-mode characterization

Bipolar-mode operation
MAGWEL’s SPX Solver - TCAD inspired

• Simulation Flow
  • Geometry from GDS
  • Layers in tech file
  • 3D structure with substrate and ports
  • DOE for DC bias
  • Analyze distributions
    – Quasi-Fermi level
    – Densities
    – Current, ...

• Solver’s Strategy
  • Solve for equilibrium
  • Solve Poisson field
  • only one(!) per bias
  • Replace junctions by boundary conditions
  • Solve minority flow
  • Solver majority flow
  • Check solution quality
  • Typically 3 mins per bias point
  • Sweeping all diodes in 24 hours
Top view of the structure

- **E1**: 0 to -2 V
- **C2**: 10 V
- **C3**: Floating
- **C4**: Floating
- **P-taps**: 0 V

Distance: 57 µm
Some mesh details (SPX)
Excess electron density

Z = 310 μ

Z = 320 μ

Z = 330 μ

y is constant and x through center E1 and C2
Excess electron density

boxGenerationRate: 0 Step: 4
y=2900

y is constant and x through center C3 and C4
Severe meshing demands!
Pioneered at EPFL, tested at AMS and STM

Commercialized by PN Solutions (spin-off P&M Curie /EPFL)

A 3D mesh of “QNR resistors”

- One wire for “total current”
- One wire for “minority carriers gradient”

Models junctions, dynamic effects, breakdown

Drawback: 3D mesh solved in circuit simulator
• Ports with wires for carrier densities and electric potential
• Carrier transport in the substrate modeled by fitting functions to TCAD simulations
• VerilogA model computes distribution of carriers
• Drawback: standard TCAD solver not optimized for QNR
Validating the QNR Mesh “Claim”

- I3T80 test-chip
- 4x 70x70μm² pockets
- + 1 long subs. contact
- Diode-mode biasing:
  - One pocket biased negatively wrt to substrate
  - Other pockets floating
  - (zero total current)
- Bipolar operation:
  - Single collectors
  - Multiple collectors
  - Multiple emitters
• Several QNRRes instances for the pockets
• One QNRMesh instance for the substrate
• Comparison of floating pocket voltages
• Model ’s extracted from SPX simulations
Model Validation: Bipolar Mode

• Comparing SPX and circuit model to measured data
  – 1 emitter, 3 collectors, model extracted from diode mode, no fitting
  – Residues are the errors in measured and SPX simulated balances
Model Validation: More Bipolar Mode

- Comparing SPX and circuit model to measured data
  - 1 emitter, 3 collectors, model extracted from diode mode, no fitting
Implications of the QNR Mesh Results

• Diode-mode characterization:
  – Linear in the number of ports:
  – Sweep one diode and collect ‘s
  – *(no need to measure interactions)*
  – Faster n-port characterization with FEM tool

• Carrier injection efficiencies:
  – Find risky aggressor – victim pairs by inspection
  – for high-injection effects
Summary

• Modeling is done as:
  – Substrate block acts as a transport vehicle for carriers
    ▪ Resistive network
    ▪ Mesh-based network (SPX)
  – Carriers are injected and collected with compact-model models representing biased pockets
    ▪ Analytic compact models
    ▪ Numerical compact models (SPX)
Conclusions

• The **dual-carrier framework** and the **superposition of diode-mode solutions** are proven to work well for building substrate models.

• A 2-port model and a **multi-port generalization** were generated and validated.

• **EEPO (OnSemi)** is building a complete flow based on FEM calibration of compact substrate models.

• Future work:
  – Scaling to more than 1000 ports (multi-pole methods)
  – AC and transient behavior
  – More physical collector models (velocity saturation)
Time for Questions!