On the modelisation of the main characteristics of SOI Hall cells by three-dimensional physical simulations

Maria-Alexandra PAUN, *PhD*

Visiting Researcher

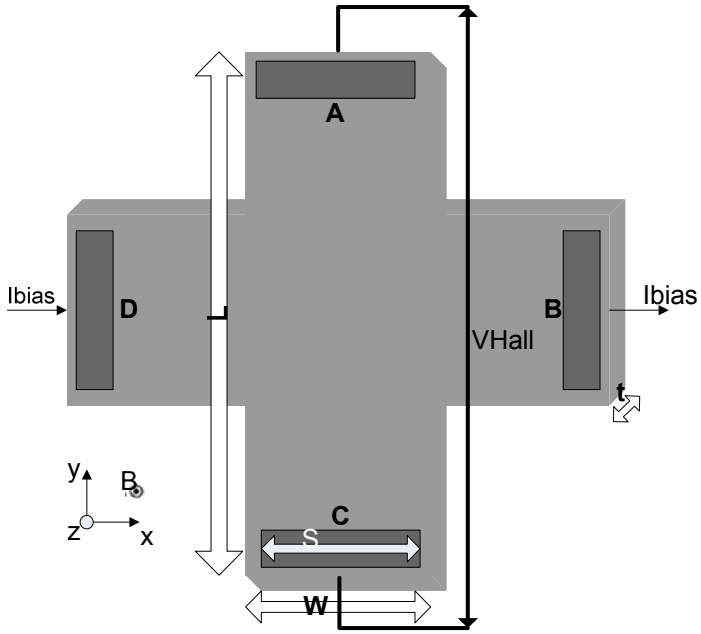
High Voltage Microelectronics and Sensors (HVMS) Group, Department of Engineering, University of Cambridge, United Kingdom

Secretary, IEEE Switzerland ExCom
Chair, IEEE WIE Switzerland

OUTLINE

- Different Hall cells configurations have been integrated in bulk CMOS technology and analyzed in terms of their specific parameters.
- A selection of these shapes will be also integrated in a CMOS SOI technology.
- Geometry plays an important role in Hall cells performance, the optimum cell is presented in this work.
- The most important parameters of a specific Hall cell, based on SOI structure, are evaluated through three-dimensional physical simulations.

Hall Effect Sensors



(1) $$V_{HALL} = S_A B$$

$$S_A = \frac{Gr_H}{nqt} I_{bias} \quad (2)$$

- low-power applications
- current sensing
- position detection & contactless switching

Hall Cells Design Selection

- Different 3D Hall sensors were integrated in bulk CMOS.
- They are all symmetrical and orthogonal structures.
- The geometry plays an important role in the sensors performance.

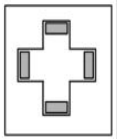
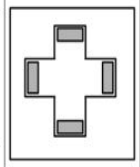
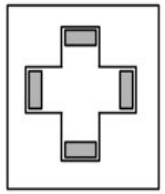
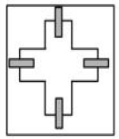
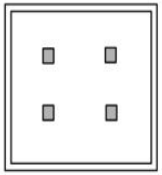
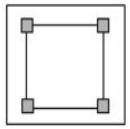
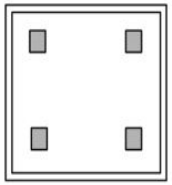
$$G \cong 1 - \frac{16}{\pi^2}\exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\left[1 - \frac{8}{9}\exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\right]\left(1 - \frac{\theta_H^2}{3}\right) \qquad (3)$$

valid if $0.85 \le L/W < \infty$ and $0 \le \theta_H \le 0.45$

Hall Effect Sensors Measurements

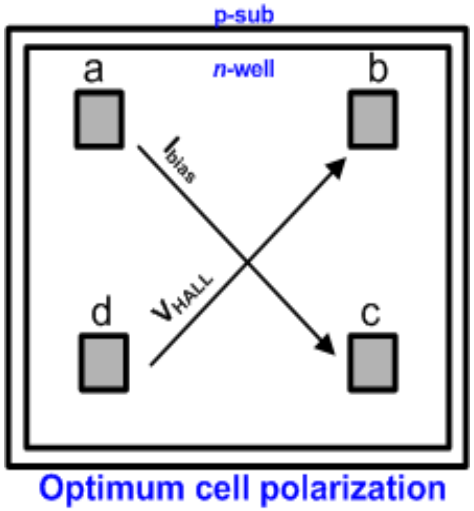
- Measurements results on nine different Hall Effect sensors
- Strict project specifications to be met

Objectives: offset @ T=300 K < ±**30 µT** & *offset drift* < ±**0.3 µT/°C**

Geometry Type	*Basic*	*Low-doped*	*L*	*XL*	*45 Deg*	*Narrow Contacts*	*Borderless*	*Square*	*Optimum*
Integrated Shape (CMOS 0.35 µm)									
R_0(kΩ) @ T=300 K, B=0 T	2.3	5.6	2.2	2.2	2.1	2.5	1.3	4.9	1.5
S_A (V/T) @ I_{bias}=1 mA	0.0807	0.3392	0.0804	0.0806	0.0807	0.0822	0.0325	0.0884	0.0635
Offset drift (µT/°C) (4-phase current spinning)	0.409	0.067	0.264	0.039	0.373	0.344	0.526	0.082	0.328
L, W (µm) of the Active Area (N-well)	L=21.6	L=21.6	L=32.4	L=43.2	L=21.64	L=21.6	L=50	L=20	L=54
	W=11.8	W=11.8	W=17.8	W=22.6	W=11.8	W=9.5	W=50	W=20	W=54
L/W	1.83	1.83	1.82	1.91	1.83	2.27	1	1	1
s (µm) for Sensing Contacts	11	11	16	20.7	11	1.5	2.3	2.3	5.4
Geometrical Correction Factor *(G)*	0.913	0.913	0.912	0.924	0.913	0.87	0.76	0.73	0.74

Single Phase and Residual Offset

- Cell polarization and the corresponding phases



Optimum cell polarization

Phases	Ibias	V_{HALL}
Phase 1	a to c	b to d
Phase 2	d to b	a to c
Phase 3	c to a	d to b
Phase 4	b to d	c to a

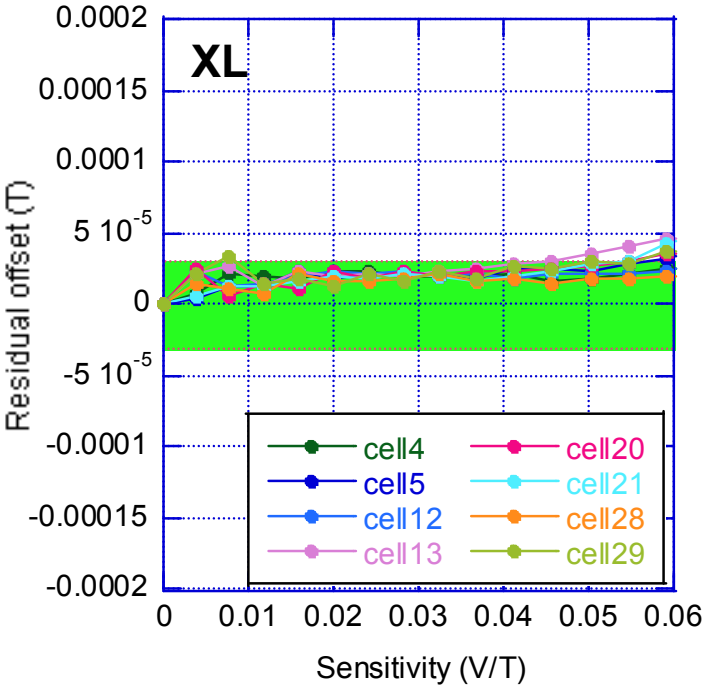
- Single phase offset and residual offset

$$V_{out} = V_{HALL}(B) + V_{offset} \quad (4)$$

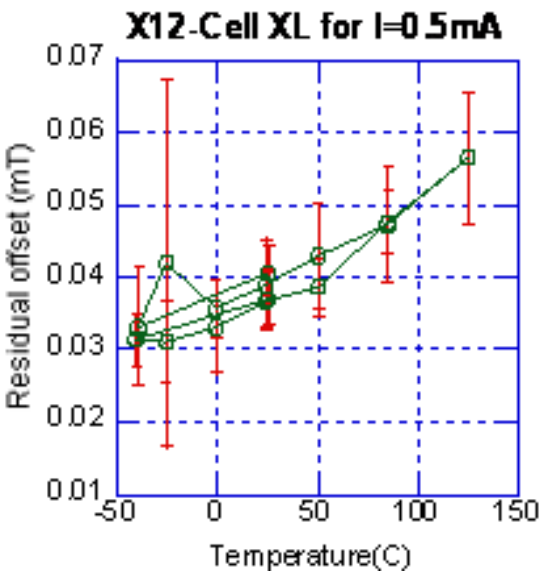
$$Offset_{residual\ (4\,phase)} = \frac{V_{P1} - V_{P2} + V_{P3} - V_{P4}}{4} \quad (5)$$

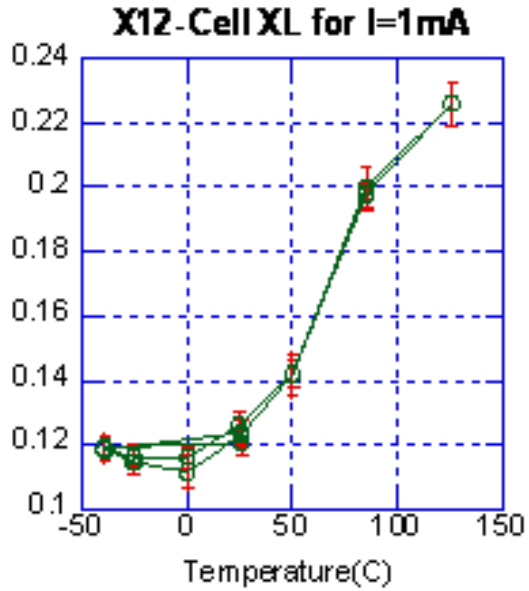
Offset Measurements of bulk CMOS Hall sensors

- An AC automated measurement setup was used to test the Hall structures.
- Manual phase switching was used in the case of temperature investigation.
- Experimental data presented for XL Hall cell (regular bulk CMOS technology).



Residual offset vs. sensitivity for XL cell





Residual offset vs. temperature for XL cell

Regular bulk vs. SOI CMOS technology

The sensors fabricated in SOI (***S***ilicon ***O***n ***I***nsulator) technology have obvious benefits, with respect to the bulk Hall sensors.

- higher magnetic sensitivity
- less noise generation
- possibility to use lower biasing voltage
- smaller leakage current through the dielectric
- enhanced radiation resistance etc.

SOI CMOS technology

➢ The stacking of the layers, according to a SOI XFAB XI10 fabrication process.

➢The active silicon layer is found on top of the dielectric buried silicon oxide (SiO_2) layer, which is in its turn found on the silicon substrate, or handle wafer.

DOPING CONCENTRATIONS IN THE SOI HALL CELL FABRICATION

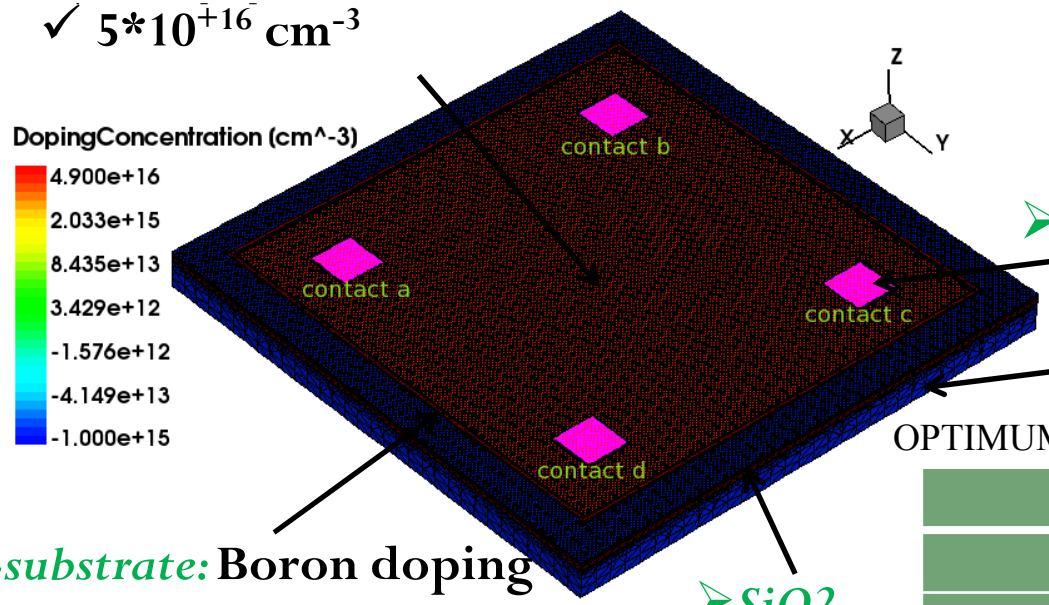
Layer	Type	Numerical value
Wafer (handle) substrate	Si, p-doped (Boron)	6.5 E+14 cm^{-3}
Dielectric	Buried Silicon Oxide, $Si0_2$	
p-substrate in active Silicon layer	Si, p-doped (Boron)	1E+15 cm^{-3}
n-well in active Silicon layer	Si, n-doped (Arsenic)	5E+16 cm^{-3}

The 3D Simulation of SOI Hall Cells

➢**The structure follows the SOI XFAB XI10 fabrication process.**

➢*active n-well region:* **Arsenic doping**

- ✓ **Uniform profile implantation**
- ✓ **$5*10^{+16}$ cm^{-3}**



➢*electrical contacts*

➢*Handle wafer*

➢*p-substrate:* **Boron doping concentration of 10^{+15} cm^{-3}**

➢*SiO2*

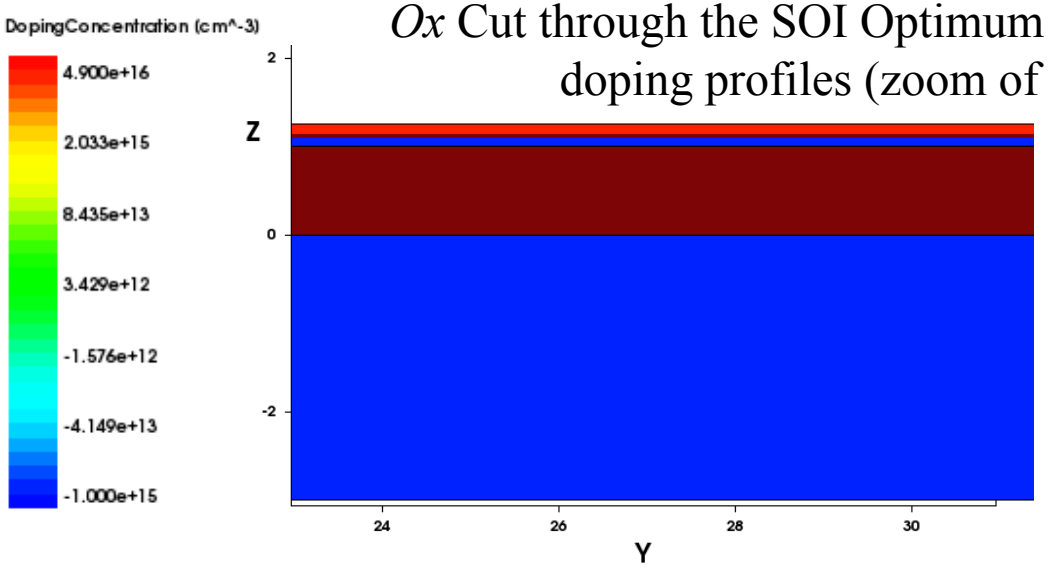
OPTIMUM HALL CELL DESIGN FEATURES

Parameter	Value
L (µm)	50
W (µm)	50
Contacts dimensions (µm)	4.7

The 3D model of Optimum SOI Hall cell

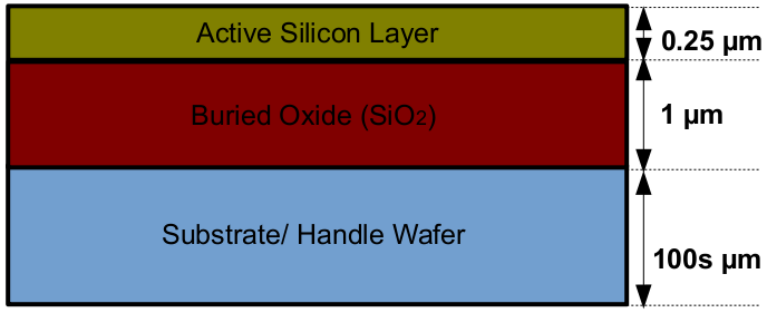
Three-Dimensional Physical Simulations

➢ **Details on the SOI process layering:**

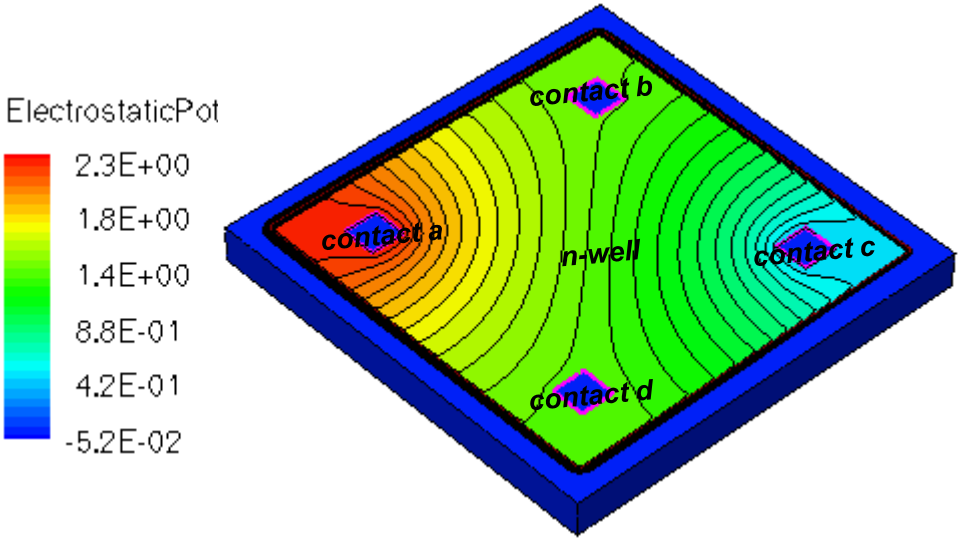


Ox Cut through the SOI Optimum Hall cell, depicting the doping profiles (zoom of a certain area)

The fabrication layers of an SOI XFAB XI10 integration process

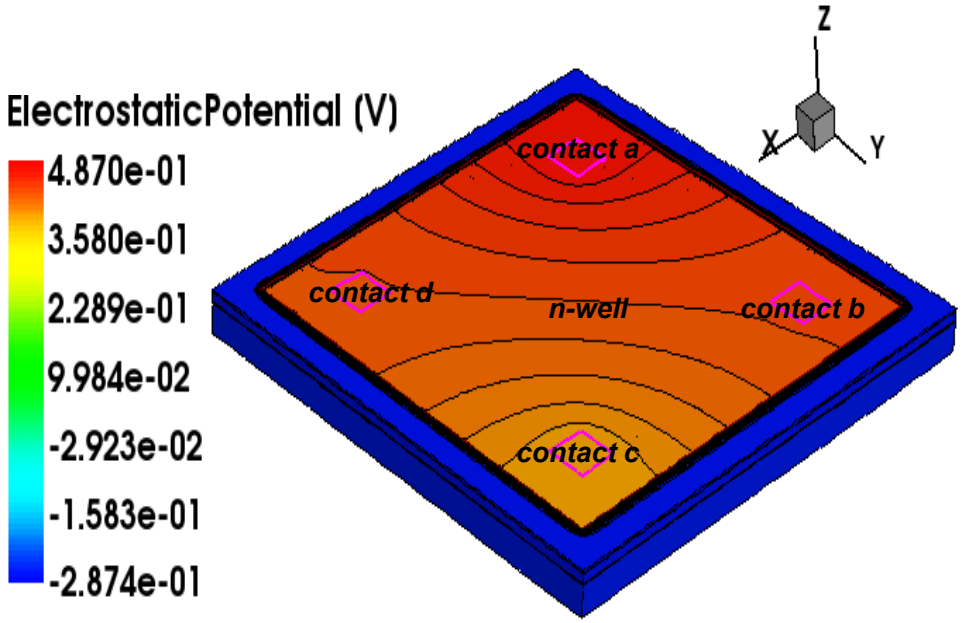


The simulated Hall cells (bulk vs. SOI CMOS)



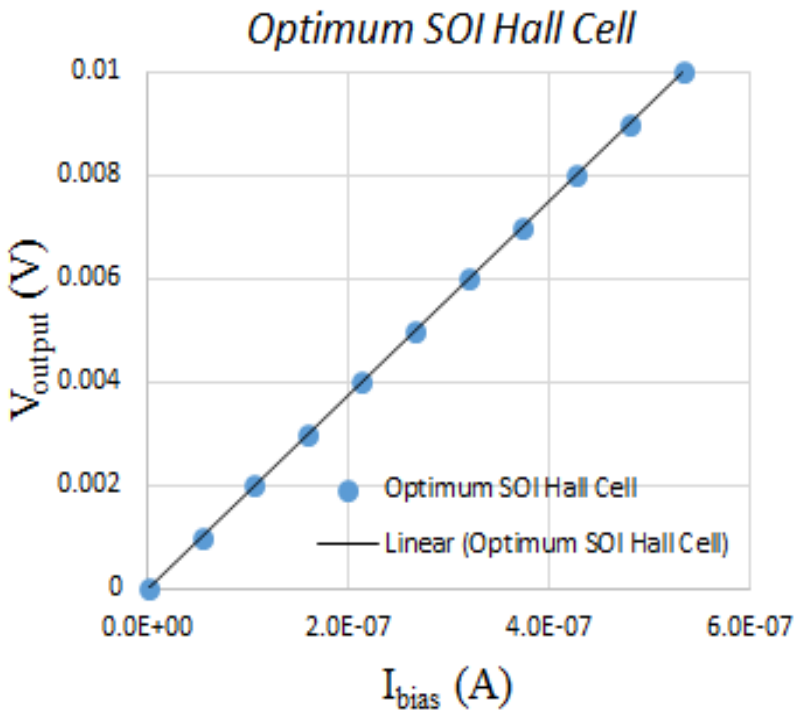
Bulk Optimum Cell, Vbias=1V, B=0.5 T

SOI Optimum Cell, Vbias=0.01V, B=0.05 T

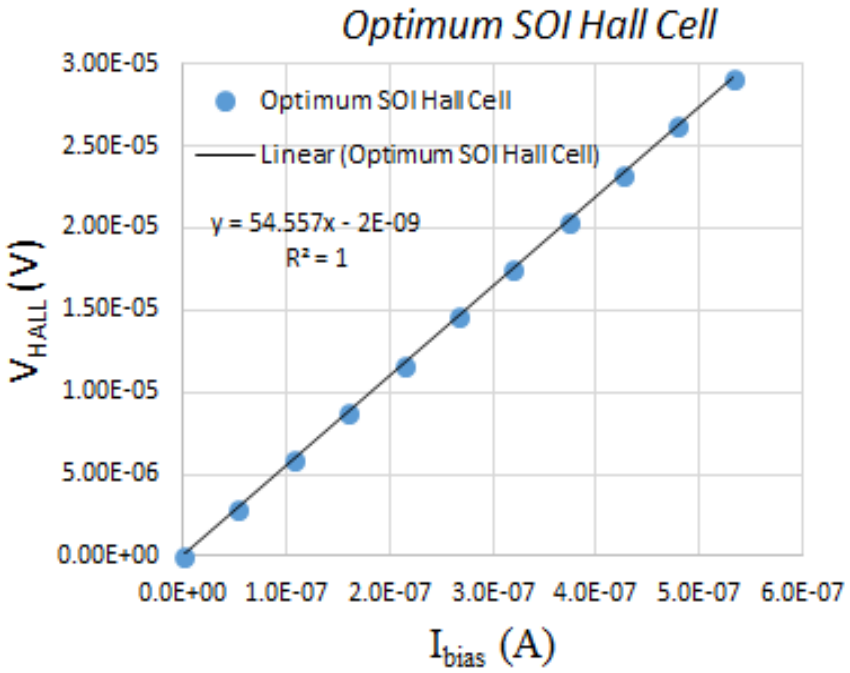


3D Simulations results (I)

- **I-V characteristics**
- **V_{HALL} estimation**
- **Sensitivity numerical estimation**
- **Temperature effects**

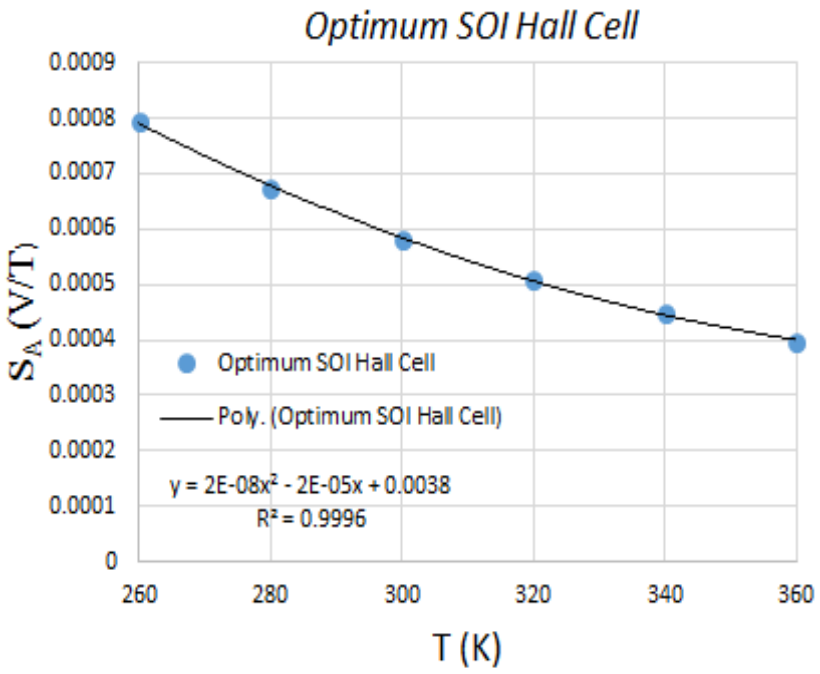


V-I characteristics of the SOI Basic Hall cell

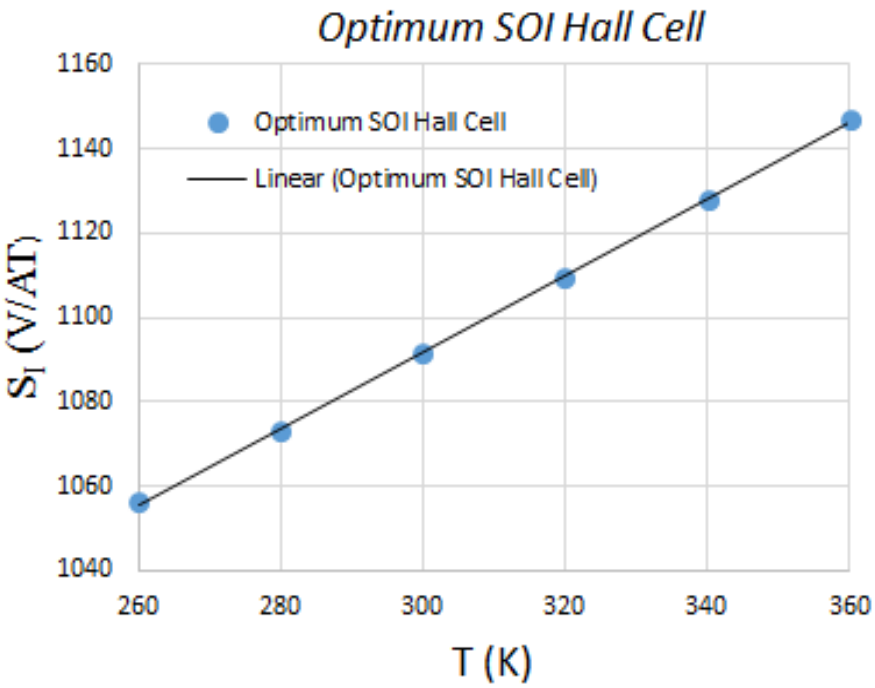


Hall voltage vs. biasing current for the SOI optimum Hall cell

3D Simulations results (II)



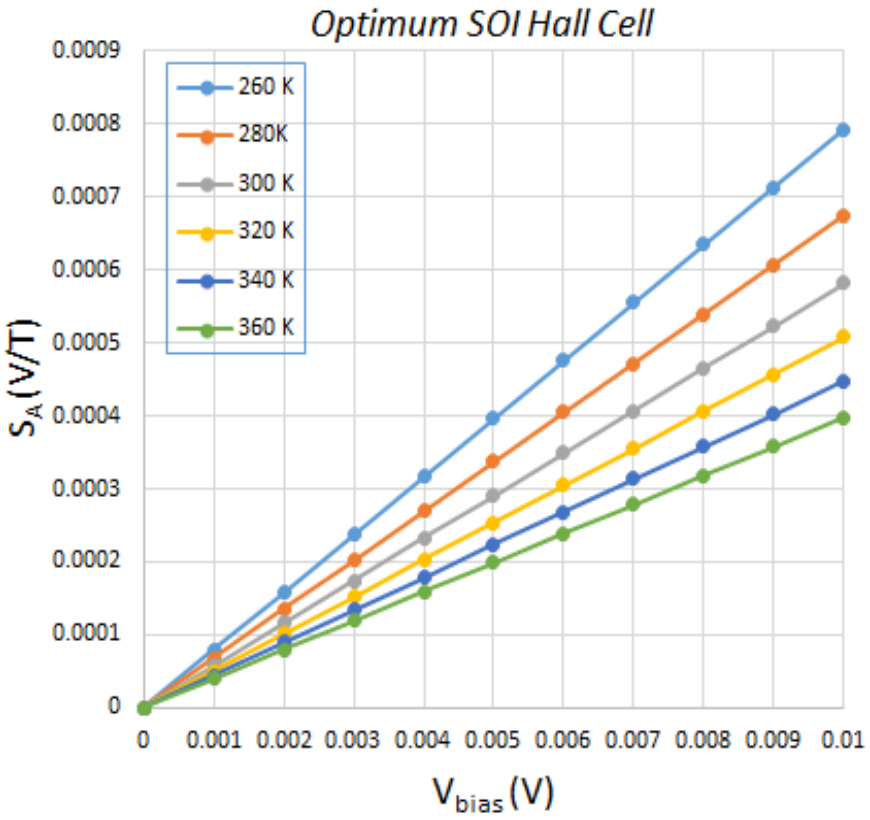
Simulated absolute sensitivity *vs.* temperature



Simulated current-related sensitivity *vs.* temperature

3D Simulations results (II)

- **Simulations with temperature effects were performed**
- **Different temperatures considered**



Simulated absolute sensitivity *vs*. V_{bias}, for different temperatures

3D Simulations results (III)

OPTIMUM HALL CELL PERFORMANCE IN REGULAR BULK AND SOI CMOS TECHNOLOGY

Parameters	CMOS bulk	CMOS SOI
R_{input} (kΩ)	1.8*	18.7**
V_{HALL} (mV) for V_{bias}=0.01 V	1.77E-1*	2.91E-1**
S_A (mV/T) for I_{bias} =5E-7 A	3.2E-5*	5.82E-4**

*measured data
**simulated data

- A very high absolute magnetic sensitivity on one hand and higher input resistance on the other hand.

- In the present case, the input resistance of the optimum cell is almost ten times higher for the SOI technology than the regular bulk CMOS.

- The input resistance can be decreased by adding extended n+ strips around the contacts but in this case the sensitivity will also decrease.

CONCLUSIONS

- This work was intended to analyze the behaviour of a certain optimum Hall cell in a SOI fabrication process, by performing three-dimensional physical simulations.

- To model the SOI Hall cells behavior and predict their performance, 3D physical simulations were performed.

- The Hall voltage, absolute sensitivity and input resistance were extracted through simulations. The electrostatic potential distribution and space charge were looked at for the Optimum SOI Hall cell.

- With respect to equivalent devices fabricated in regular bulk, the Hall devices built in SOI technology offer higher absolute sensitivity.

References (selective list)

[1] Paun M.A., *Hall Cells Offset Analysis and Modeling Approaches*, PhD Thesis, EPFL, Switzerland, 2013.

[2] Paun, M.A., Sallese, J.M., Kayal, M., "*Comparative Study on the Performance of Five Different Hall Effect Devices",* Sensors, ISSN 1424-8220, Vol. **13,** Issue 2, 2013, pp. 2093-2112.

[3] Paun, M.A., Sallese, J.M., Kayal, M., *"A circuit model for CMOS Hall Cells Performance Evaluation Including Temperature Effects"*, Advances in Condensed Matter Physics, Vol. **2013**, Article ID 968647, 10 pages, 2013.

[4] Paun, M.A., Sallese, J.M., Kayal, M., *"Temperature considerations on Hall Effect sensors current-related sensitivity behaviour"*, Analog Integrated Circuits and Signal Processing: Vol. **77**, Issue 3, pp. 355-364, 2013.

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Thank you for your attention!