

# Design and Simulation MOSFET Models: Closing the Gap

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## Motivation

- › **Develop a MOSFET model for analog design**
  - › Must describe all regions of operation
- › **Simulation models have become**
  - › Very accurate, but...
  - › Very complex, inadequate for hand calculation!
- › **Design is not done “by SPICE”!**
  - › Model used in design must be simple but relatively accurate
  - › SPICE provides the ultimate accurate verification
- › **Start from physics**
  - › Minimize number of parameters
  - › Use Matlab for help!

# Overview

- **Applications and Requirements**
- **Compact Model Approximation**
  - Basic Equations
  - Parameters and their Extraction
- **$g_m/I_D$  Analog Design Methodology**
- **Design Example**
  - Opamp Design
  - Design Verification
- **Conclusion**

# Applications of Device Models

- **Estimation/Design**
  - Simple for hand-calculation
  - Accurate for relevant results!
  - Examples: Level=1,  $\alpha$ -Power
- **Circuit Simulation (SPICE)**
  - Currents and Charges function of terminal voltages
  - Continuous functions and first derivatives over
    - All regions of operations
    - Temperatures
    - Geometries
  - Model parameters: physical and scalable
- **Device Simulation**
  - Semiconductor-device physics carrier concentrations

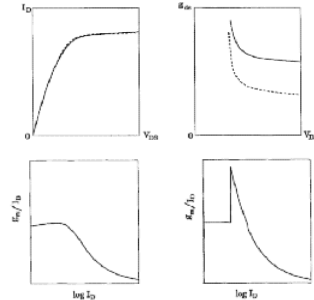
## Device Model Requirements for IC Design Applications

### ➤ Digital Circuits

- Very accurate  $I_{ON}$  and  $I_{OFF}$  (subthreshold)
- No negative conductances

### ➤ Analog Circuits

- Accurate everywhere especially transition regions!
  - Accurate  $I_D$  in all regions
  - Accurate values for small-signal
    - $g_m, g_{ds}, g_{mbs}, C_{gs}, C_{gd}$
  - Correct small-size



## Application: Analog CMOS Design

### ➤ Operation at low $V_{GS}-V_{TH}$ (Moderate Inversion)

- Maximum gain according to LEVEL=1 (strong-inversion only)

$$a_v = \frac{g_m}{g_o} = \frac{2}{\lambda(V_{GS}-V_{TH})}$$

- $V_{GS}-V_{TH} \downarrow a_v \uparrow$ ;  $V_{GS}-V_{TH} \rightarrow 0$ ,  $a_v \rightarrow \infty$ , better model is needed!
- Low-power - moderate or weak inversion
- **Operation up to the edge of saturation**
  - Max output resistance
  - Max output swing
- **Estimation model accuracy needed**
  - from weak to strong inversion
- **Big Gap with latest simulation models!**

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# Charge-Based Estimation Model

- Charge Sheet Model (surface potential model) [1]

$$I_D dx = \mu W [-Q'_i d\psi_s + U_T dQ'_i]$$

- Compact Model replace  $\psi_s$  by mobile charge density  $Q'_i$ 
  - by introducing constant parameter  $n$  (the slope factor) [2,3]

$$d\left(-\frac{Q'_i}{C'_{oc}}\right) = -n d\psi_s$$

$$I_D dx = -\mu C'_{ox} W \left[ \frac{1}{n} \left( -\frac{Q'_i}{C'_{ox}} \right) + U_T \right] d\left(-\frac{Q'_i}{C'_{ox}}\right)$$

\* [1] Brews J.R.

A charge sheet model for the MOSFET. Solid-State-Electronics. Vol 21, p 345-355, 1978.

\* [2] Cunha A.I.A., Scheider M.C. and Galup-Montoro C.

An MOS transistor model for analog circuit design. IEEE. JSSC, vol 33, n° 10, p 1510-1519, oct 1998.

\* [3] Enz C., Krummenacher F. and Vittoz E.

An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. Analog Integrated Circuits and Signal Processing, Vol 8, p 83-114, 1995.

## Charge-Based Estimation Model (Cont'd)

- › Define normalized  $q$ , 
$$q = -\frac{Q'_i}{2nU_T C'_{ox}}$$
- › Define the specific current  $I_S$ , the transition point W.I. – S.I.

$$I_S = 2nU_T^2 \mu C'_{ox} \frac{W}{L} = 2nU_T^2 \beta$$

- › Normalized current – charge equation

$$i = \frac{I_D}{I_S} = [q^2 + q]_{V_D}^{V_S} = i_F - i_R$$

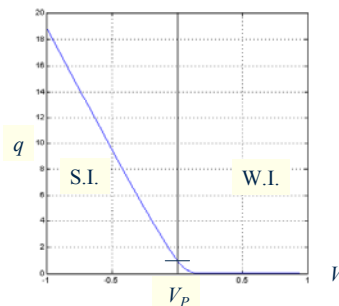
- › Forward normalized current  $i_F = q_S^2 + q_S$
- › Reverse normalized current  $i_R = q_D^2 + q_D$

## Drain, Source Voltage

- › Charge-voltage equation
- › (SEMI-COND PHYSICS + CONSTANT  $n$  APPROX)

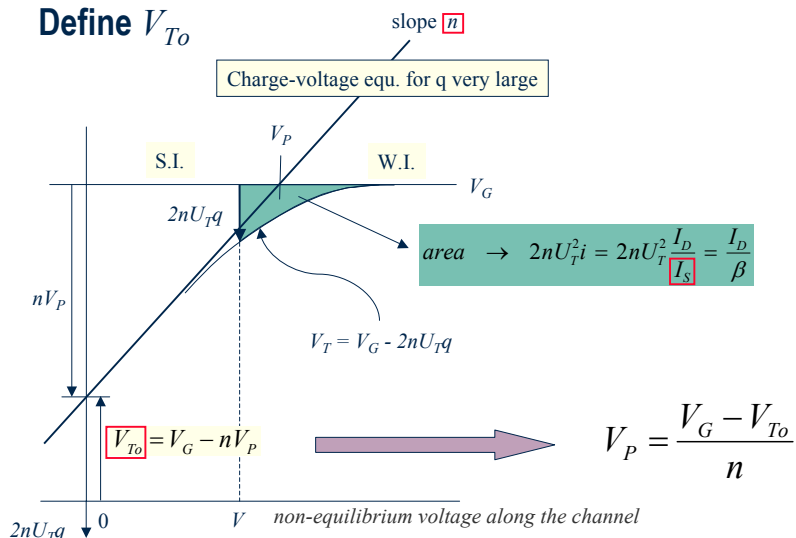
$$V_p - V = U_T [2(q-1) + \log(q)]$$

$V_p$  pinch-off voltage ( $q = 1$ )  
 $V$  is the non-equilibrium voltage along the channel  
 $V = V_S$  at the source  
 $V = V_D$  at the drain



# Gate Voltage

Define  $V_{T0}$



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# $I_D - V_G$ Characteristic – General Philosophy

- The shape of the  $I_D(V_G)$  characteristic changes little as the channel length shrinks, displaying weak (W.I.) and strong inversion (S.I.) regions separated by a moderate inversion region (M.I.).
- The gate controls the inversion layer especially, whereas source and drain control not only the inversion layer but also the regions below and near the junctions.
- Compact models derived from the Charge Sheet representation lend themselves to better representations for gate-driven configurations than source- and/or drain-driven.
- It is possible to reconstruct  $I_D(V_{GS})$  characteristics with less than 2 to 3 % error with only three parameters  $n$ ,  $I_S$  and  $V_{T0}$  and a small-size polynomial  $\theta(i)$ .

$n, I_S, V_{T0}$  and the coeffs of  $\theta$  poly depend on  $V_{DS}, V_{SB}$  and  $L$ , not on  $V_{GS}$ .

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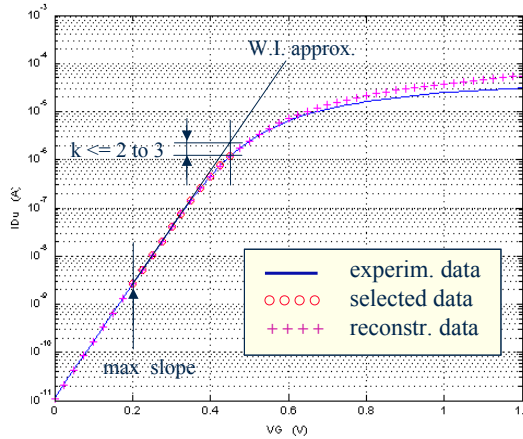
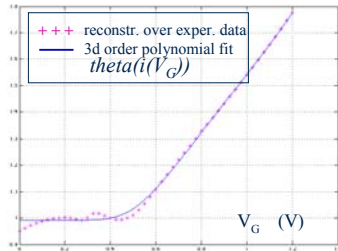
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# Model Parameters $n$ , $V_{T0}$ , $I_S$ and $\theta$ poly

given  $V_{DS}$ ,  $V_{BS}$  and  $L$

- ooo select data in weak-mod inv
- extract param.  $n$ ,  $V_{T0}$ ,  $I_S$
- +++ reconstruct  $I_{Du}(V_G)$
- find coeff. of fitting polynomial  $\theta(i(V_G))$



1.2 V low-power 90 nm technology  
(by courtesy of IMEC)

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# Parameter Extraction: $n$ , $V_{T0}$ and $I_S$

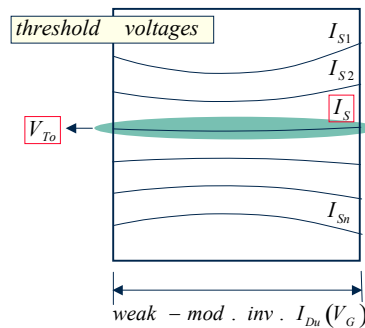
- choose  $I_{Du}(V_G)$  in weak and moderate inversion
- $n$  max. of subthreshold slope
- Iteratively find  $I_S$  that minimizes variance of  $V_{T0}$  for selected  $I_{Du}$ 's ( $I_D$  for  $W = 1 \mu\text{m}$ )

$$I_S \rightarrow i = \frac{I_{Du}}{I_S}$$

$$q = 0.5(\sqrt{1 + 4i} - 1)$$

$$V_p = U_T(2(q-1) + \log(q))$$

$$V_p = \frac{V_G - V_{T0}}{n} \rightarrow V_{T0}$$

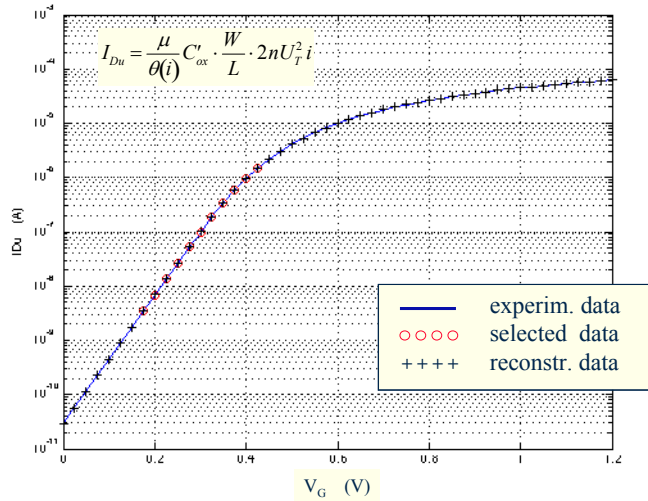


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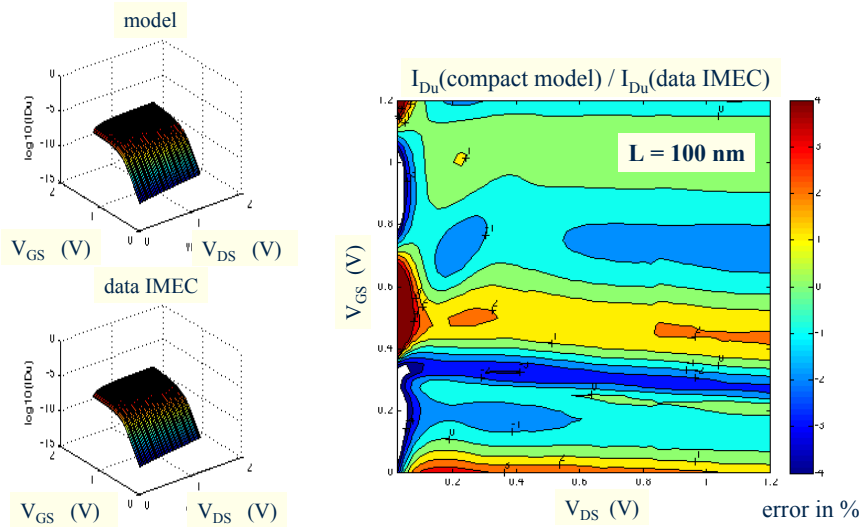
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# Reconstructed $I_D(V_G)$

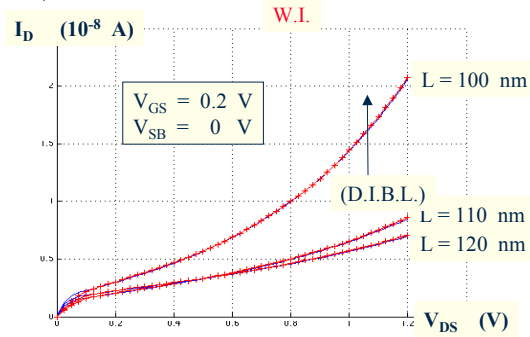
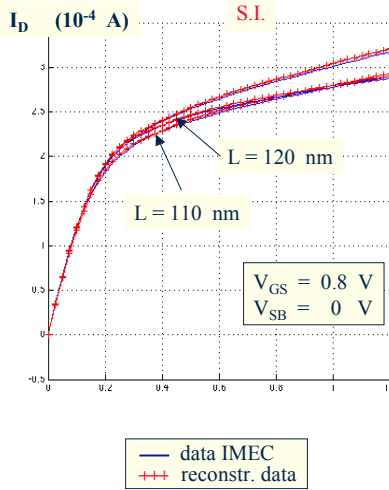


# Model Verification: $I_{Du}(V_{GS}, V_{DS})$

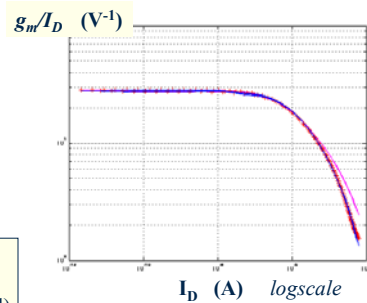
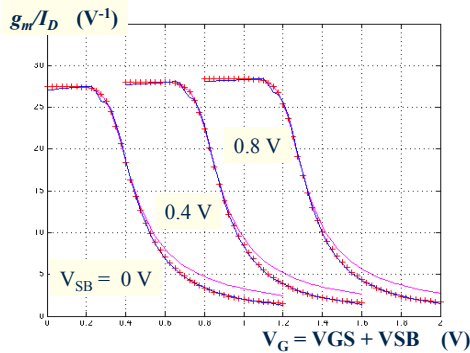




# Drain Current $I_D(V_{DS})$



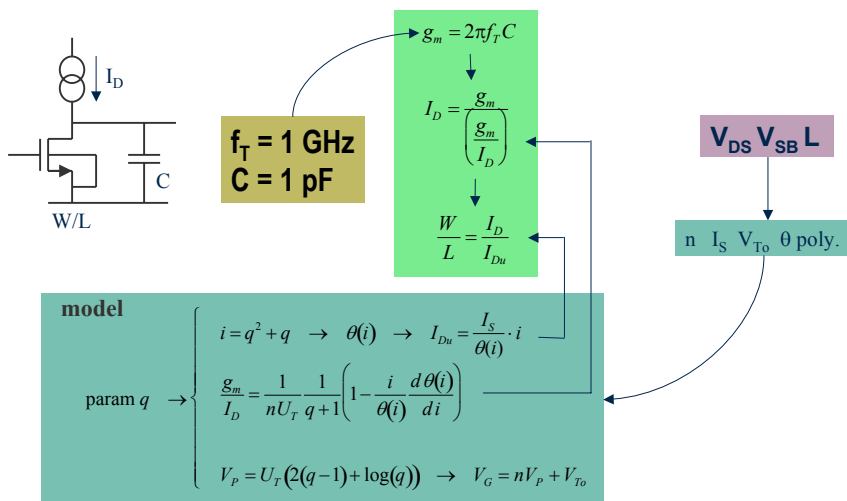
# Model verification: $g_m/I_D$



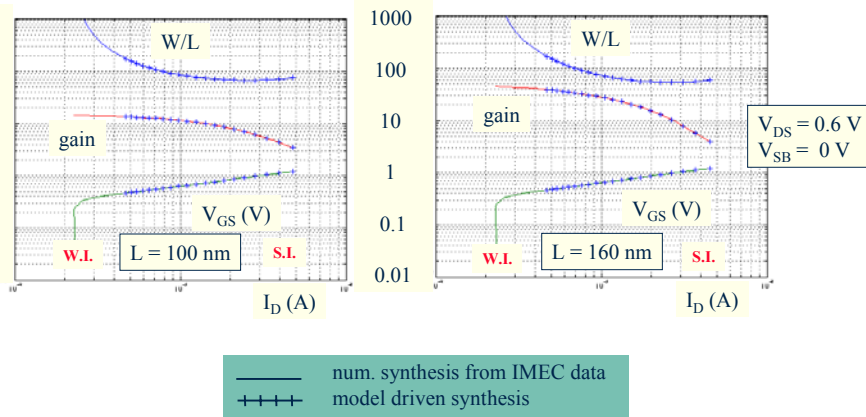
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# Intrinsic Gain Stage – Exploration Phase (1)



## Intrinsic Gain Stage – Exploration Phase (2)



## Design methodology

- $g_m/I_D$  methodology\* is used to derive sizing and currents of the desired circuit
  - $g_m/I_D = f(I_D/(W/L))$
  - Relates  $g_m$ , power, MOS geometry
- **Set source and drain voltages**
  - Fixes  $n I_s$  etc..
  - Allows the evaluation of  $g_m/I_D$  versus  $V_G$
- **Choose current levels as independent variables**
- **Derive  $I_D$  and W/L of MOSFET**

\* F. Silveira, D. Flandre, and P. G. A. Jespers, "A  $g_m/I_D$  Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a SOI Micropower OTA" IEEE JSSC, vol. 31, pp. 1314-1319, Sept. 1996.

# Design Flow\*

- **Exploration phase (Matlab)**
  - Capture circuit performance in analytical expressions
  - Apply proposed MOSFET estimation model with parameters  $n$ ,  $I_s$ ,  $V_{T0}$  extracted for target technology
  - Plot multi-parametric design space
- **Design phase (Constrained optimization in Matlab)**
  - Use Matlab Optimization Toolbox to improve performance in selected design point
  - Selected objective function is optimized
    - under performance and bias constraints
- **Verification and Process centering phase (SPICE)**
  - Uses foundry provided process data with simulation MOSFET model
  - Applies optimization for improving objective performance under constraints
- **Automated layout from sized schematic**

\* A. Vladimirescu, R. Zlatanovici and P. G. A. Jespers, "Analog Circuit Synthesis using Standard EDA Tools", Proc. Int. Symposium on Circuit and Systems, May 2006.

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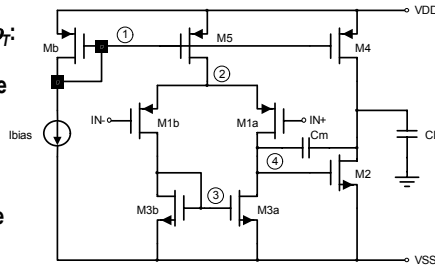
# Design example: CMOS Miller opamp

- $M_{1,a,b}$  are sized based on the desired bandwidth  $\omega_T$ :  

$$g_{m1} = \omega_T \cdot C_m \quad (1)$$
- Non-dominant pole  $\omega_{NDP}$  and the zero  $\omega_Z \rightarrow$  phase margin:  

$$\omega_{NDP} = NDP \cdot \omega_T; \quad \omega_Z = Z \cdot \omega_T \quad (2)$$
- $M_{3,a,b}$  have the same gate voltage as  $M_2$  for minimizing offset;
- $M_b, M_4$  and  $M_5$  operate in strong inversion and are sized to provide the desired current levels in the differential pair and second stage;
- The  $W/L$  of the transistors can be computed from:
- Inversion level  $i_1$  for transistors  $M_{1,a,b}$ , and  $i_2$  for  $M_2$ , are taken as parameters
  - in the design space of equal area, gain and current-supply curves
- Transistors'  $L$  vs.  $L_{min}$   

$$L_{M1} = 3 \cdot L_{min}; \quad L_{M3} = 7 \cdot L_{min}; \quad L_{M2} = L_{min}; \quad L_{M4} = 3 \cdot L_{min}; \quad L_{M5, Mb} = 10 \cdot L_{min}$$
- Symmetry and Matching



$$\frac{W}{L} = \frac{I_D}{2 \cdot n \cdot V_{th}^2 \cdot \mu \cdot C_{ox}} \cdot \frac{1}{i} \quad (3)$$

$$(W/L)_3 = I_{D1} / I_{D2} \cdot (W/L)_2 \quad (4)$$

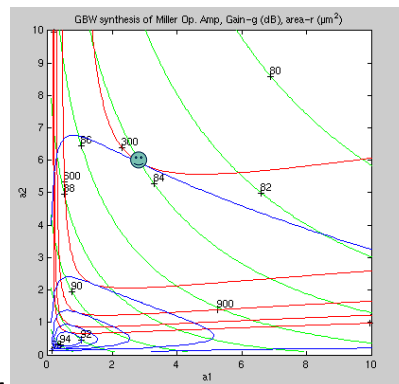
$$(W/L)_4 = I_{D2} / 2I_{D1} \cdot (W/L)_5 \quad (5)$$

# Exploration phase

- Performance space and initial sizing
  - Design tradeoffs between Gain, Supply current and Area
- Select: ☺
  - Gain (GBW as  $\omega_T$  is set) = 84 dB
  - Supply current = 53  $\mu$ A
  - $i_1 = 2.9, i_2 = 6$  in a  $0.25 \mu$ m technology
- Resulting  $W$  and  $L$ 's for this design point
  - Lead to min Area of  $300 \mu$ m<sup>2</sup>
  - Did not take into account terminal voltages!

Initial sizes:

Transistor	W ( $\mu$ m)	L ( $\mu$ m)	Transistor	W ( $\mu$ m)	L ( $\mu$ m)
M1a-b	10.8	0.75	M4	15	0.75
M2	15	0.25	M5	10	2.5
M3a-b	13.6	1.75	Mb	10	2.5



— Gain [dB]  
— Supply Current [ $\mu$ A]  
— Area [ $\mu$ m<sup>2</sup>]

## Design phase

- **Constrained design optimization**

- **Maximize GBW**

- Parameters:  $I_{D1}$ ,  $I_{D2}$ ,  $(W/L)_1$ ,  $(W/L)_2$ ,  $(W/L)_3$

- Constraints: DC, AC, transient, symmetry

$$V_{GT} = 2nU_T \log \left[ \exp \left( \sqrt{\frac{I_D}{2nU_T^2 K_{n,p} (W/L)}} \right) - 1 \right]$$

M1 bias	$V_{GT1} \leq V_{cm,min} + V_{T,p} - V_{T,n}$
M2 bias	$V_{GT2} \leq V_{out,min}$
M4 bias	$V_{GT4} \leq V_{DD} - V_{out,max}$
M5 bias	$V_{GT5} + V_{GT1} \leq V_{DD} - V_{cm,max} - V_{T,p}$
Unity gain bw	$\omega_T \geq \omega_{min}$
Slew rate	$2 \cdot I_{D1} / C_m \geq SR_{min}$
Non-dominant pole	$\omega_{NDP} \geq NDP \cdot \omega_T$
Zero	$\omega_Z \geq Z \cdot \omega_T$

## Verification phase

- **SPICE verification with actual process parameters**

- **Design objective:**

- Maximize Gain: 84 dB min

- **Main constraints**

- Unity-gain Bandwidth  $\geq 10$  MHz

- Slew rate  $\geq 1V/\mu s$

- Phase margin  $\geq 45^\circ$

- **Matlab design matches simulated circuit within 10% except for  $f_T$**

- **Design point corresponds to both stages operating in moderate inversion with  $(I_D/I_S)_1 = 2.9$  and  $(I_D/I_S)_2 = 6$**

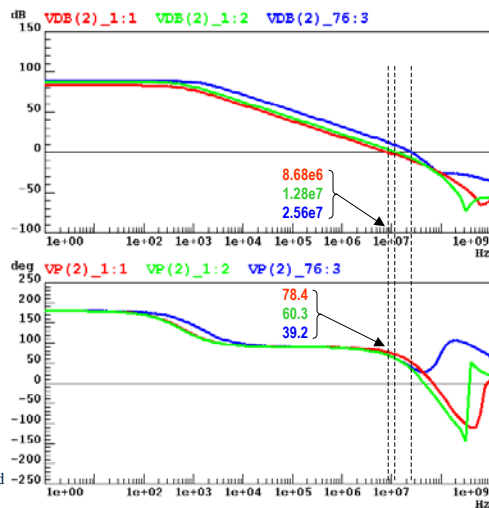
# SPICE optimization

Parameter	Initial value	Matlab	Eldo optimal
(W/L)1	10.8/0.75	13.85	136.5
(W/L)2	15/0.25	22.4	49
(W/L)3*	13.6/1.75	1.87	1.13
(W/L)4*	15/0.75	82.48	86.5
(W/L)b	10/2.5	13.79	1.95
Cm (pF)	1	0.26	0.2
ID1 ( $\mu$ A)	4.5	1.54/1.55	2.6
ID2 ( $\mu$ A)	60	18.5/28.6	328
Gain (dB)	84/83	91/87.7	89
FT (MHz)	15/9	16/12.5	26
GBW (GHz)	127	303	693

\* Derived based on Eq. (5) and (6)

— SPICE (Eldo) Optimized  
— Matlab Optimized  
— Design  
— Initial Design Point

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Simulated Gain, in dB, and Phase for the opamp output VDB(2), VP(2), ESSCIRC'06

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# Conclusion

- **Design model based on charge-sheet is proposed\***
  - Good match with measurement with just a few parameters
- **MOSFET models for design differ from simulation ones**
  - Need to be simple enough but accurate
  - Describe operation in all regions of operation
  - Contain very few parameters
  - Closer to physics
- **$g_m/I_D$  methodology based on proposed model is exemplified**
  - Automated design flow
  - Opamp synthesis using simple model is verified and improved by complete simulation

\* P. G. A. Jespers, "The  $g_m/I_D$  Methodology, a Synthesis Tool for Low-Voltage Analog CMOS Circuits", Springer, to be published spring 2007