Status of the EKV3.0 MOS Transistor Model

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Compact Modelling for Emerging Technologies  
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Presentation Outline

- About EKV3
- Model Code in Verilog-A
- Physical Effects & Parameters
  - Parameter Extraction Basic Methodology
- Modelling Results
- Summary
About EKV3

- A Design-Oriented, Charge-Based Model
- Moderate and Weak Inversion
- Special Attention to Analog/RF IC Design Requirements
  - High Frequency Operation, Noise
- All Pertinent Effects to 45nm CMOS
  - Scaling over Technologies, Geometry, Temperature, Bias
- Validated on Various CMOS Technologies.
  - TOSHIBA, Infineon, Cypress, Atmel.
  - Used for Commercial IC Design.
EKV: Charge Based Modelling

**Inversion Charge**

\[ q_i = q_i (\Psi_s); \quad q_s, q_d \]

**Drain Current**

\[ i = q_s^2 + q_s - q_d^2 - q_d \]

**Transconductance-to-Current Ratio**

\[ \frac{g_m}{i_{d\text{sat}}} = \frac{1}{1/2 + \sqrt{i + 1/4}} \]

**Transconductances**

- \( g_{ms} \propto q_s \)
- \( g_{md} \propto q_d \)
- \( g_m \propto \frac{q_s - q_d}{n} \)

**Capacitances & Charges**

- \( Q_D \propto W \int_0^L x q_i dx \)
- \( Q_S \propto W \int_0^L \frac{1-x}{L} q_i dx \)
- \( C_{XY} = \pm \frac{\partial Q_x}{\partial V_y} \)

**Short-Channel Thermal Noise Induced Gate Noise**

...
EKV3 in Verilog-A

- The Verilog-A Code of EKV3.0
  - Hierarchical Structure
    - 18 files
      - one main file
      - many smaller
    - In Total: 83KB
  - Compatible with (at least)
    ELDO, ADS, SPECTRE, ADMS, …
  - Used as the Reference Code
    for all Model Implementations
    - ADMS provides “standard”
      C-code Various Simulators.
EKV3 and ADMS

- EKV3 Verilog-A Code Tested with ADMS (v2.1)
  - Current version: ADMS v2.2.4
- Tested with XML Interface for SPICE3
- Different XML Interfaces for Different Simulators
EKV3 “Design Kit” in ADS

- Tiburon: A Verilog-A Compiler in ADS
- An EKV3 “Design Kit” for ADS has been developed
  - Design Kit contains 8 Elements, only MOSFET
    - QS / NQS
    - NMOS / PMOS
    - MODEL-CARD / INSTANCE
  - 120nm CMOS Design Kit has been used to Design
    - Base-Band Elements (OP-AMPs)
    - LNA
EKV3 in ELDO (C-code)

- In ELDO a Hand-Written C-code Version of the Model exists
- Verilog-A Code: Simpler but less Efficient
  - Not always Efficiently handled by the Simulators
- Generally “Verilog-A + ADMS” and C-code have the same Functionality
## Phenomena covered by EKV3.0 -- Associated Parameters

<table>
<thead>
<tr>
<th>Modelled effect</th>
<th>Related Parameters / Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Physical Modelling of Charges</strong></td>
<td>COX(TOX), PHIF, GAMMA(NSUB), VTO(VFB), GAMMAG(NGATE)</td>
</tr>
<tr>
<td>Including Accumulation Region</td>
<td></td>
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<tr>
<td>Polysilicon Depletion, Quantum Mechanical Effects</td>
<td></td>
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<tr>
<td><strong>Bias-Dependent Overlap Capacitances</strong></td>
<td>LOV, GAMMAOV(NOV), VFBOV</td>
</tr>
<tr>
<td><strong>NQS</strong></td>
<td>[Channel Segmentation]</td>
</tr>
<tr>
<td><strong>RF Model</strong></td>
<td>[Appropriate Scaling of RG, RSUBs with W, L and NF]</td>
</tr>
<tr>
<td>External Sub-Circuit</td>
<td></td>
</tr>
<tr>
<td><strong>Mobility</strong> (Reduction due to Vertical Field Effect)</td>
<td>KP(U0), E0, E1, ETA ZC, THC</td>
</tr>
<tr>
<td>Surface Roughness-, Phonon-, Coulomb Scattering</td>
<td></td>
</tr>
<tr>
<td><strong>Impact Ionization Current</strong></td>
<td>IBA, IBB, IBN</td>
</tr>
<tr>
<td><strong>Gate Current</strong> (IGS, IGD, IGB)</td>
<td>KG, XB, UB</td>
</tr>
</tbody>
</table>

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## Phenomena covered by EKV3.0 -- Associated Parameters

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<thead>
<tr>
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<tbody>
<tr>
<td><strong>Longitudinal Field Effect</strong></td>
<td></td>
</tr>
<tr>
<td>Velocity Saturation, Channel Length Modulation</td>
<td>UCRIT (VSAT), LAMBDA, DELTA</td>
</tr>
<tr>
<td><strong>Reverse Short Channel Effect</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LR, QLR, NLR</td>
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<tr>
<td><strong>Inverse Narrow Width Effect</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>WR, QWR, NWR</td>
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<tr>
<td><strong>Drain Induced Barrier Lowering</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ETAD, SIGMAD</td>
</tr>
<tr>
<td><strong>Source and Drain Charge Sharing</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LETA, {LETA2}, WETA</td>
</tr>
<tr>
<td><strong>Halo/Pocket implant effects</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LETA0</td>
</tr>
<tr>
<td><strong>Edge Conduction</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>WEDGE, DGAMMAEDGE, DPHIEDGE</td>
</tr>
<tr>
<td><strong>Geometrical Effects, Width scaling</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Various Parameters (DL, WQLR, ...)</td>
</tr>
<tr>
<td><strong>Noise</strong></td>
<td>AF, KF</td>
</tr>
<tr>
<td>Flicker Noise, Short-Channel Thermal Noise,</td>
<td></td>
</tr>
<tr>
<td>Induced Gate and Substrate Noise</td>
<td></td>
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<tr>
<td><strong>Temperature Effects</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Various Parameters</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>&lt;100</td>
</tr>
</tbody>
</table>
Basic Parameter Extraction Methodology

Wide Long CV
- CGG vs VG:
  - COX, VTO, GAMMA, PHIF, GAMMAG

Wide Short IV
- gm vs VG (lin):
  - DL, RSX
  - (fixing RSCE for correct $V_{TO}$)

Wide Long IV
- gm vs VG (lin):
  - KP, E0, E1, [ETA]

Wide All Lengths IV
- VTO vs L:
  - LR, QLR, NLR
  - {RSCE}, [LETA, LETA2, ETAD]

Wide Short CV
- CGG vs VG:
  - LOV, GAMMAOV, [VFBOV], DLC

Narrow channel
similar procedure

Width scaling:
All lengths w.r.t. width

Narrow short
combined effects
[fine tuning]

Temperature analysis

END
Short-Channel Characteristics

$L = 70\text{nm}$

- Correct Weak & Moderate Inversion Behaviour
  - Smoothness and Correct Asymptotic Behaviour
  - Correct Weak Inversion Slope and DIBL Modeling
- Transconductance-to-Current Ratio vs. Drain Current (log. axis)
Short-Channel Output Characteristics

L = 70nm

L = 70nm VB = 0V

L = 70nm VB = -1V

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NQS Model @ RF \([\text{Re}(Y_{21}), \text{Im}(Y_{21})]\)
Edge Conduction Effect on $I_D$ and $g_m/I_D$

- **NMOS 10um/10um**
  - $L=10um$
  - $V_D=1V$

- **NMOS 10um/80nm**
  - $L=80nm$
  - $V_D=1V$
Gate Current & Edge Conduction

- Gate Current is also affected by Edge Conduction
- EKV3.0 gives reasonable fits to ID, gm/ID, IG even in case of presence of Edge Conduction Effect
- Edge Conduction affects gm/id dramatically in Weak-Moderate Inversion
Temperature Scaling

L = 150nm

- $I_D - V_G$ and $I_D (g_{ds}) - V_D$ vs. Temperature
## EKV3 and Industries

<table>
<thead>
<tr>
<th>Company</th>
<th>Processes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOSHIBA Semiconductors</td>
<td>✓ 140nm</td>
</tr>
<tr>
<td></td>
<td>✓ 110nm</td>
</tr>
<tr>
<td></td>
<td>✓ 80nm</td>
</tr>
<tr>
<td>Infineon Technologies</td>
<td>✓ 120nm</td>
</tr>
<tr>
<td></td>
<td>✓ 90nm</td>
</tr>
<tr>
<td></td>
<td>✓ 65nm</td>
</tr>
<tr>
<td>Cypress Semiconductors</td>
<td>✓ 150nm</td>
</tr>
<tr>
<td>Atmel Corporation</td>
<td>✓ 350nm</td>
</tr>
<tr>
<td></td>
<td>✓ 130nm</td>
</tr>
<tr>
<td>AustriaMicroSystems</td>
<td>✓ 350nm</td>
</tr>
<tr>
<td></td>
<td>✓ 180nm</td>
</tr>
<tr>
<td>XFAB</td>
<td>✓ 350nm</td>
</tr>
<tr>
<td>Various Co-Operations</td>
<td>✓ Tektronix</td>
</tr>
</tbody>
</table>

![Toshiba Logo](image1.png)
![Infineon Logo](image2.png)
![Atmel Logo](image3.png)
![Cypress Logo](image4.png)
![AustriaMicroLogo](image5.png)

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Developments underway (EKV3.1)

- Vertical Non-Uniform Doping.
- Accounting for Carrier Heating/Velocity Saturation in Induced Gate Noise.
- Mobility Effect to Improve Flexibility for Short-Channel Back-Bias
- Output Conductance Effects in Long Channel Halo/Pocket Implanted Devices
- Layout Dependent Stress Effects
- ...
Summary

- EKV3.0: a design-oriented, charge-based, compact model for Next Generation CMOS
  - Moderate and Weak Inversion, Analog/RF IC Design
  - Validated on Various CMOS Technologies to 65nm.
    - Used for Commercial IC Design.
  - Developed in Verilog-A
    - Verilog-A Code is Available to CAD Vendors.
    - Specific Simulators require Specific XML interface in ADMS
    - MOS Design Kits developed.
  - Implementation ongoing for:
    - ELDO, Smash, GoldenGate, …
    - Spectre, HSPICE, …
Thank you very much
for your time and attention