Status of the EKV3.0 MOS Transistor Model

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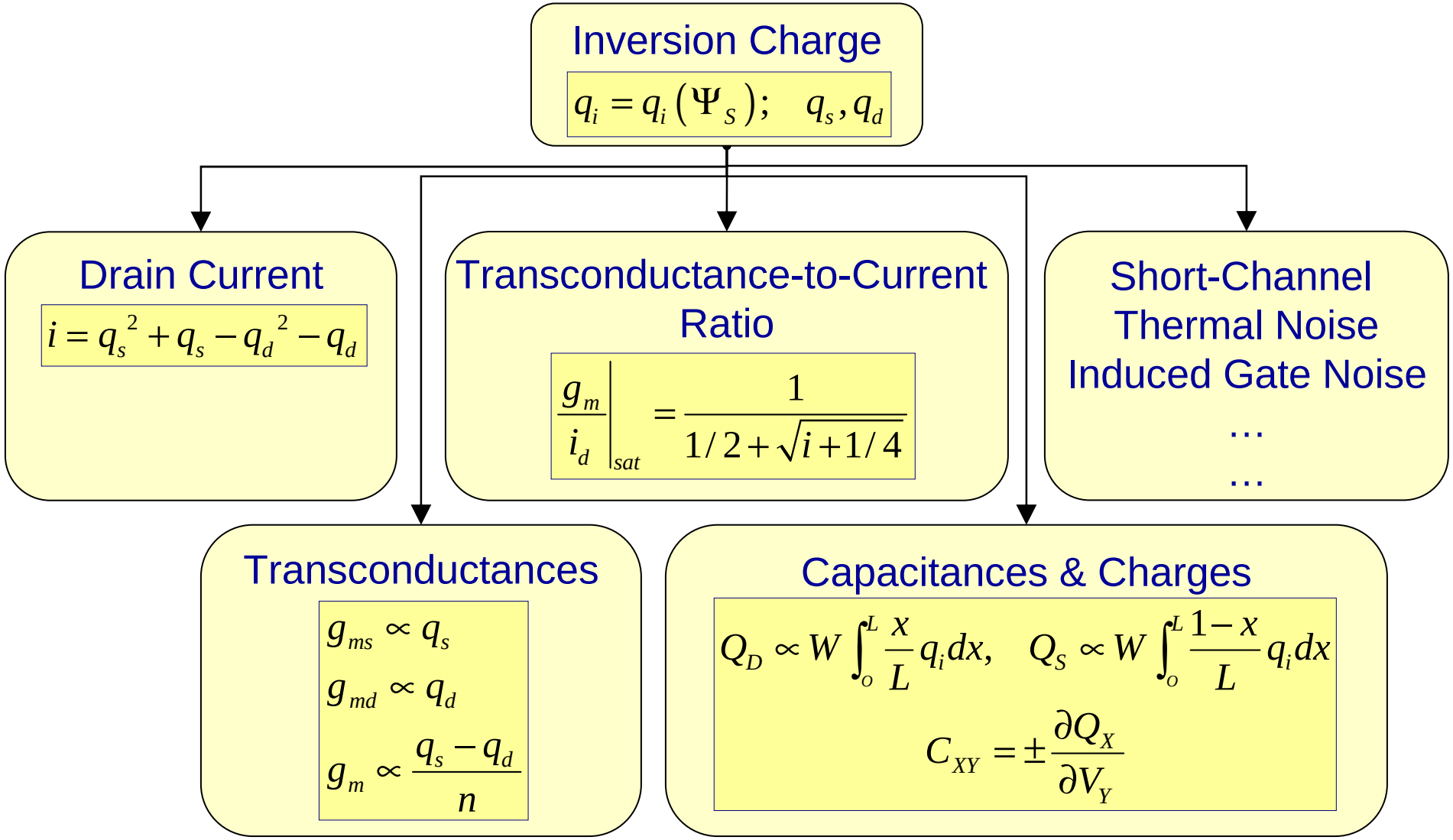
Presentation Outline

- About EKV3
- Model Code in Verilog-A
- Physical Effects & Parameters
  - ✓ Parameter Extraction Basic Methodology
- Modelling Results
- Summary

About EKV3

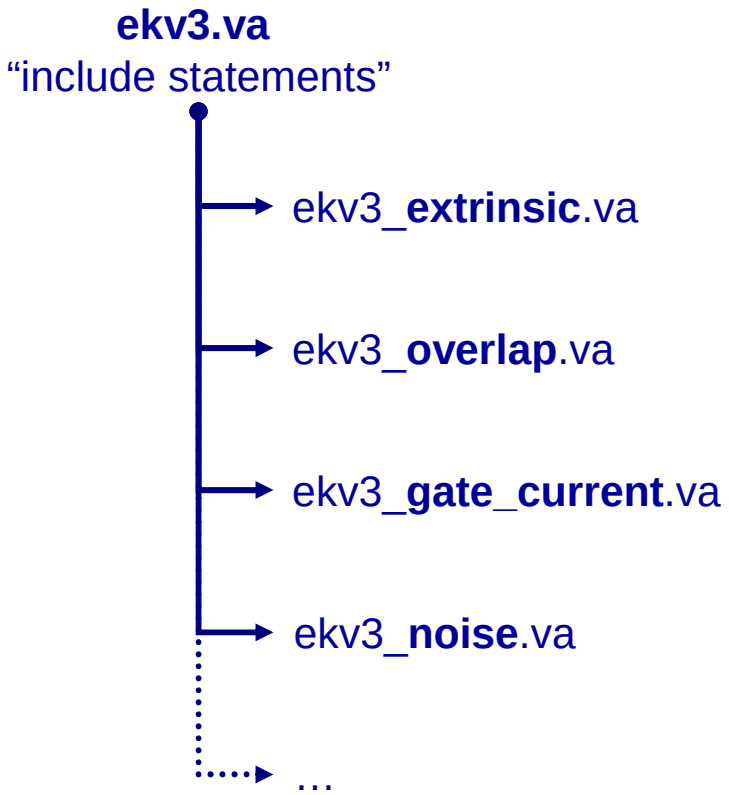
- A Design-Oriented, Charge-Based Model
- Moderate and Weak Inversion
- Special Attention to Analog/RF IC Design Requirements
  - ✓ High Frequency Operation, Noise
- All Pertinent Effects to 45nm CMOS
  - ✓ Scaling over Technologies, Geometry, Temperature, Bias
- Validated on Various CMOS Technologies.
  - ✓ TOSHIBA, Infineon, Cypress, Atmel.
  - ✓ Used for Commercial IC Design.

EKV: Charge Based Modelling



EKV3 in Verilog-A

- The Verilog-A Code of EKV3.0
  - ✓ Hierarchical Structure
    - 18 files
      - one main file
      - many smaller
    - In Total: 83KB
  - ✓ Compatible with *(at least)* ELDO, ADS, SPECTRE, ADMS, …
  - ✓ Used as the Reference Code for all Model Implementations
    - ADMS provides “standard” C-code Various Simulators.



EKV3 and ADMS

- EKV3 Verilog-A Code Tested with ADMS (v2.1)
  - ✓ Current version: ADMS v2.2.4
- Tested with XML Interface for SPICE3
- Different XML Interfaces for Different Simulators

EKV3 “Design Kit” in ADS

- Tiburon: A Verilog-A Compiler in ADS
- An EKV3 “Design Kit” for ADS has been developed
  - ✓ Design Kit contains 8 Elements, only MOSFET
    - QS / NQS
    - NMOS / PMOS
    - MODEL-CARD / INSTANCE
  - ✓ 120nm CMOS Design Kit has been used to Design
    - Base-Band Elements (OP-AMPs)
    - LNA

EKV3 in ELDO (C-code)

- In ELDO a Hand-Written C-code Version of the Model exists
- Verilog-A Code: Simpler but less Efficient
  - ✓ Not always Efficiently handled by the Simulators
- Generally “Verilog-A + ADMS” and C-code have the same Functionality

Phenomena covered by EKV3.0 -- Associated Parameters

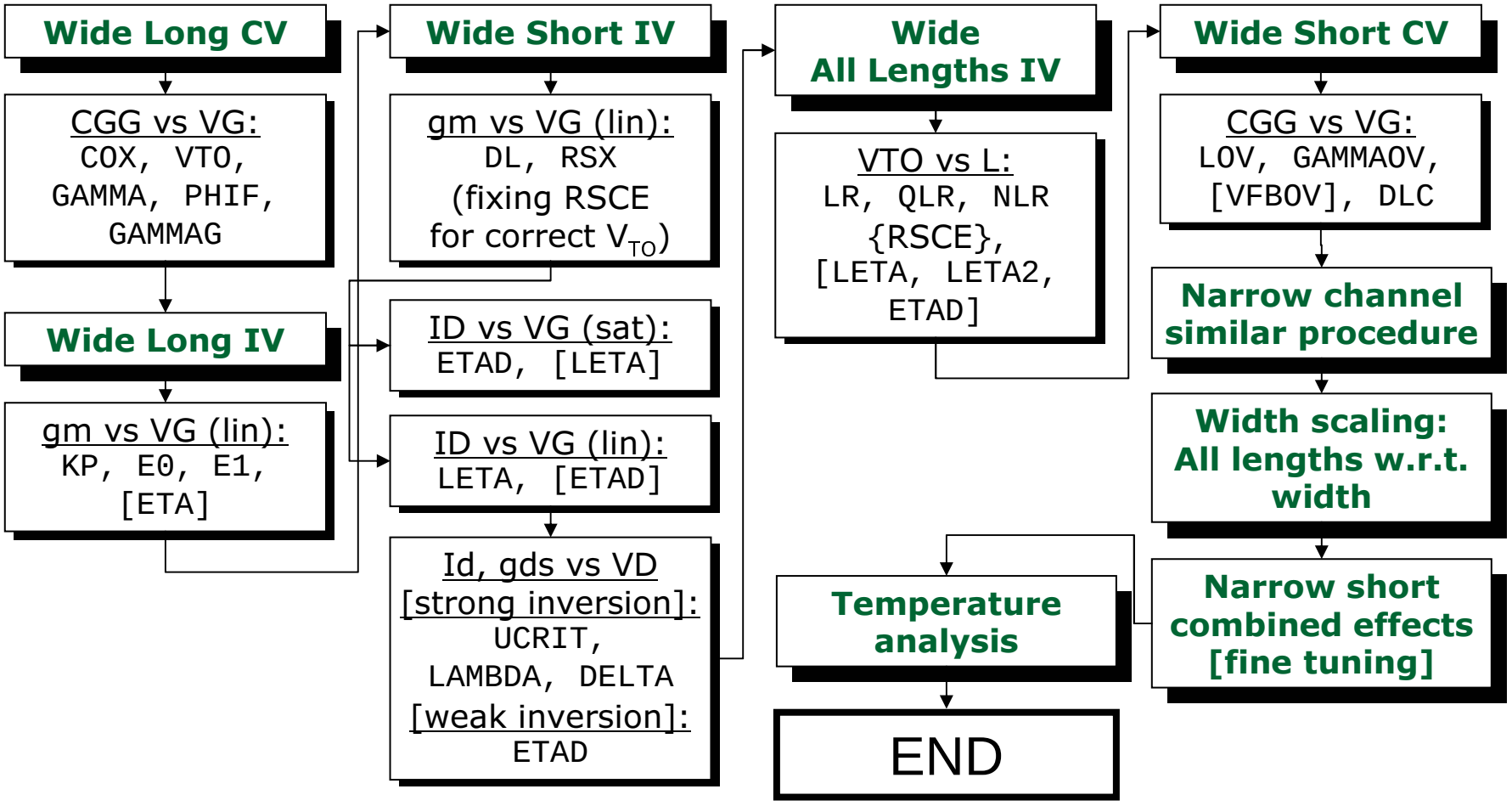
1/2

Modelled effect	Related Parameters / Comments
Physical Modelling of Charges Including Accumulation Region Polysilicon Depletion, Quantum Mechanical Effects	COX(TOX), PHIF, GAMMA(NSUB), VTO(VFB), GAMMAG(NGATE)
Bias-Dependent Overlap Capacitances	LOV, GAMMAOV(NOV), VFBOV
NQS	[Channel Segmentation]
RF Model External Sub-Circuit	[Appropriate Scaling of RG, RSUBs with W, L and NF]
Mobility (Reduction due to Vertical Field Effect) Surface Roughness-, Phonon-, Coulomb Scattering	KP(U0), E0, E1, ETA ZC, THC
Impact Ionization Current	IBA, IBB, IBN
Gate Current (IGS, IGD, IGB)	KG, XB, UB

Phenomena covered by EKV3.0 -- Associated Parameters

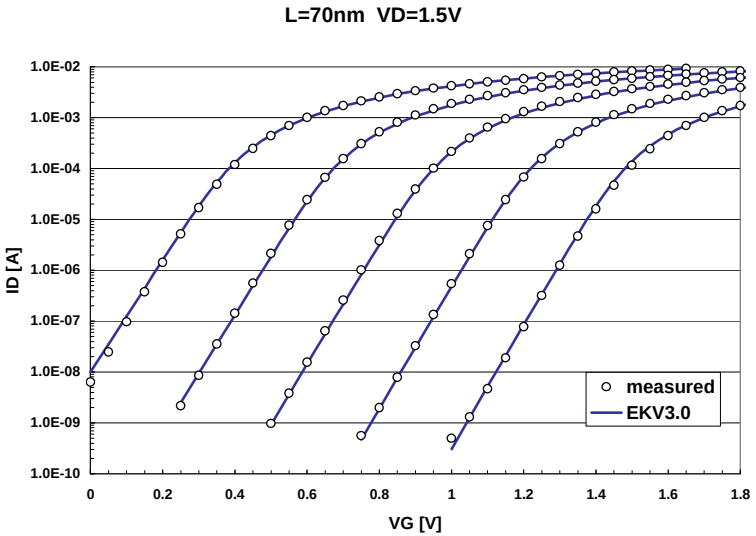
Modelled effect	Related Parameters / Comments
Longitudinal Field Effect Velocity Saturation, Channel Length Modulation	UCRIT(VSAT), LAMBDA, DELTA
Reverse Short Channel Effect	LR, QLR, NLR
Inverse Narrow Width Effect	WR, QWR, NWR
Drain Induced Barrier Lowering	ETAD, SIGMAD
Source and Drain Charge Sharing	LETA, {LETA2}, WETA
Halo/Pocket implant effects	LETA0
Edge Conduction	WEDGE, DGAMMAEDGE, DPHIEDGE
Geometrical Effects, Width scaling	Various Parameters (DL, WQLR, …)
Noise Flicker Noise, Short-Channel Thermal Noise, Induced Gate and Substrate Noise	AF, KF
Temperature Effects	Various Parameters
TOTAL	<100

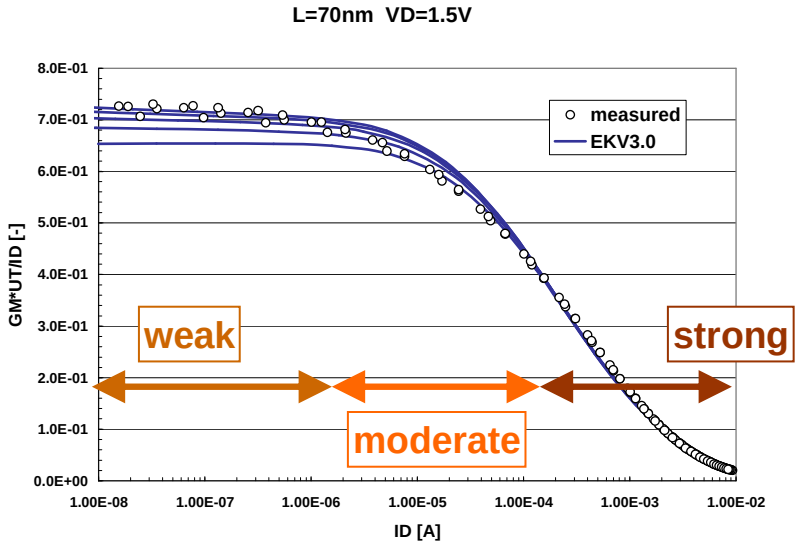
Basic Parameter Extraction Methodology



Short-Channel Characteristics

L = 70nm

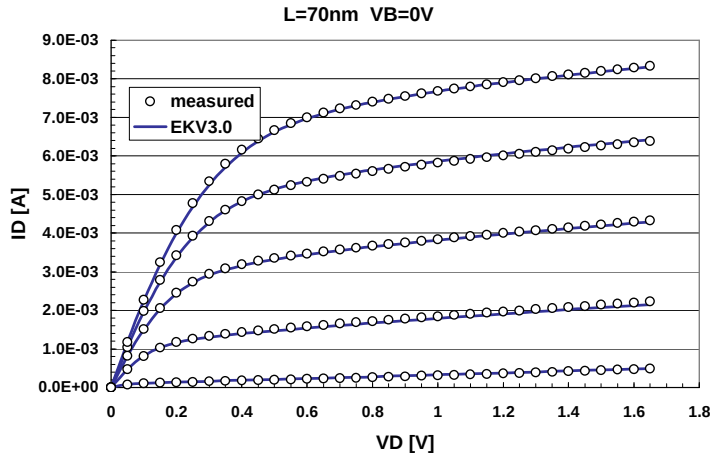


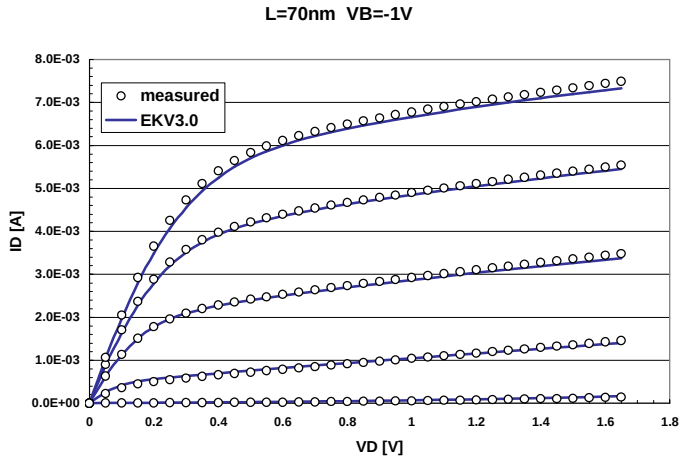


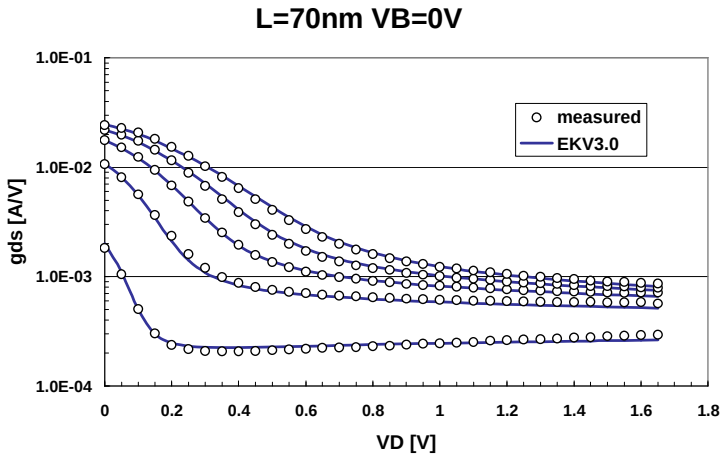
- Correct Weak & Moderate Inversion Behaviour
  - ✓ Smoothness and Correct Asymptotic Behaviour
  - ✓ Correct Weak Inversion Slope and DIBL Modeling
- Transconductance-to-Current Ratio vs. Drain Current (log. axis)

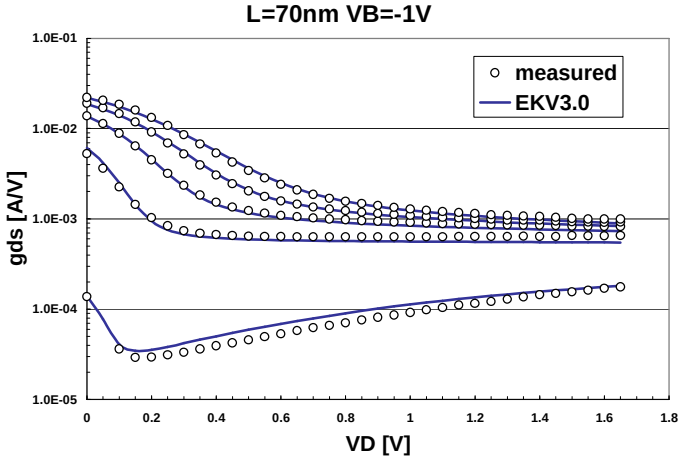
Short-Channel Output Characteristics

L = 70nm



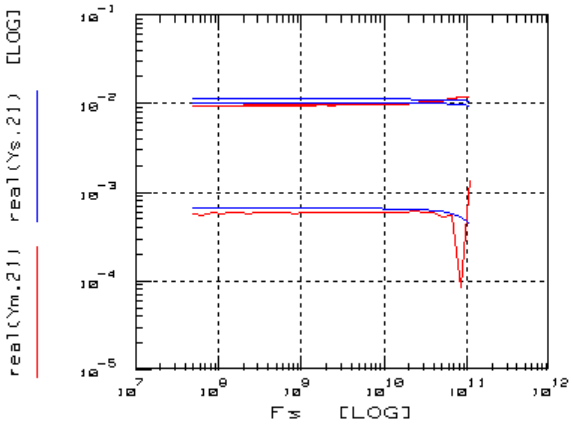


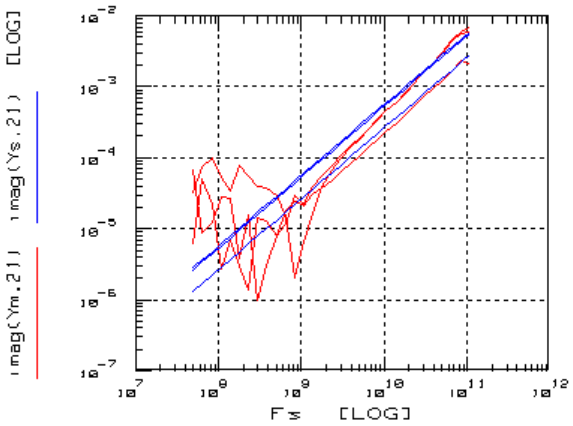




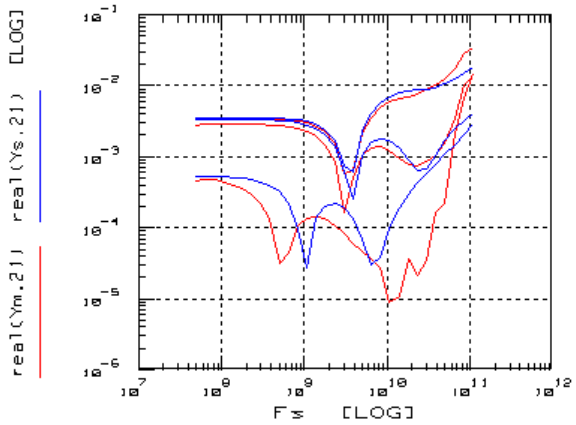
NQS Model @ RF *[Re(Y21), Im(Y21)]*

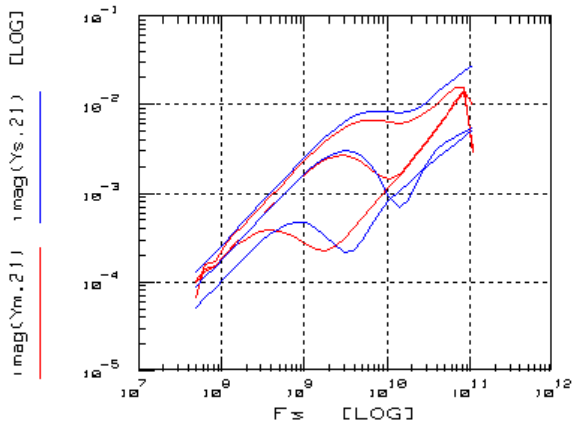
NMOS Lg=80nm





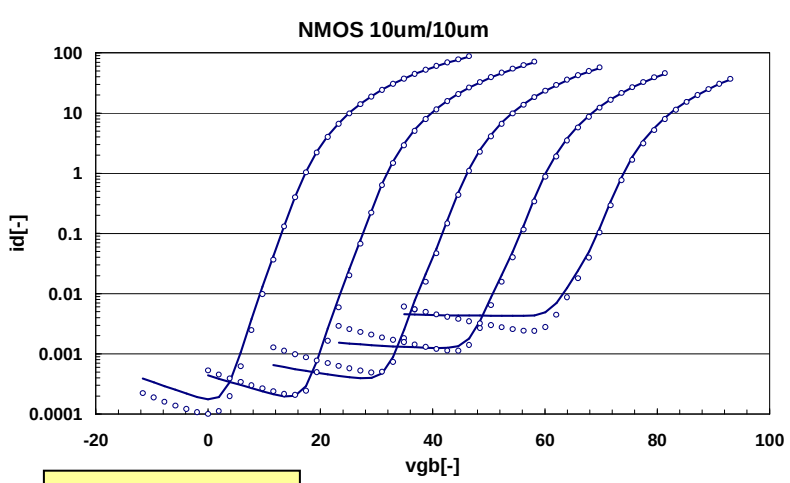
NMOS Lg=2um



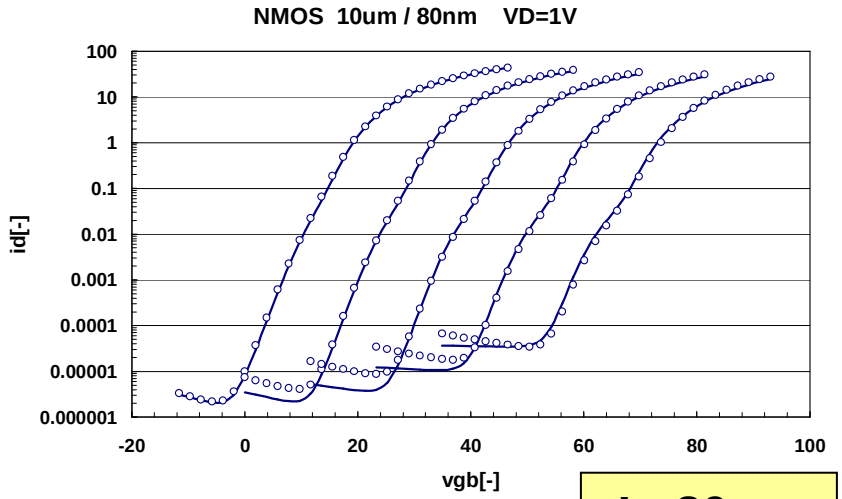


Multifinger Devices @ Various VG Values, Saturation

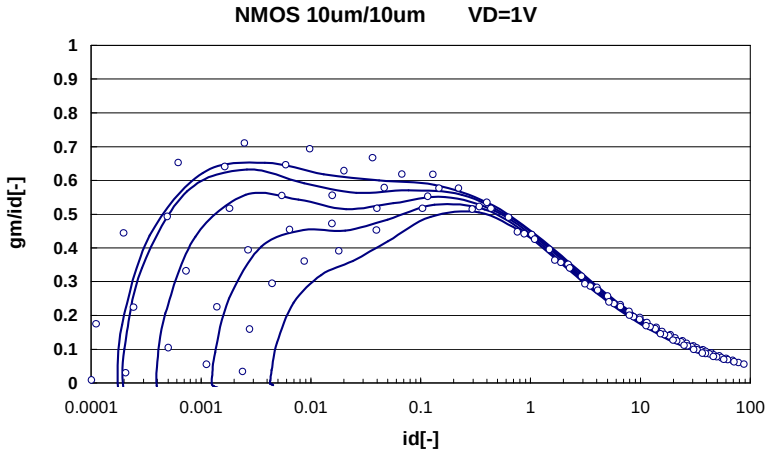
Edge Conduction Effect on I_D and g_m/I_D

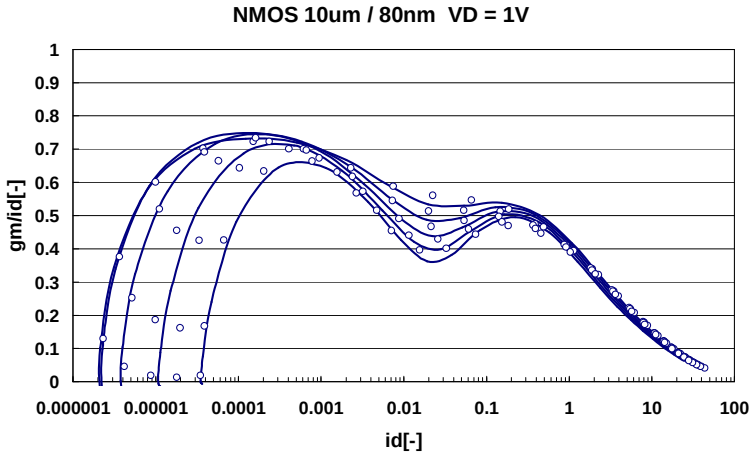


L=10um

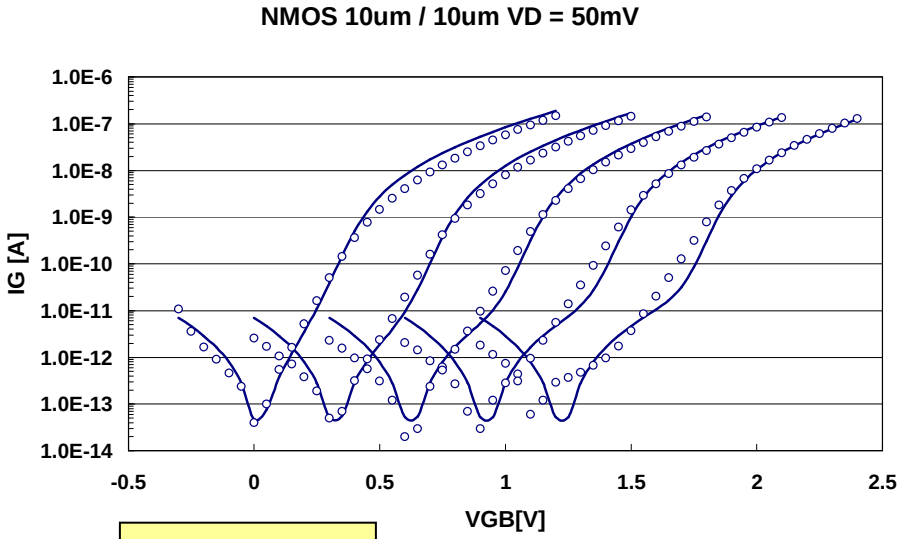


L=80nm

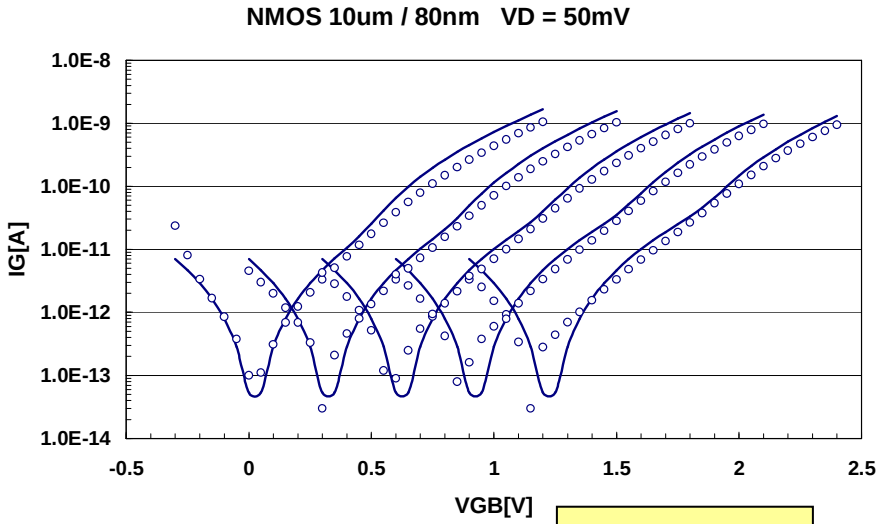




Gate Current & Edge Conduction



L=10um

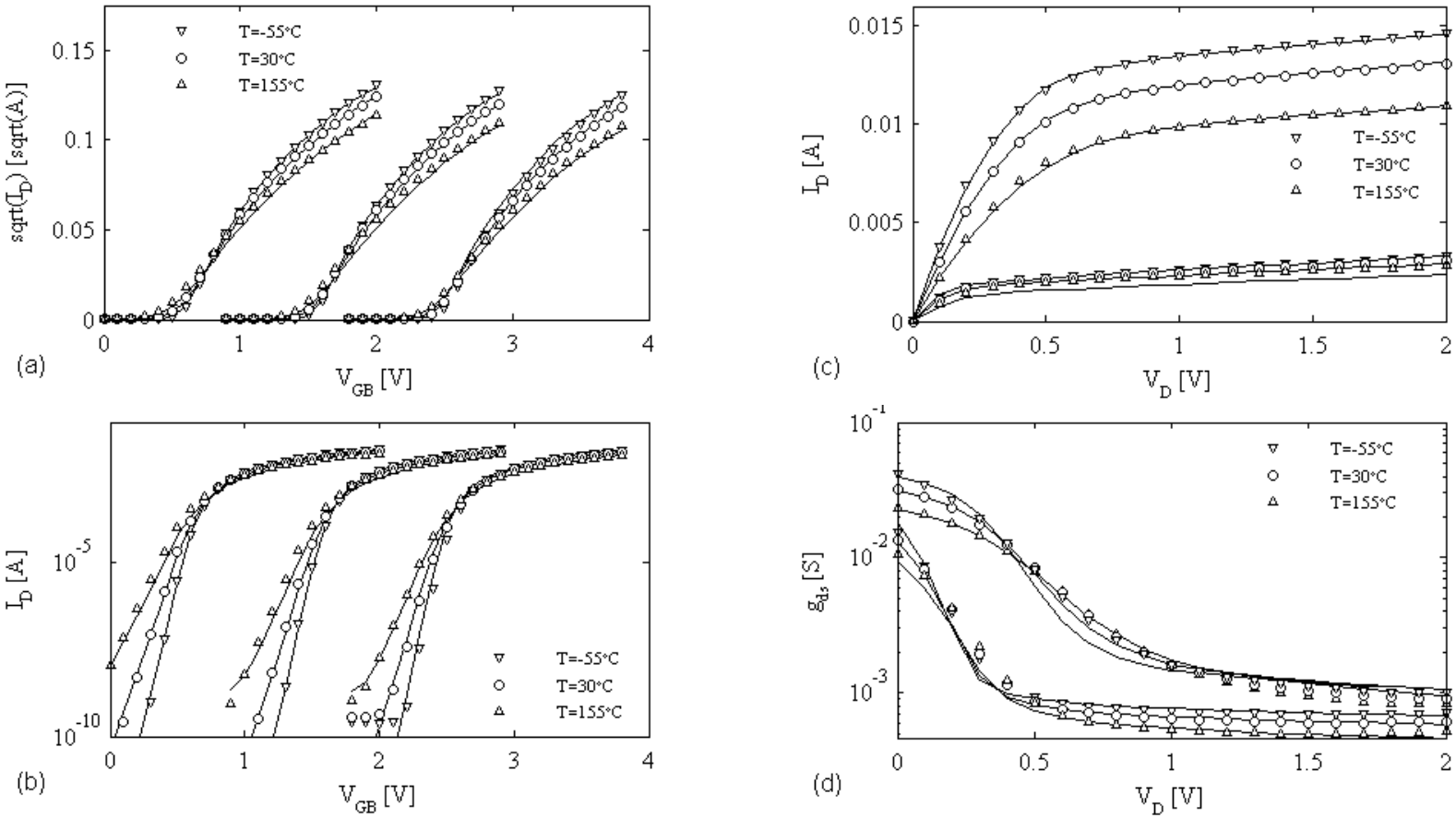


L=80nm

- Gate Current is also affected by Edge Conduction
- EKV3.0 gives reasonable fits to ID, gm/ID, IG even in case of presence of Edge Conduction Effect
- Edge Conduction affects gm/id dramatically in Weak-Moderate Inversion

Temperature Scaling

L = 150nm



- $I_D - V_G$ and I_D (g_{ds}) - V_D vs. Temperature

EKV3 and Industries

- TOSHIBA Semiconductors
  - ✓ 140nm
  - ✓ 110nm
  - ✓ 80nm
- Infineon Technologies
  - ✓ 120nm
  - ✓ 90nm
  - ✓ 65nm
- Cypress Semiconductors
  - ✓ 150nm
- Atmel Corporation
  - ✓ 350nm
  - ✓ 130nm
- AustriaMicroSystems
  - ✓ 350nm
  - ✓ 180nm
- XFAB
  - ✓ 350nm
- Various Co-Operations
  - ✓ Tektronix

Developments underway (EKV3.1)

- Vertical Non-Uniform Doping.
- Accounting for Carrier Heating/Velocity Saturation in Induced Gate Noise.
  - ✓ A. S. Roy and C. C. Enz, WCM 2006
- *Mobility Effect to Improve Flexibility for Short-Channel Back-Bias*
- *Output Conductance Effects in Long Channel Halo/Pocket Implanted Devices*
- *Layout Dependent Stress Effects*
- …
- EKV3.1 Release expected: 2007.

Summary

- EKV3.0: a design-oriented, charge-based, compact model for Next Generation CMOS
  - ✓ Moderate and Weak Inversion, Analog/RF IC Design
  - ✓ Validated on Various CMOS Technologies to 65nm.
    - Used for Commercial IC Design.
  - ✓ Developed in Verilog-A
    - Verilog-A Code is Available to CAD Vendors.
    - Specific Simulators require Specific XML interface in ADMS
    - MOS Design Kits developed.
  - ✓ Implementation ongoing for:
    - ELDO, Smash, GoldenGate, …
    - Spectre, HSPICE, …

Thank you very much
for your time and attention