



The PSP compact MOSFET model

An update

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Affiliations



<http://pspmodel.asu.edu>
http://www.nxp.com/Philips_Models/mos_models/psp/



Outline

- ▶ History & overview
- ▶ DC verification on 65nm technology
- ▶ Symmetry and distortion
- ▶ Non-quasi static effects
- ▶ Summary & references



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History

- ▶ April 2005: First PSP version (100.0) released. Created from
 - MOS Model 11 (Philips)
 - SP (Penn State)
- ▶ December 2005: CMC elects PSP as “next generation compact MOSFET model” (i.e. successor of BSIM3/4)
- ▶ June 2006: First CMC-standardized version (PSP 102.0) was released
- ▶ Future: PSP extended to complete family of models
 - Bulk CMOS
 - Varactor
 - PD-SOI
 - FD-SOI
 - FinFETs
 - ...

Model overview

- ▶ PSP is a **surface potential based** compact MOSFET model, suitable for digital, analog and RF design
 - non-uniform lateral/vertical doping
 - field-dependent mobility
 - velocity saturation
 - conductance effects (CLM, DIBL, etc.)
 - series-resistance
 - short-channel effects (incl. RSCE)
 - narrow-width effects
 - gate poly-depletion
 - quantum-mechanical corrections
- overlap capacitances (ψ_s -based)
- impact ionization current
- **gate leakage current**
- gate-induced drain/source leakage (GIDL, GISL)
- **junction diode I-V and C-V (forward and reverse)**
- diode reverse breakdown
- **noise (1/f, thermal, induced gate and shot noise)**
- **non-quasi-static effects**
- gate and bulk resistances
- STI stress effect

See also MOS-AK 2005

Update PSP 102.0

- ▶ Changes PSP 100.0 → 102.0
 - Binning
 - Improved Gummel symmetry (modified CLM-model and V_B -clamping)
 - Replaced lateral gradient factor
 - More flexible geometry scaling
 - Improved mobility model (CS, FETA, scaling)
 - Improved forward bulk-bias behavior
 - BSIM-like instance parameters for JUNCAP2 (AS, AD, PS, PD)
 - Several minor improvements, bug fixes, and maintenance
 - October 2006: PSP 102.1 includes first C-implementation of NQS-model
- ▶ Partly based on useful feedback by Jazz, Infineon, Freescale, STm, RFMD, Analog Devices, ...

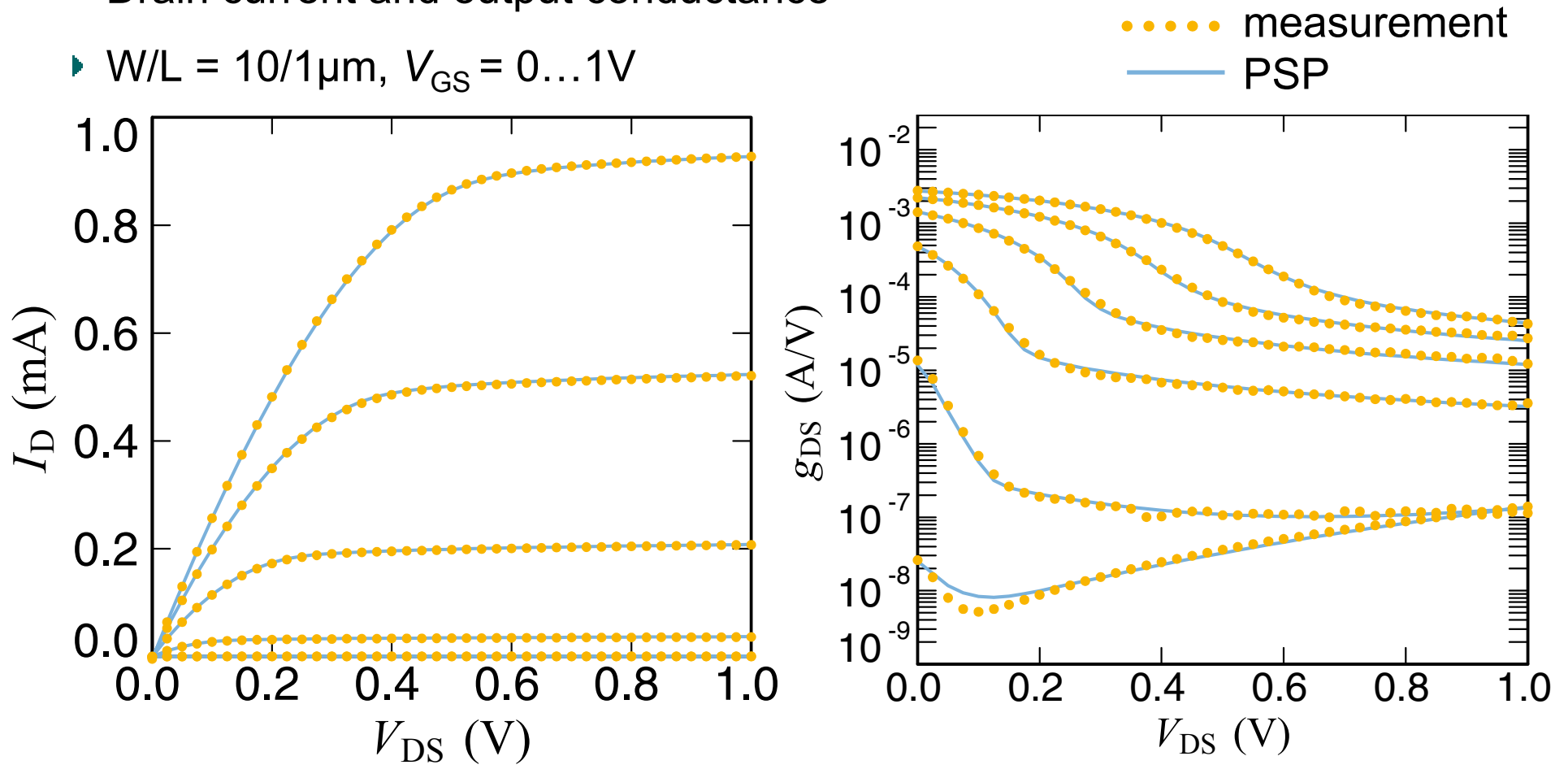
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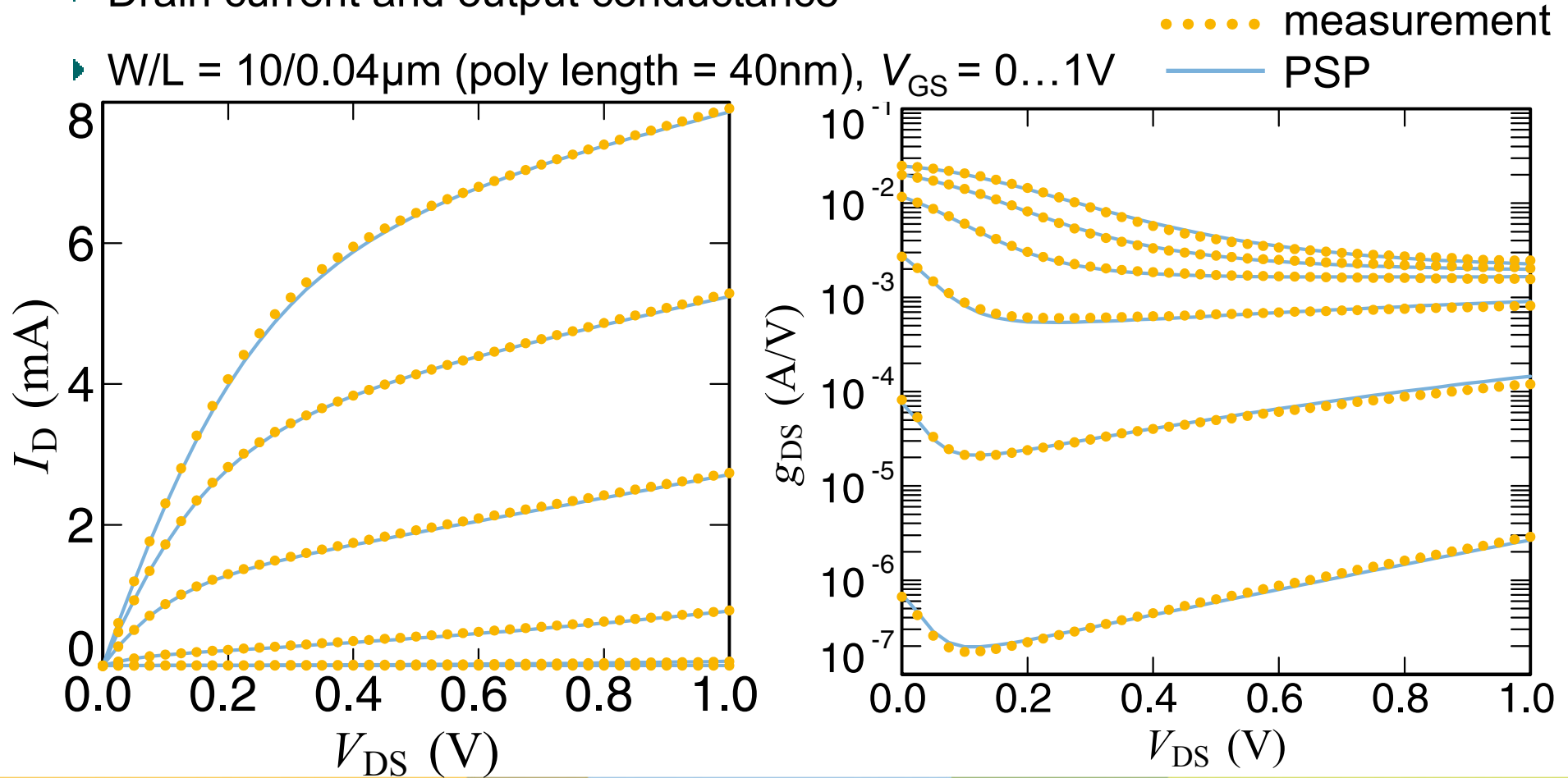
Long channel (65nm technology)

- ▶ Drain current and output conductance
- ▶ $W/L = 10/1\mu\text{m}$, $V_{GS} = 0 \dots 1\text{V}$



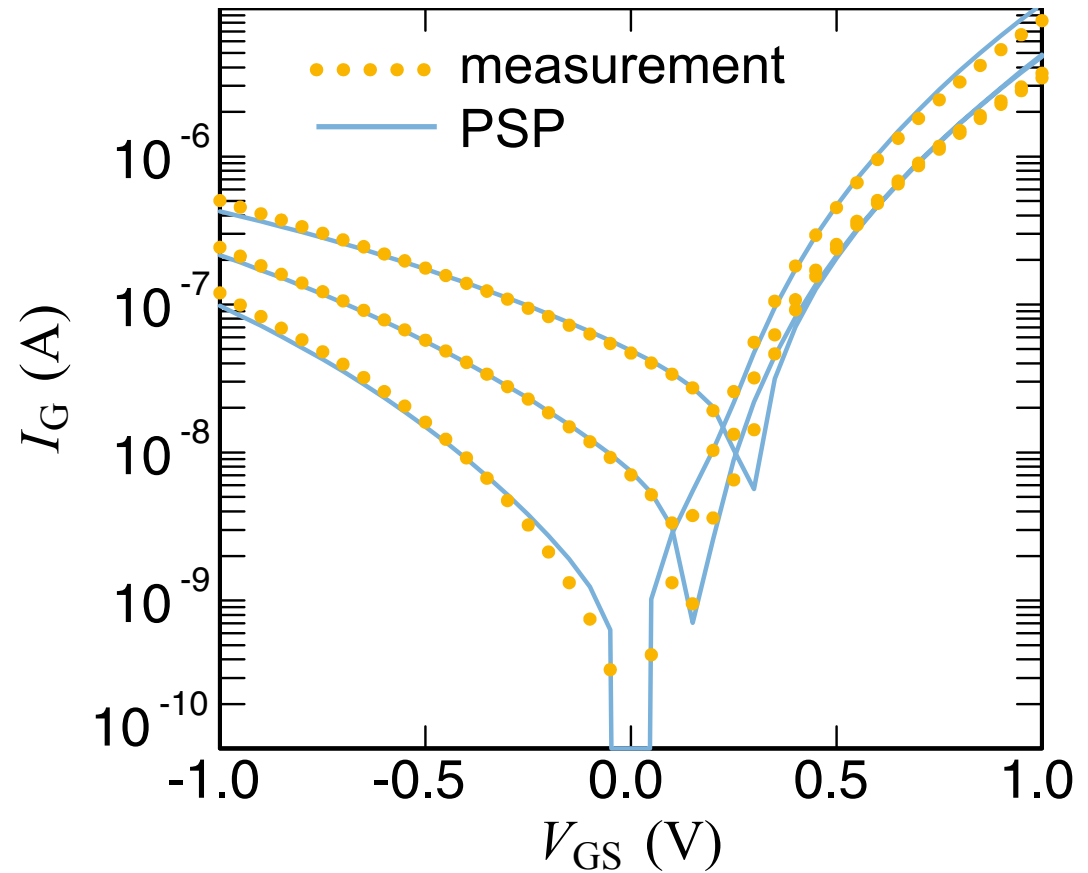
Short channel (65nm technology)

- ▶ Drain current and output conductance
- ▶ $W/L = 10/0.04\mu\text{m}$ (poly length = 40nm), $V_{GS} = 0 \dots 1\text{V}$



Gate current (65nm technology)

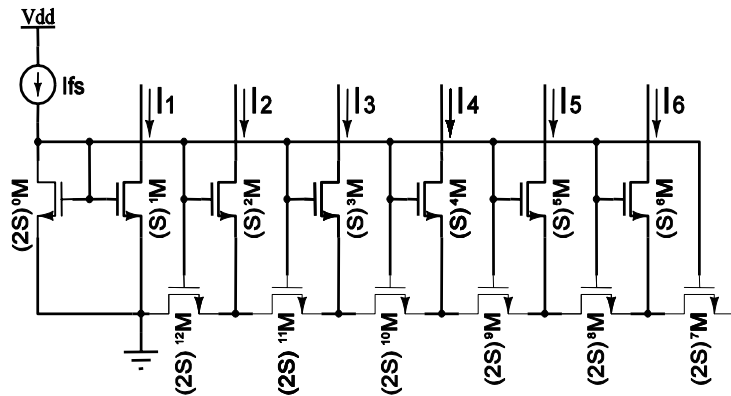
- ▶ Gate current
- ▶ $W/L = 10/1\mu\text{m}$, $V_{DS} = 0 \dots 1\text{V}$



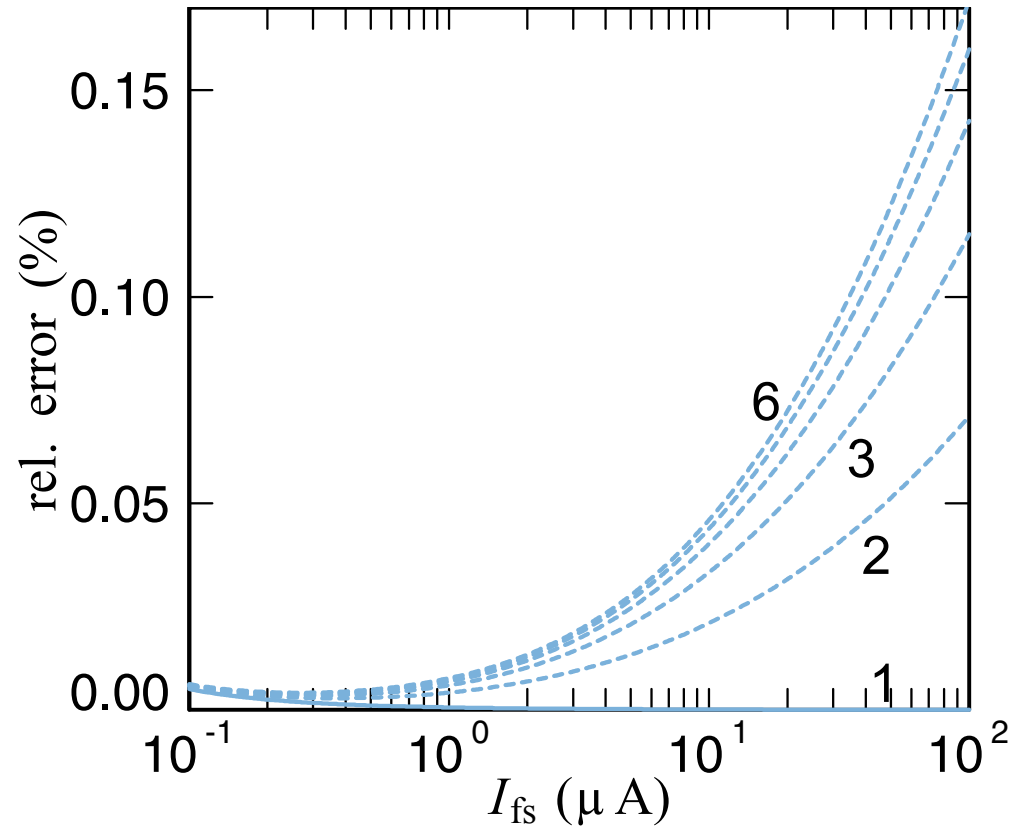
PSP model has been verified to successfully describe various 90nm, 65nm and 45nm processes

R2R-circuit

- ▶ Benchmark test for quality of integral along channel $I_{DS} = -\frac{W}{L} \int_{V_{SB}}^{V_{DB}} \mu \cdot q_{inv} \cdot dV$
- ▶ Ideal long channel model



$$\text{rel. error} = \frac{2^{n-1} \cdot I_n - I_{fs}}{I_{fs}}$$



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Gummel symmetry (i)

- ▶ CMOS devices are symmetric w.r.t. source/drain
- ▶ Imposed on the model by applying **source/drain interchange**

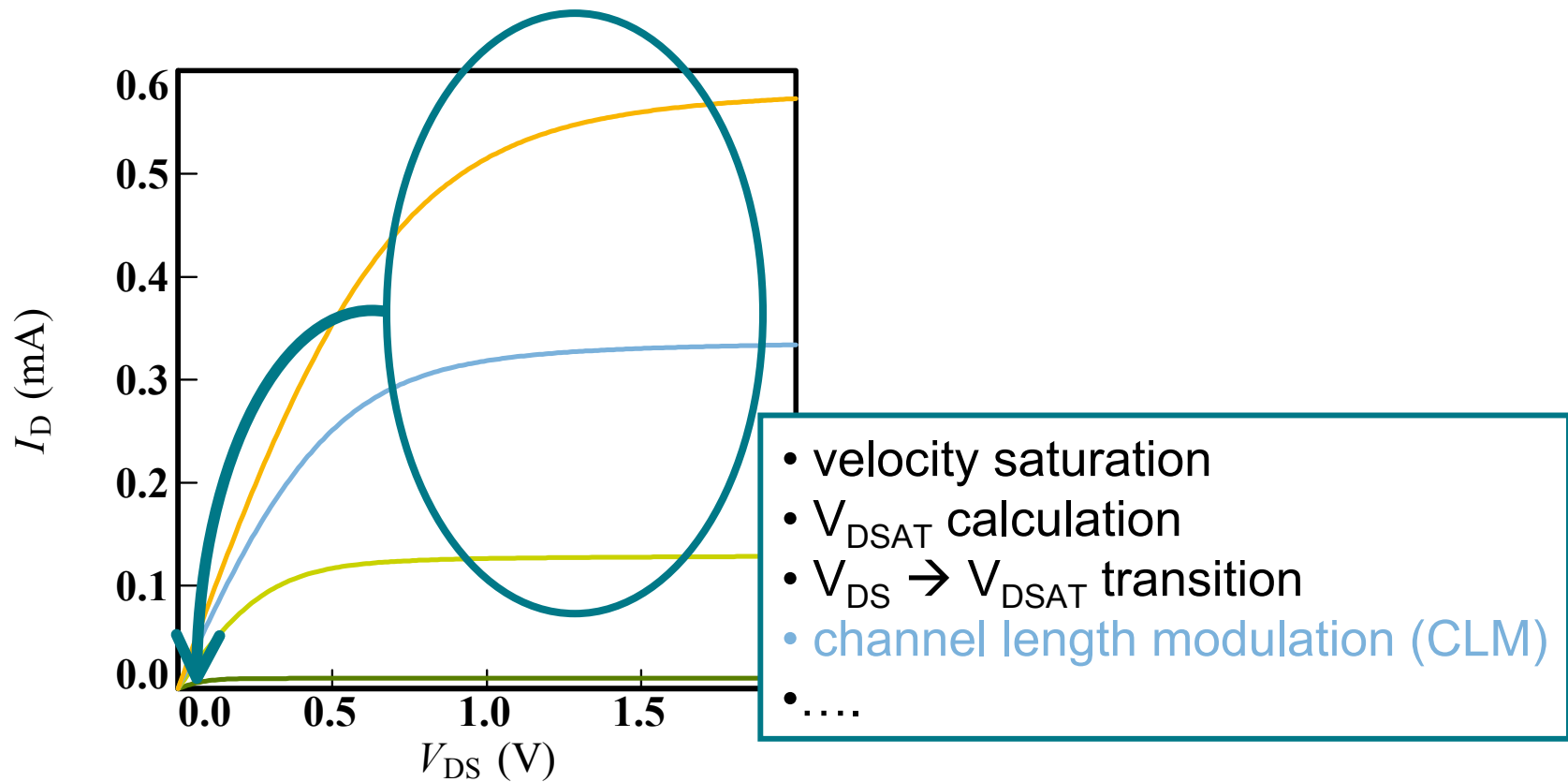
$$V_{DS} \geq 0 : I_{DS}(V_D, V_G, V_S, V_B) = I_{DS}^+(V_D, V_G, V_S, V_B)$$

$$V_{DS} < 0 : I_{DS}(V_D, V_G, V_S, V_B) = -I_{DS}^+(V_S, V_G, V_D, V_B)$$

- ▶ Guaranteeing a smooth connection at $V_{DS}=0$ is **nontrivial**

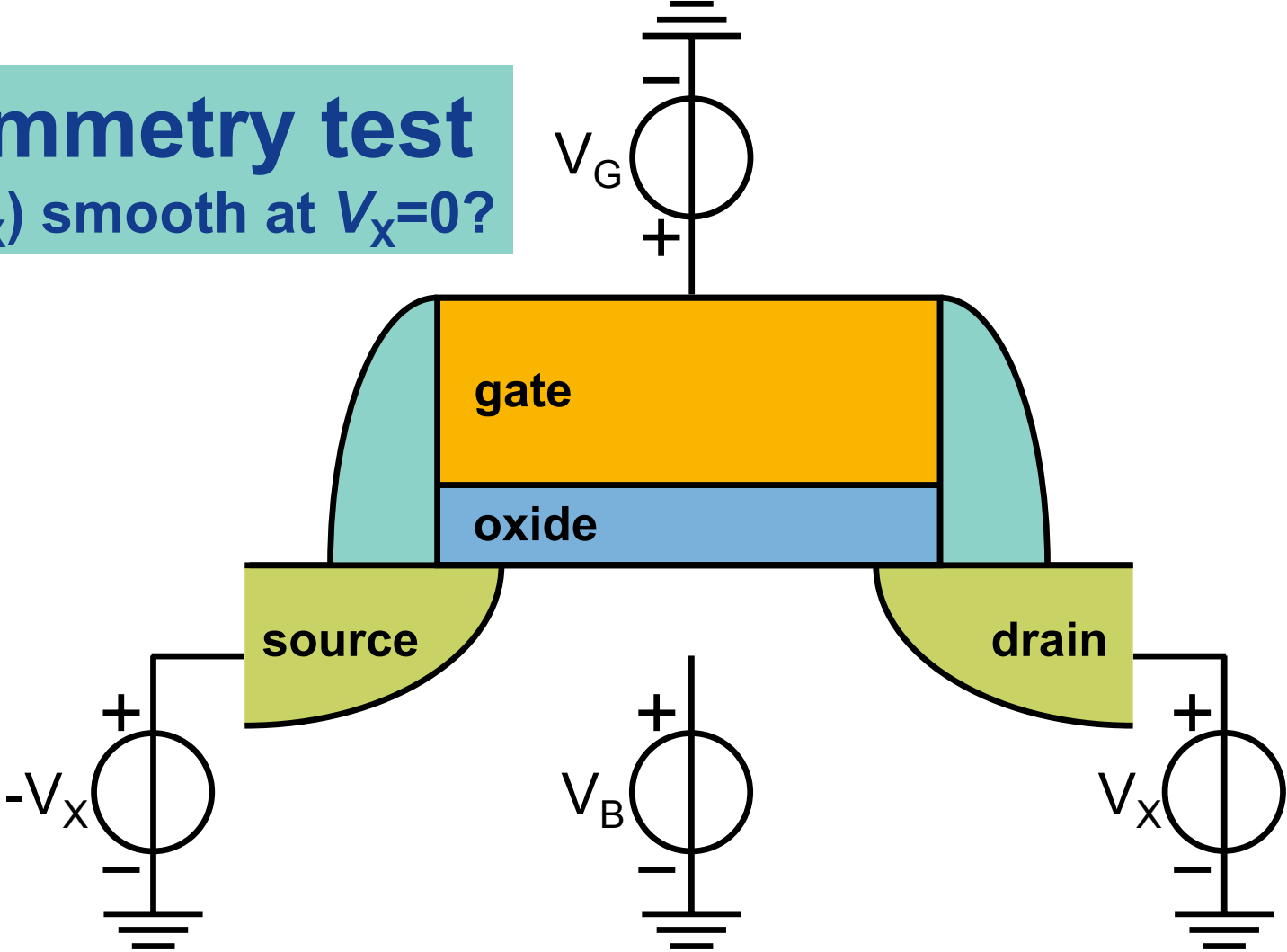
Gummel symmetry (ii)

- ▶ Why is Gummel symmetry nontrivial to achieve?

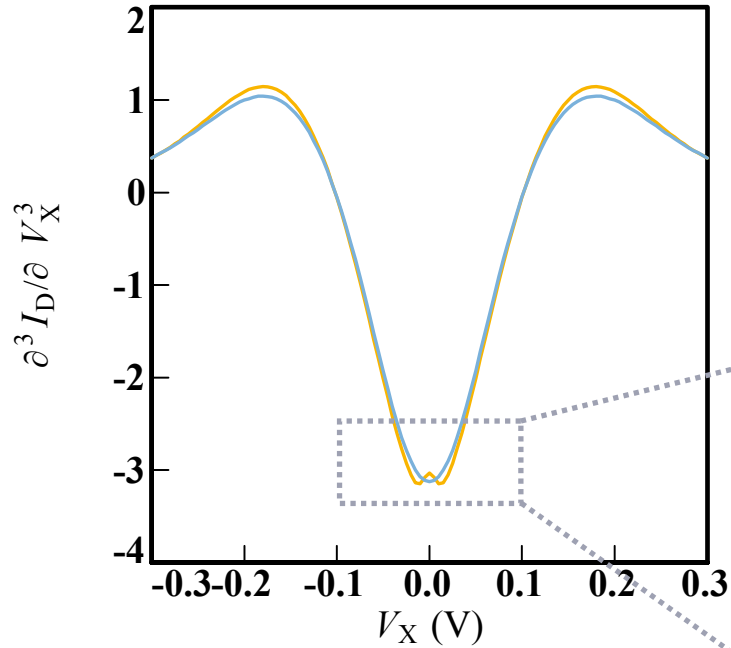


Gummel symmetry (iii)

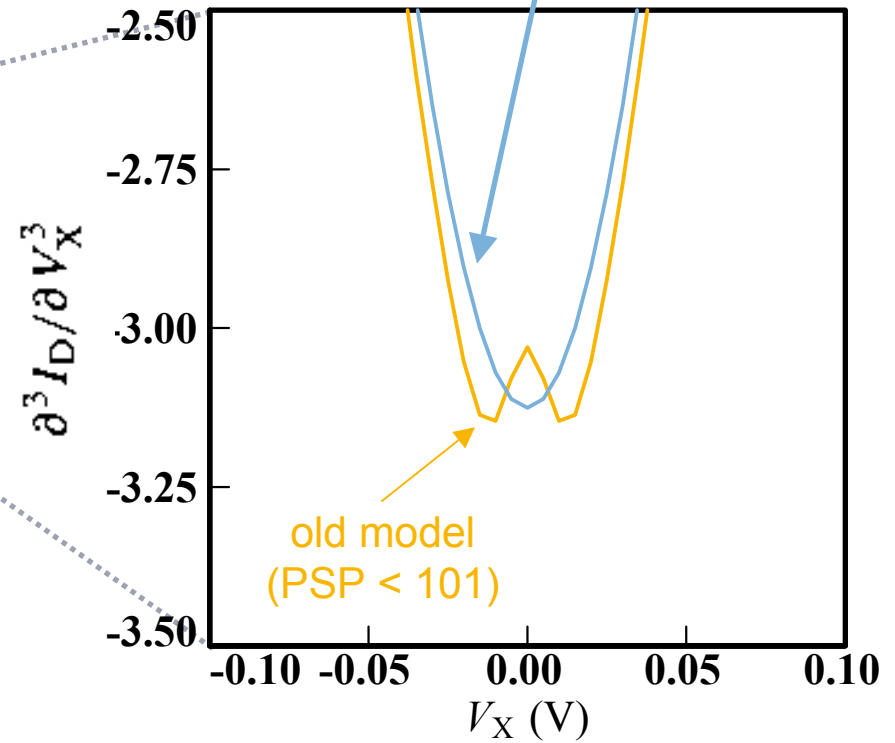
Symmetry test
 $I_D(V_X)$ smooth at $V_X=0$?



Gummel symmetry (iv)

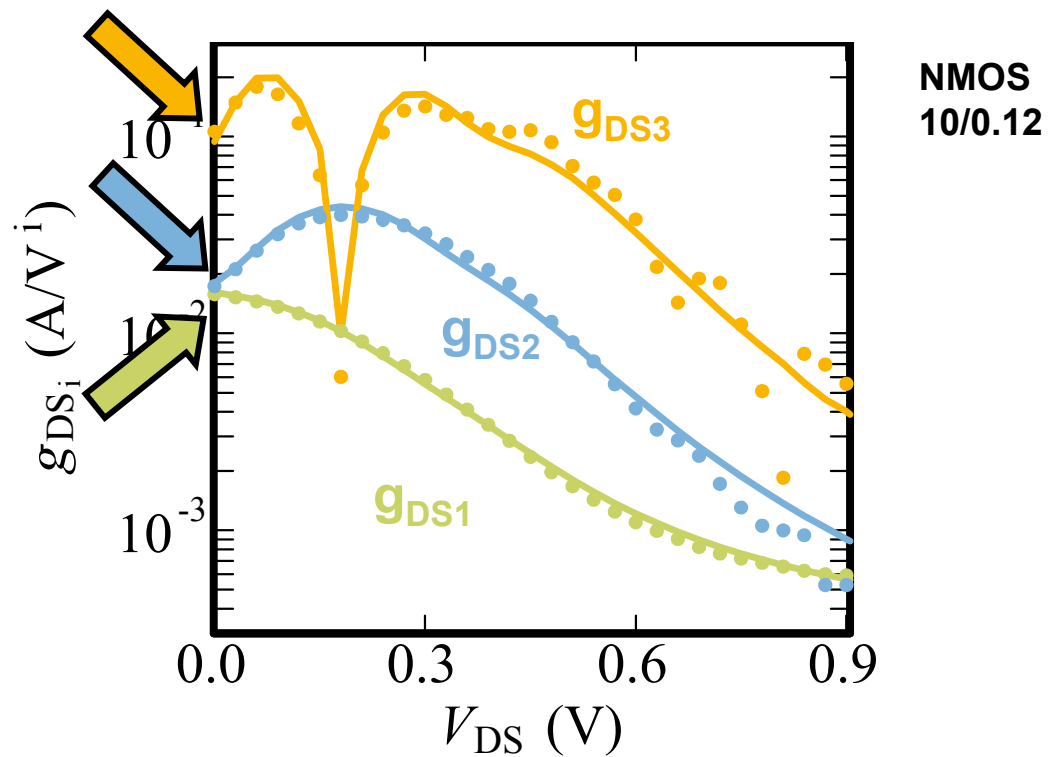


improved CLM model
(PSP102)



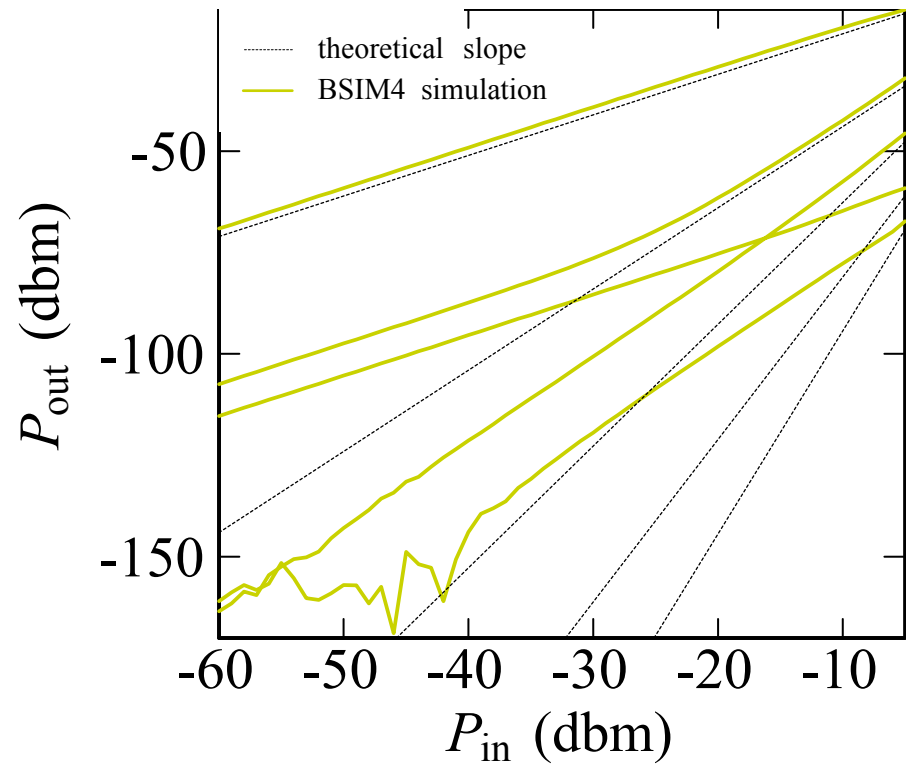
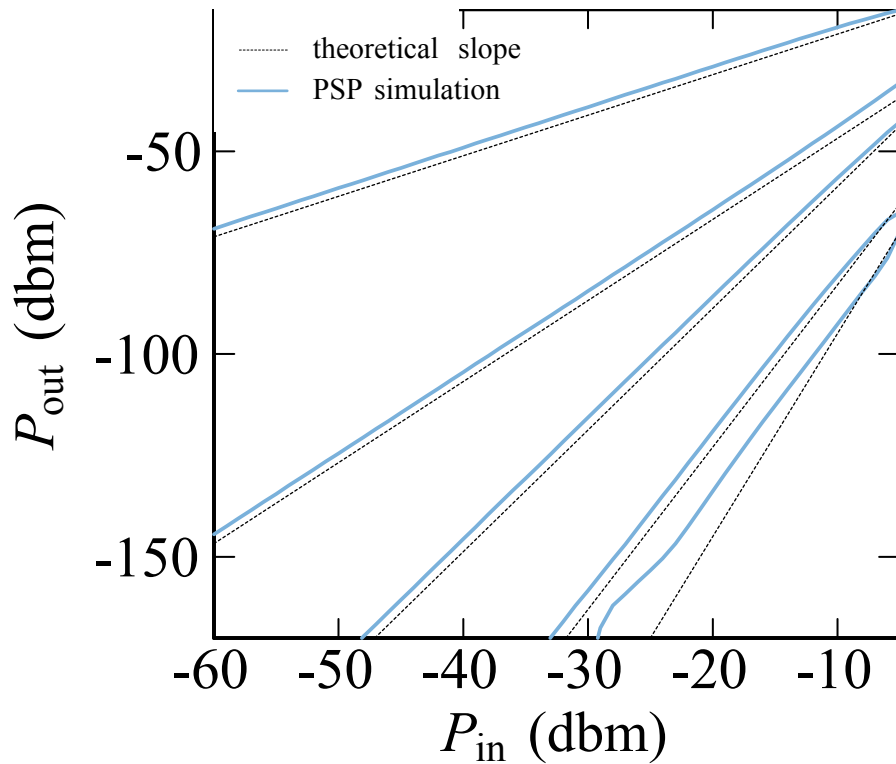
Distortion (i)

- ▶ Gummel symmetry is important for RF-CMOS circuit design (distortion)
- ▶ PSP gives excellent description up to at least 3rd order derivatives



Distortion (ii)

- ▶ Two-tone intermodulation distortion simulation (1.8 and 1.9 GHz)
- ▶ $V_{GS}=1V$, $V_{DS}=V_{SB}=0V$, $W/L=5/0.3\mu m$ NMOS, 90nm technology)



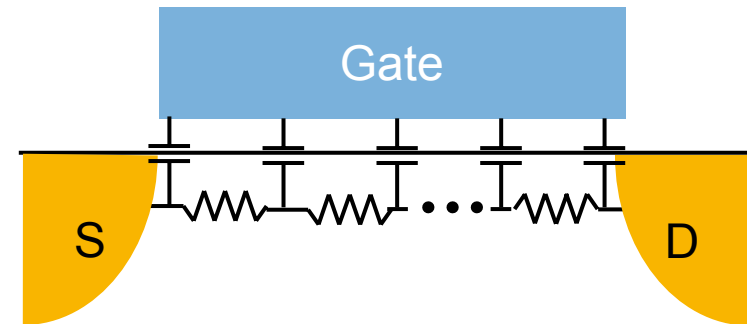
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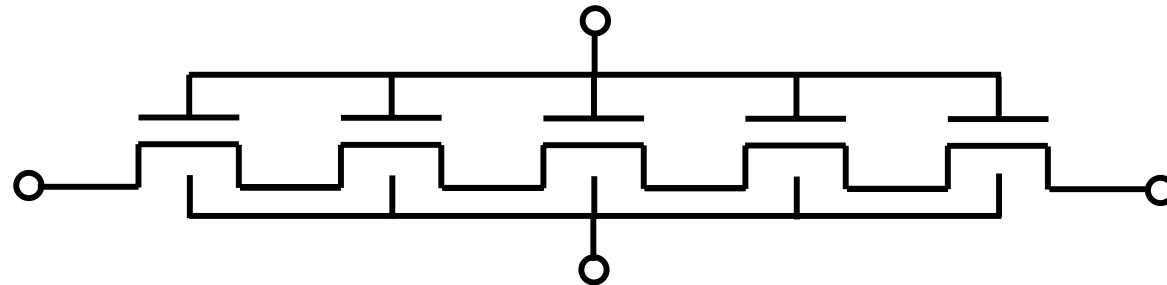


PSP NQS model (i)

- ▶ Non-quasi static effects:
it takes **time** for charge to move through the channel
 - distributed effect
 - “memory” effect
 - continuity equation: $dQ/dt \propto dI/dx$



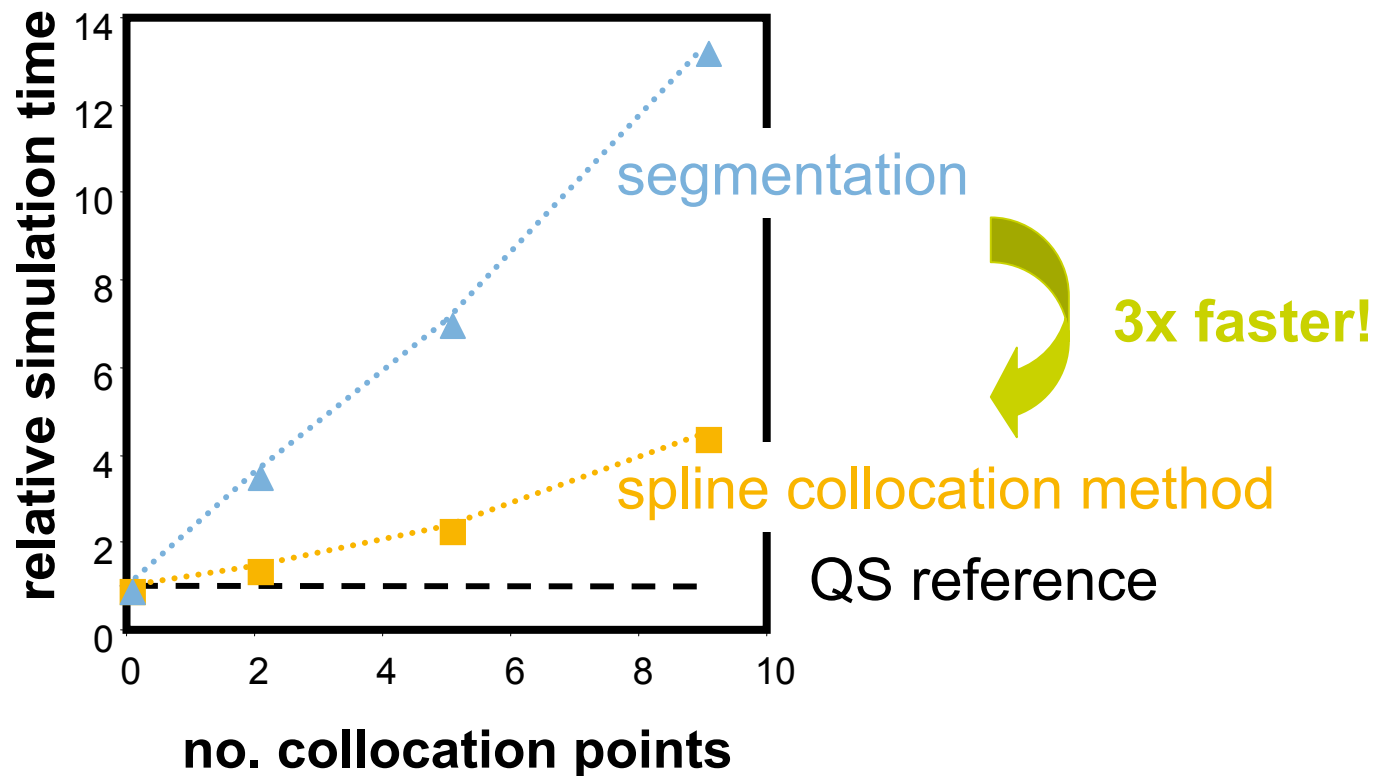
- ▶ Previously: channel segmentation (still good benchmark!)



- ▶ PSP: spline collocation method (adopted from SP model)
- ▶ No parameter fitting!

PSP NQS model (ii)

- ▶ Same physics as segmentation model, but much faster:



PSP NQS model (iii)

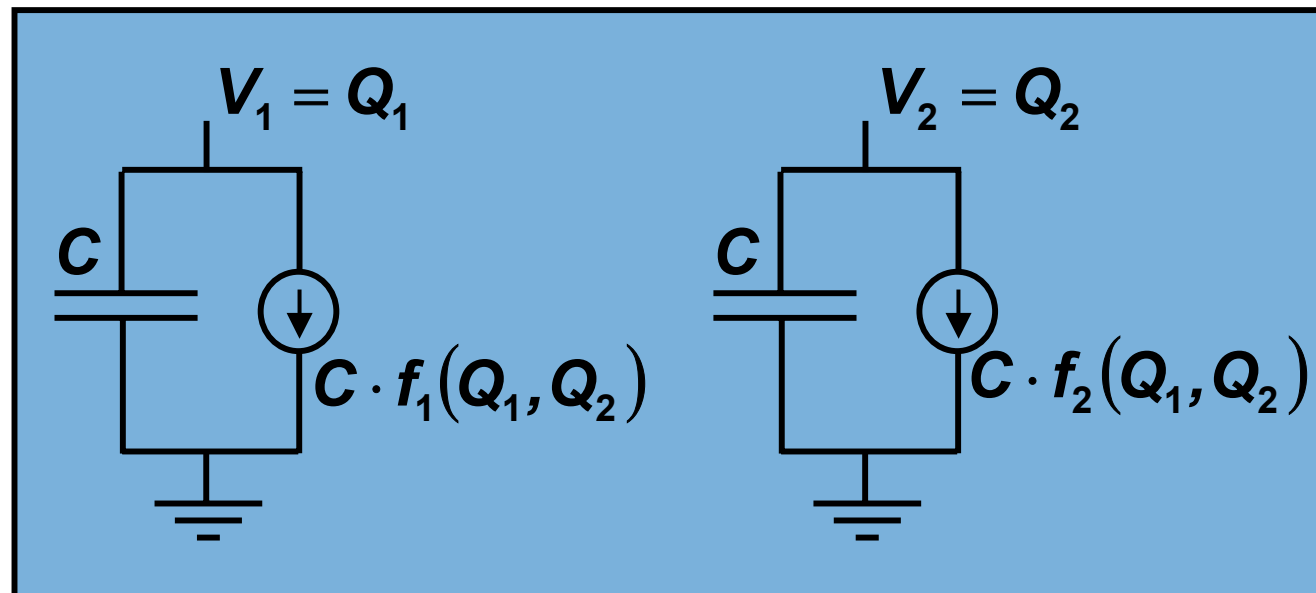
current continuity equation + spline approximation

→ system of (coupled) ordinary differential equations

$$\frac{dQ_k}{dt} = -f_k(Q_1, \dots, Q_N) \quad Q_k: \text{charge densities along channel}$$

implemented as sub-circuits, solved by circuit simulator:

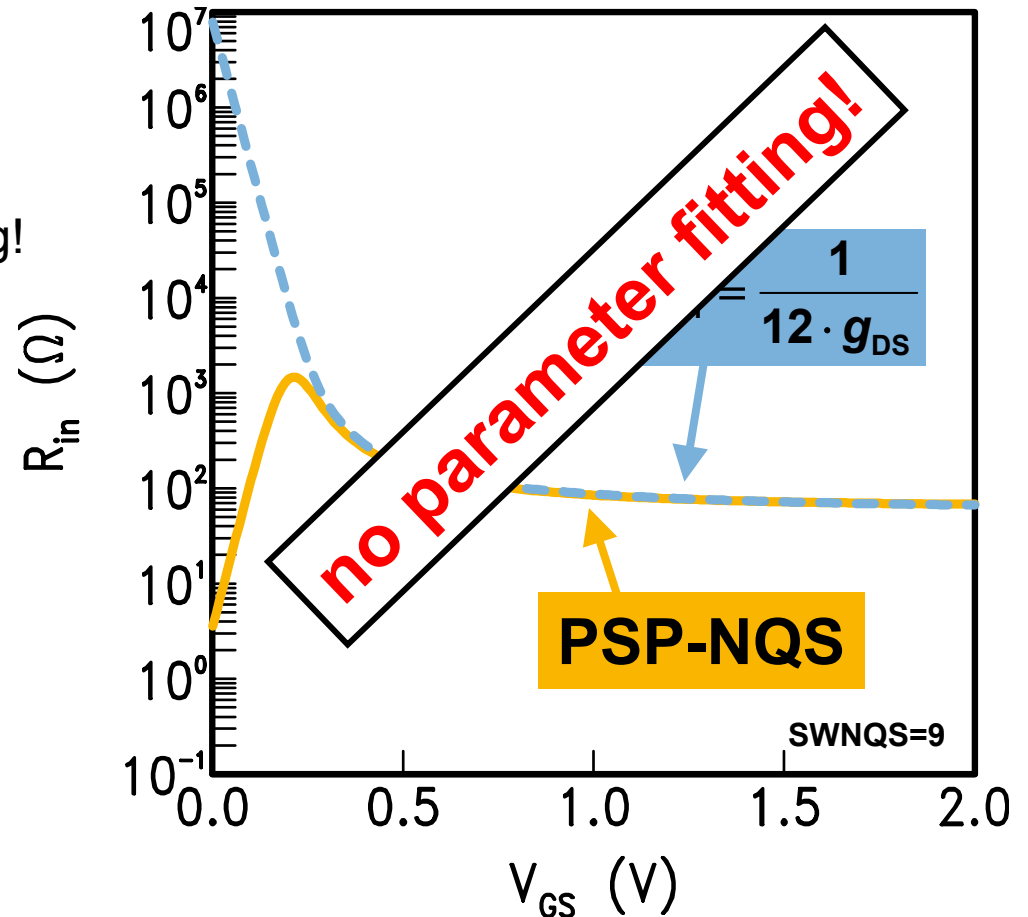
example:
($N = 2$)



PSP NQS model (iii)

- ▶ Does model preserve basic physics?
- ▶ NQS model sanity check
 - Important for varactor modeling!
- ▶ Basic NQS physics
 - strong inversion
 - $V_{DS}=0$
 - $f \rightarrow 0$

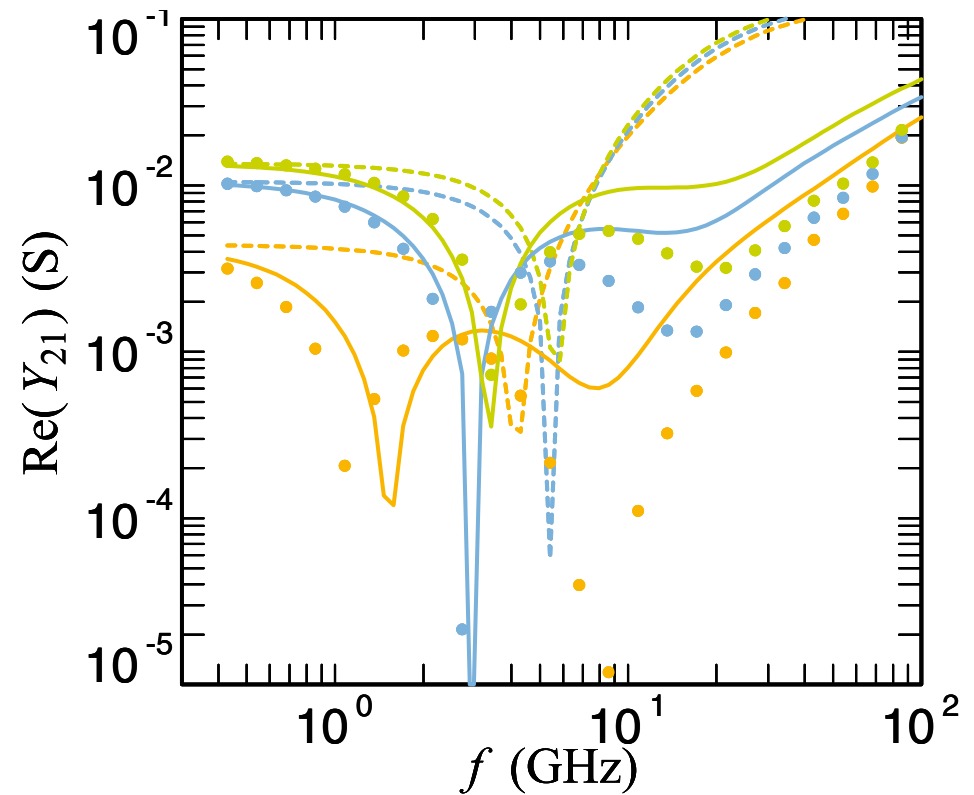
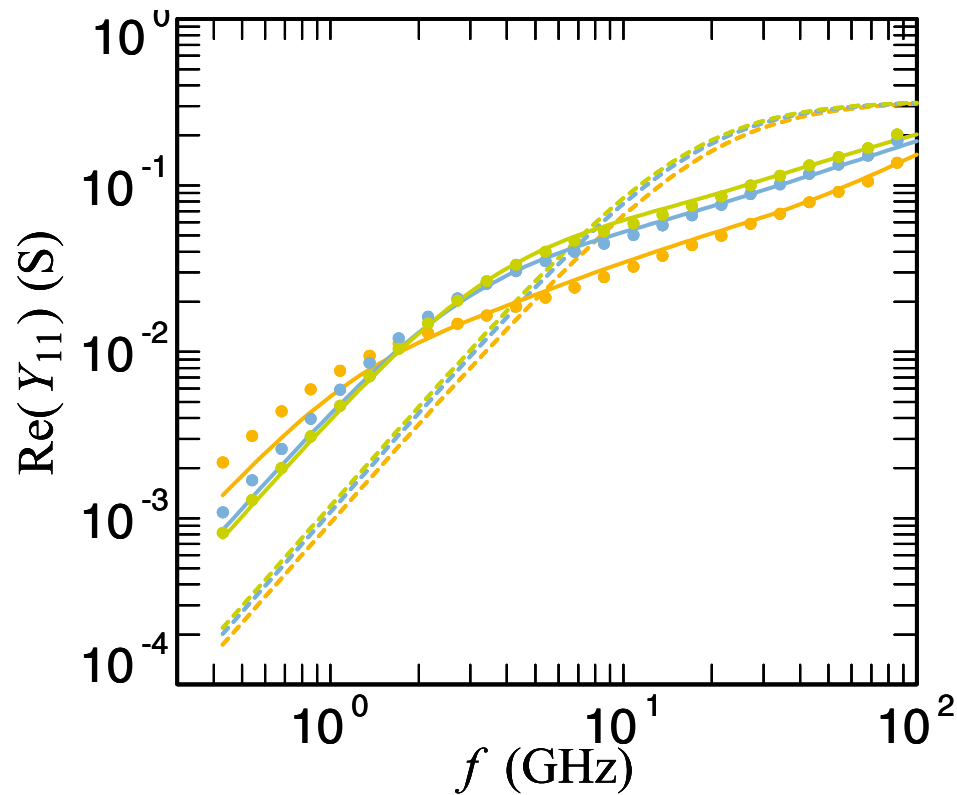
$$R_{in} = \frac{1}{12 \cdot g_{DS}}$$



PSP NQS model (v)

- ▶ Y-parameter measurements
- ▶ NMOS $W/L=120/3\mu\text{m}$, $V_{DS} = 1.5\text{V}$, $V_{GS} = 0.5, 1.0, 1.5\text{V}$

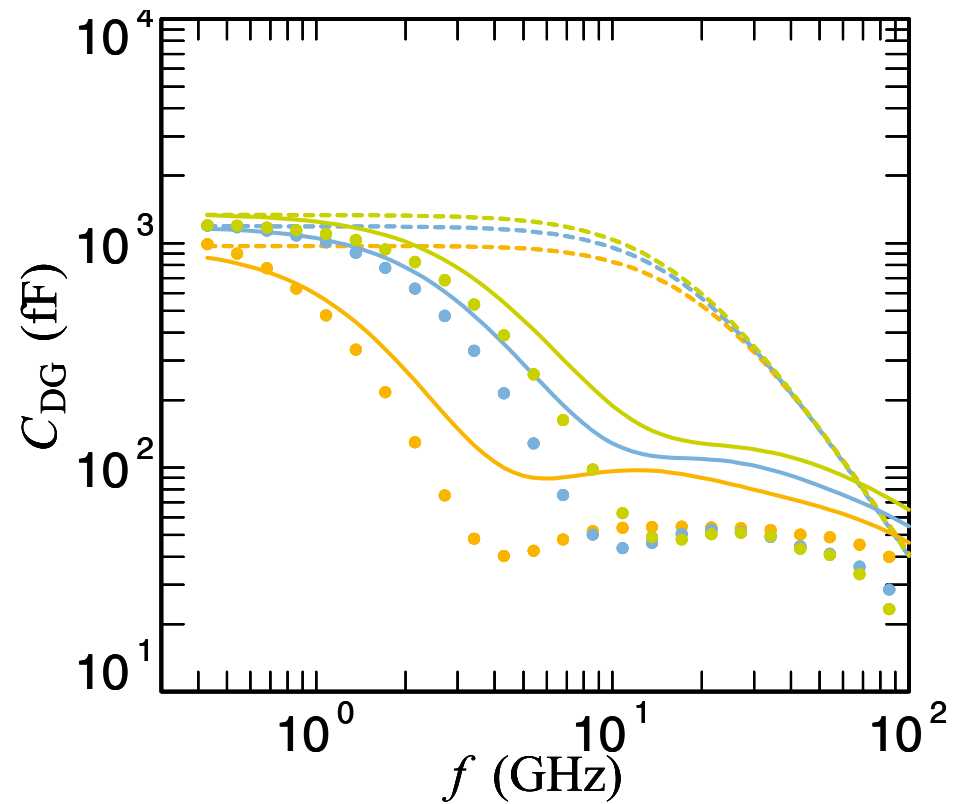
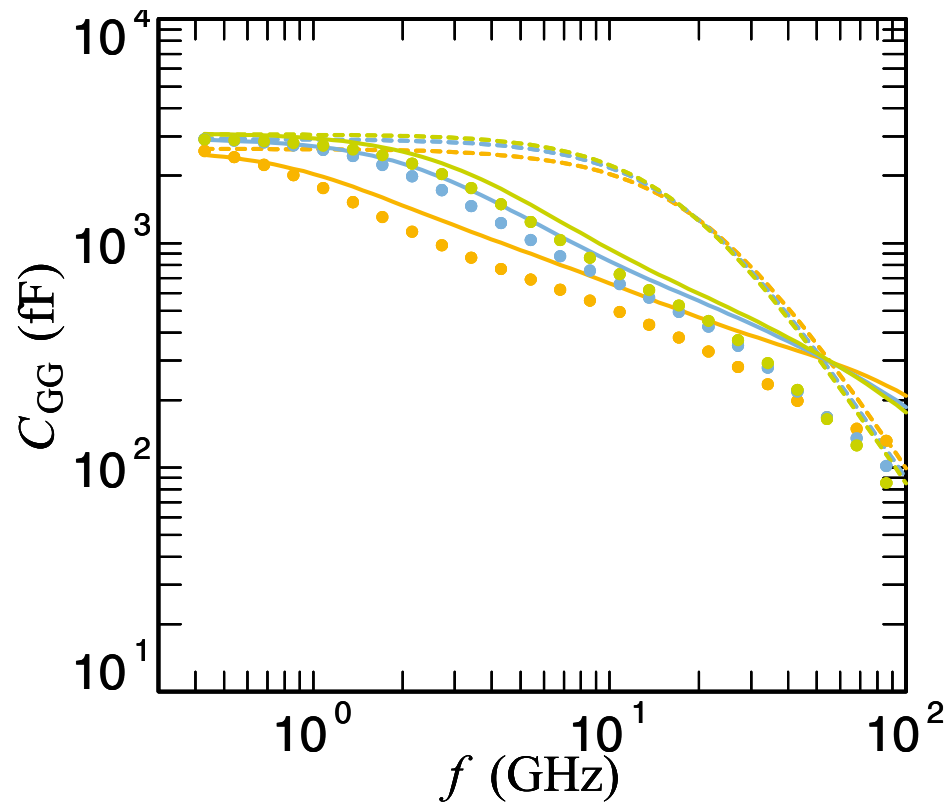
..... measurement
----- PSP quasi-static
———— PSP NQS



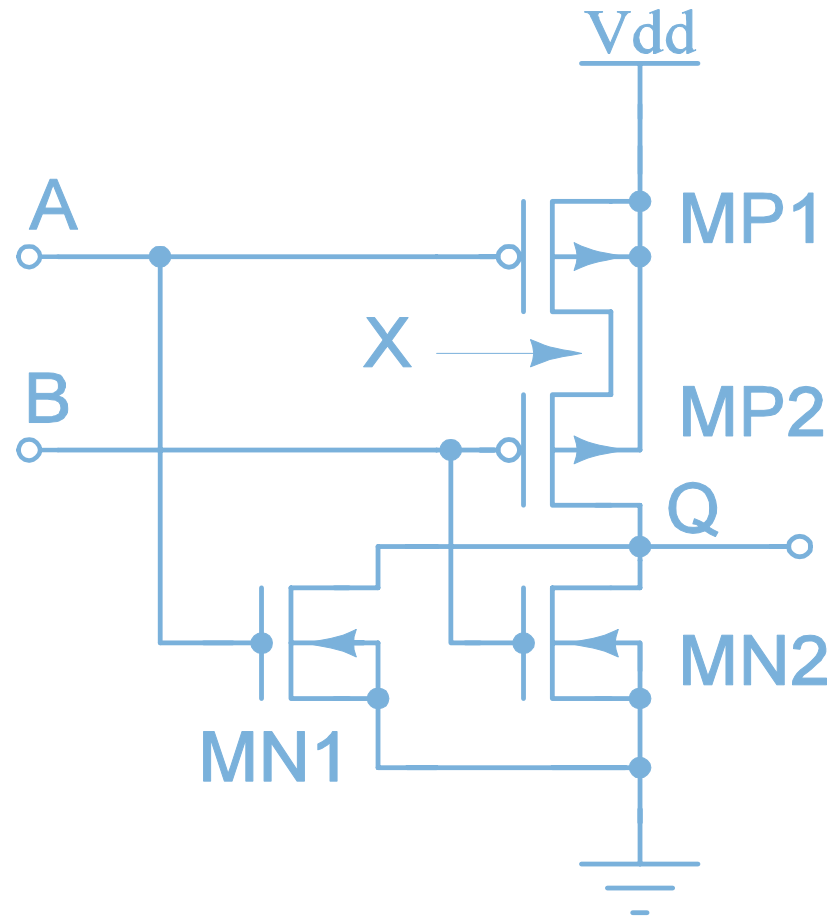
PSP NQS model (vi)

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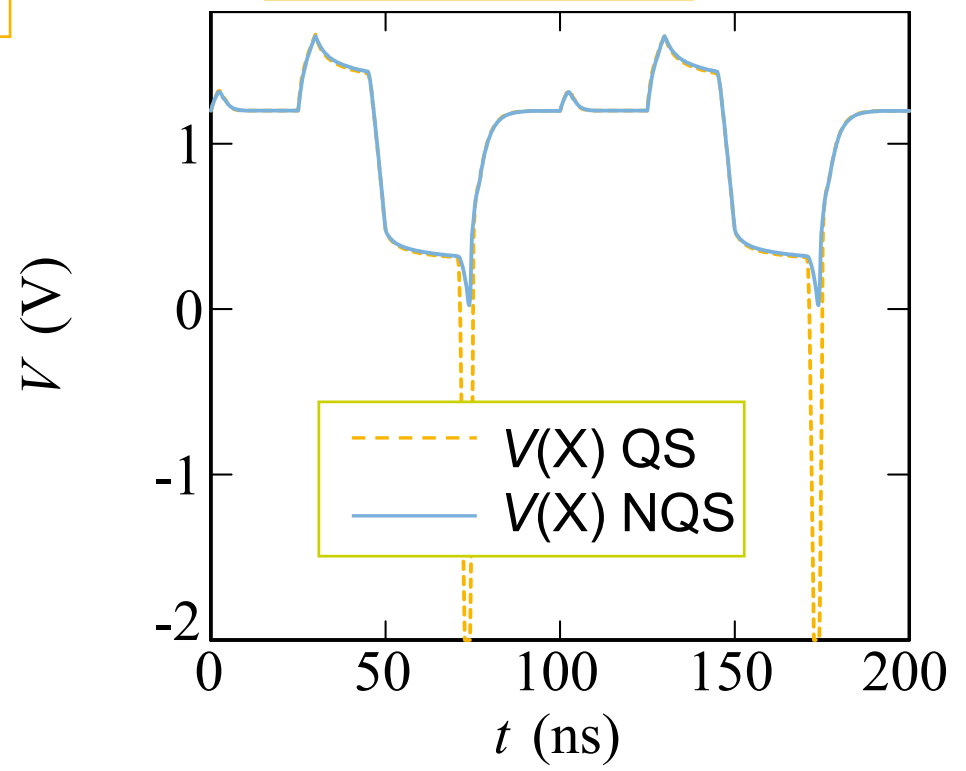
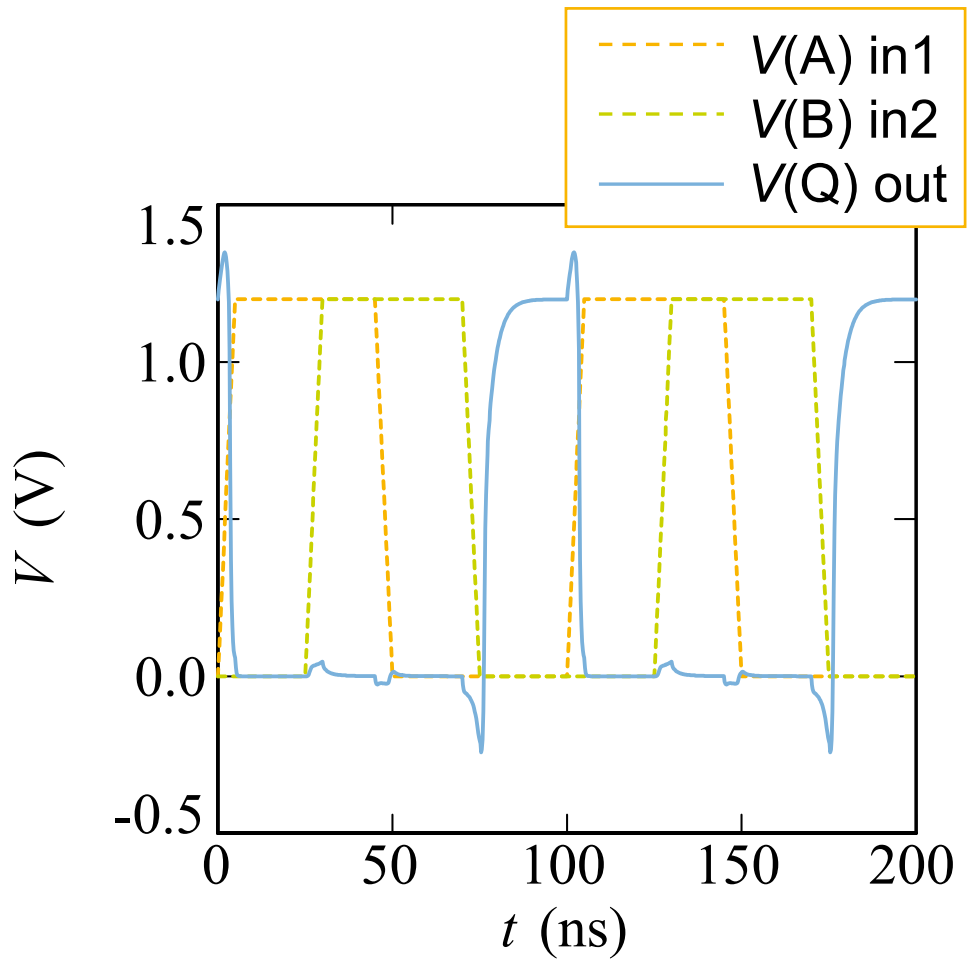
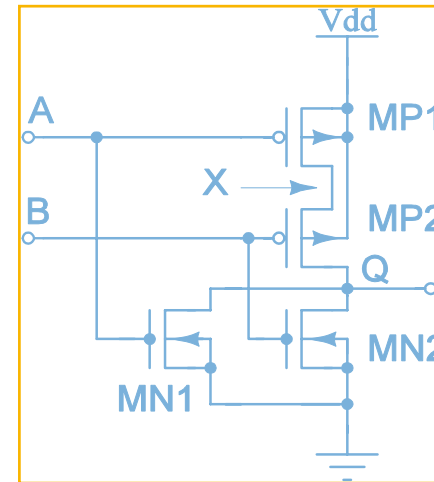
..... measurement
---- PSP quasi-static
—— PSP NQS



“Killer” NOR circuit (i)



“Killer” NOR circuit (ii)



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Summary

- ▶ Affiliation change:
 - Philips → NXP
 - Penn State → Arizona State
- ▶ PSP is the new CMC industrial standard MOSFET model
- ▶ PSP has an excellent description of distortion
- ▶ PSP has a unique physics based NQS-extension



References

- ▶ website <http://pspmodel.asu.edu>
- ▶ PSP general
 - TED 53(9), p. 1979 (2006)
 - Chapter 2 of “*Transistor Level Modeling for Analog/RF IC Design*”, W. Grabinski, B. Nauwelaers and D. Schreurs (Eds.), Springer-SBM, February 2006
- ▶ PSP NQS
 - TED 53(9), p. 2035 (2006)
- ▶ JUNCAP2
 - TED 53(9), p. 2098 (2006)
- ▶ FinFETs
 - IEDM 2006

