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Low-Power Circuits and Beyond: a Designer's Perspective on the EKV Model and its Usage

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Introduction

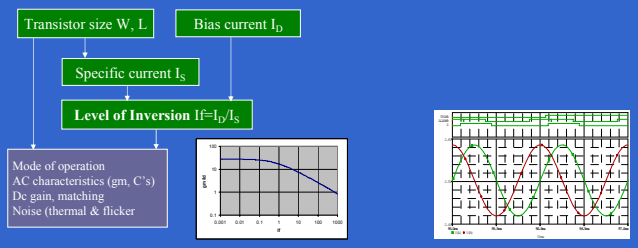
Why use the EKV model…

…when there is a perfectly good 'industry standard' model supported by all the foundries and EDA tool vendors?

Low power circuits:
- Better modeling of the weak and moderate inversion areas
- The model was developed for low-power circuits. This is the typical application for the EKV model.

Compact model:
- True 'compact' model (small number of parameters)
- Hierarchical model: can be used both for simulations and hand calculation
- Faster simulations

Analog IC design:
- Better modeling of gm and noise, not just I_D
- Analog circuits are usually biased with currents
- 'Level of inversion' design methodology

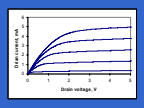


Hand calculations

Circuit simulations

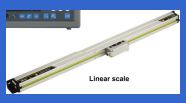
Both are based on the same model and the theory behind it.

Example 1 – Very low power analog circuit for battery operated small tools

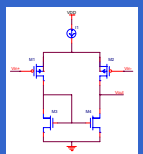


- Low power circuit – typical application for the EKV model.
- Foundry supplied transistor samples – we performed the extraction using a rented HP4155B.
- After presenting the benefits of the EKV model for low power design to the foundry model specialists, they took over the extraction and the model support.
- The design was successful and the chip is now in production.

Example 2 - Photo Diode Amplifier Input Stage Optimization



- Line –powered (5.0V) circuit – Although this is NOT a typical application for the EKV model, the model has some key advantages for analog circuit design.
- The design was optimized using the 'level of inversion' design methodology.
- The design was successful. The circuit performance exceeded expectations and the chip is now in production.

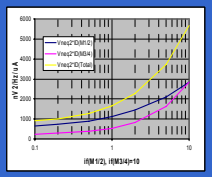


$$i_f = \frac{I_D}{I_S}$$

$$\frac{g_m}{I_D} = \frac{1}{n \cdot UT} \cdot \frac{2}{1+\sqrt{4 \cdot i_f + 1}}$$

$$\gamma = n \cdot \frac{1}{1+i_f} \cdot \left(\frac{1}{2} + \frac{2}{3} \cdot i_f\right)$$

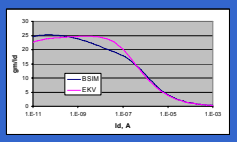
$$V_n^2 = \gamma \cdot \frac{4KT}{g_m}$$

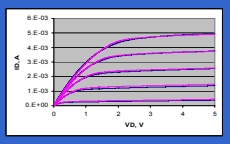


- The circuit equations can easily be combined with the EKV-based level of inversion equations to optimize the circuit performance (power consumption, gain, bandwidth, noise...).
- We had a power budget for each amplifier, and needed to optimize the circuit for low noise, bandwidth requirements and size.
- This optimization was done using a simple Excel spreadsheet.

The Designer's Challenge: Obtain the Model Parameters!

Method 1 – Estimate the EKV model from the foundry-supplied model (BSIM)

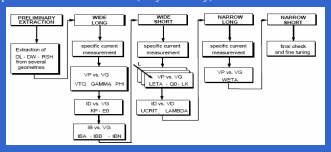




- Sometimes it is the only available option.
- However, we are extracting from a model that is not 'perfect'.
- BSIM-EKV conversion tools exist (EPFL).
- Can use as a starting point for method 3.

Method 2 – Perform EKV extraction on transistor samples

- Best method, as the recommended EKV extraction method can be followed.
- Best if the extraction is performed by the foundry (unlikely).
- Can use a qualified extraction service (may be costly).

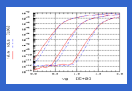


Recommended EKV2.6 extraction flowchart

Method 3 – Extract the model from typical foundry-supplied transistor data

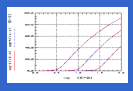
- May be the best possible compromise for a better model with minimal involvement from the foundry (the foundry just has to provide tested transistors data).
- The tested data can be used to 'fine tune' the model estimated from the BSIM model.
- We are using this approach on a current project using a 0.35um analog process.

Use Log(Id) vs.Vg for threshold parameters



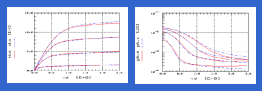
➡ VT0, PHI, GAMMA, LETA(short), WETA (narrow)

Use Id vs.Vg for mobility parameters



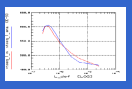
➡ KP, E0, RSH (short), DL (short), DW (narrow)

Use wide & Short Id vs.Vd



➡ UCRIT, LAMBDA

VTO vs L for RSCE



➡ Q0, LK

EKV2.6 Extraction Summary Table

Method	Accuracy – fit	Requirements	Used by MEI	Comments
1	Poor	Foundry design kit	First	Quickest
2	Best	Transistor samples Semiconductor measurement instrument	Small tool very low power project	Uses recommended EKV extraction flowchart
3	Good	Transistor data	Current projects	Good compromise

The Future: EKV 3.0

- We would like to start using the EKV3.0 model soon.
- With 0.35um geometries and below, the limitations of 2.6 are becoming more apparent (the lack of 2nd order mobility reduction, scaling with short & narrow transistors…)
- We are waiting for the full implementation of EKV3.0 in simulators. EKV2.6 is now supported by most commercial simulators. We plan on using the Verilog-AMS implementation of EKV3.0 as an intermediate solution in the near future, but it is slower than a fully implemented model.

Conclusions

- The 'level of inversion' design methodology and the EKV model have significant advantages for low-power circuits and analog circuit design.
- MEI completed several successful projects using this method. Two of those ICs are currently in production.
- The model parameters can be extracted using foundry-provided transistor samples or transistor data.
- We have been working with EKV2.6 and are planning on using the EKV3.0 version soon, as we are starting to use smaller geometry processes.

D. Foty, D. Binkley, and M. Bucher, "*gm/ID*-Based MOSFET Modeling and Modern Analog Design," *International Conference on the Mixed Design of Integrated Circuits and Systems*, June 2002.
Grabinski, EKV Model v2.6 and Extraction Methodologies', ICCAP Users' Web Conference, Dec. 2001