

Lumped Element Behavioural High Voltage MOS Model

Sebastian Schmidt
Matthias Franke

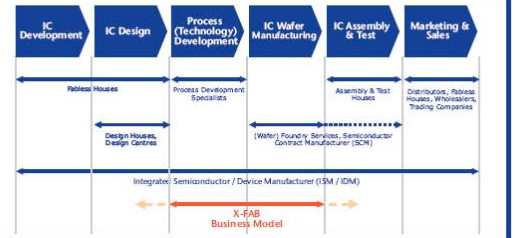
Contact:
X-FAB Semiconductor Foundries
Haarbergstr. 67, 99097 Erfurt, Germany

sebastian.schmidt@xfab.com

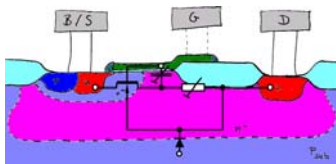
About X-FAB

X-FAB technology portfolio

- CMOS, BiCMOS technologies 0.35µm-1.0µm
- Special processes (DMOS, SOI, MEMS)
- Design Libraries (primitive devices, function blocks)
- Device Models (Cadence, Tanner, Silvaco)
- IP blocks (memory, sensors)

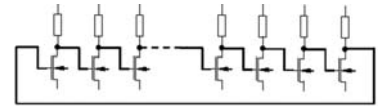


Introduction



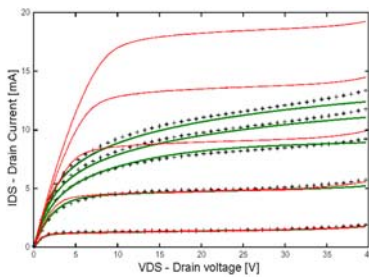
Abstract: High voltage mos transistors usually have a drift zone in the drain region. The conductivity of this drift zone is strongly dependent on the flowing current and gate voltage. Thus it has generally to be modelled with a variable resistance representing the effects on the current. The goal of this work is to show a phenomenological macro model including AC modelling. The model is restricted to a lumped element sub-circuit, which can be processed by a standard spice simulator. A drain resistance can be described by a behavioural source and a resistance in series. The source could be a current or voltage source controlled by drain current and gate voltage. The example discussed here describes a sub-circuit containing a current source with a resistor in series as well as a model of the voltage dependent gate to drain capacitance. One of the most important goals of development was a fast convergence of the transient simulation. This was achieved by a restriction of the mathematical formula for the current function. The model is tested by means of a ring oscillator. The results have been satisfactory for DC, AC as well as transient analysis.

Ring Oscillator Testbench

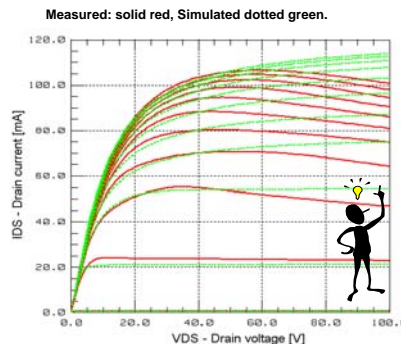


A 21 stage ring oscillator test-bench for nmos has been used for testing the convergence in transient simulations.

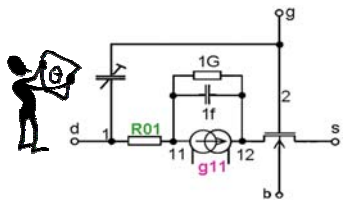
The DC Model



IDVD Characteristic showing quasi saturation. Measured data: + symbols. Red line: bsim3v3 model with resistor in series. Green line: bsim3v3 enhanced DC model

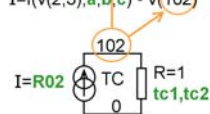


Output (idvd) characteristic of the LD MOS DC model. The model neglects the self heating effect.

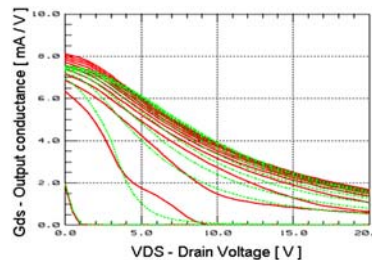


$$I(g11) = \frac{v(11,12)}{v(102) + 1 + \sqrt{1 + v(11,12)^2 / v(101)^2}}$$

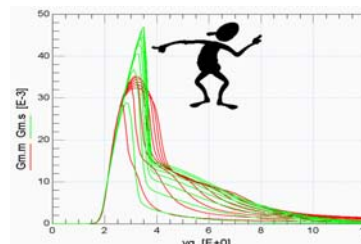
Gate Voltage influence: $I = f(v(2,3), a, b, c) \cdot v(102)$



$$I(g101) = \frac{a \cdot V(102)}{1 + \exp(-b(V(2,3) - c))}$$

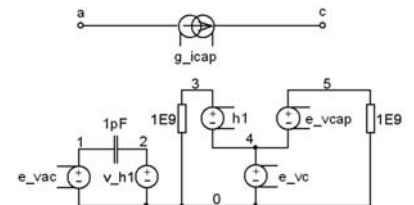


Gds characteristic of the LD MOS DC model.



Gm characteristic of the LD MOS DC model.

The AC Model



Current source and auxiliary circuit with reference capacitance

Current of the behavioural capacitance:

$$I(g_icap) = V(3,c) \cdot V(5,c)$$

Voltage between anode and cathode:

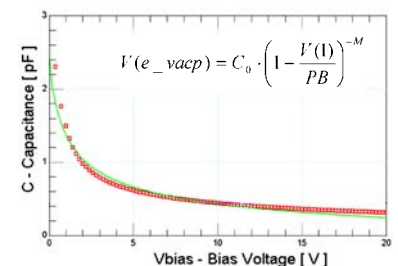
$$V(e_vac) = V(a) - V(c)$$

Cathode potential:

$$V(e_vc) = V(c)$$

Reference capacitance value as voltage:

$$V(h1) = I(v_h1)$$



The enhanced capacitance model in the HV mos model. Measured: red squares, Simulated: green line

Conclusion

The DC as well as the AC model show a good agreement with measured values and can be used in a standard spice simulator. The model has been checked regarding both usability and convergence time in order to enable good convergence in an application simulation.

The Authors

Sebastian Schmidt and Matthias Franke are with the Department of Process Characterisation, X-FAB Semiconductor Foundries, Haarbergstr. 67, 99097 Erfurt, Germany.

Acknowledgements

We would like to thank Axel Hammer for his constant and kind support for understanding modelling, Steffen Richter and Andreas Roth for a large amount of high voltage mos transistor layouts as well as Ralf Lerner for his support regarding the LD MOS transistors. All named are with X-FAB.