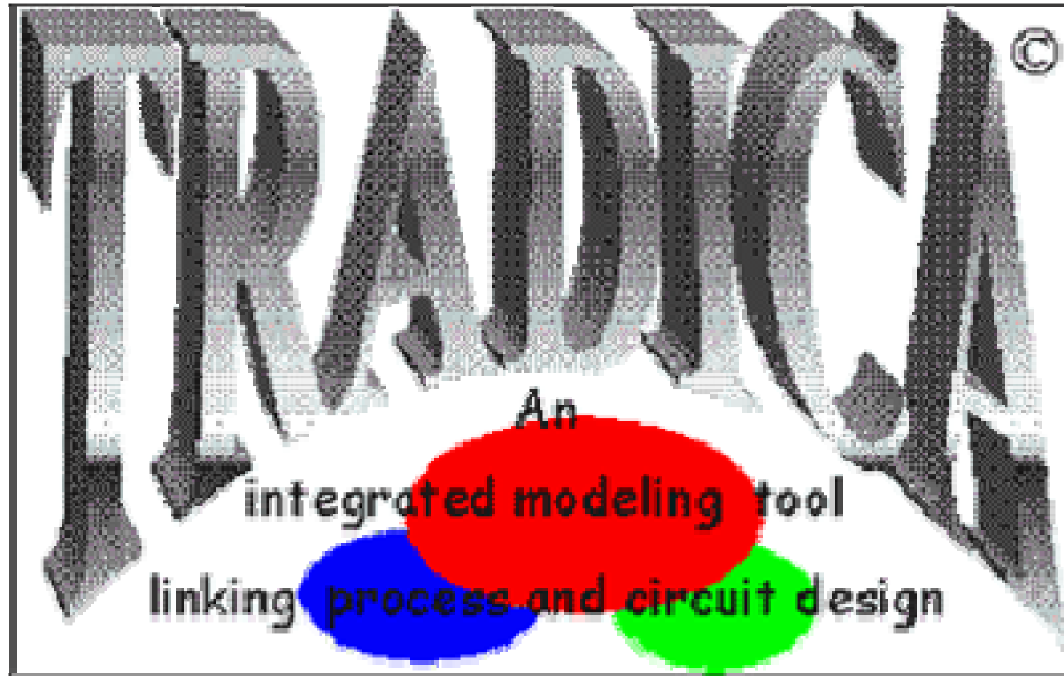


# **TRA**nsistor **DI**mensioning and **CA**lculation program

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# Outline

- Introduction
- Process Input
- Parameter Generation
- Predictive Modeling
- Statistical Modeling
- Device Sizing and Process Optimization
- Examples

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# Introduction - Motivation

- increasing demand for circuit performance
  - ⇒ requires transistor operation close to process performance limit
  - ⇒ careful circuit optimization through proper ***transistor sizing***
- large variety of circuit applications
  - ⇒ overall required number of transistor configurations is very large (>100)
  - ⇒ need ***geometry scalable compact models*** and parameters
- large variety of bipolar processes require ***sophisticated geometry scaling equations***
  - ⇒ difficult to integrate
  - ⇒ difficult to maintain
  - ⇒ difficult to update

  } in PDKs => use TRADICA instead

# Introduction - Motivation

- reduce time-to-market: start circuit design during process development (***concurrent engineering***)
  - ⇒ ***predicted*** but consistent ***model parameters*** and flexible parameter generation
- align process development with product (design) needs
  - ⇒ ***quick evaluation*** of process change impact on device and circuit performance
  - ⇒ allows fast ***decision making about suitable process***
- include process tolerances in design
  - ⇒ ***statistical* simulation**
  - ⇒ ***matching* simulation**

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# Introduction – Basic Idea

- provide ***criteria for transistor sizing***

  ⇒ calculation of device dimensions
  ⇒ calculation of device configuration

- provide fast means for generating ***consistent sets of (compact) model parameters*** based on design rules and process information

- provide compact models for various types of devices and applications
  - ***different model types***
    - MOS (EKV)
    - Bipolar (SGPM, HICUM)
    - Passives (diode, res, mincap, …)

  - **model hierarchy => different complexities** w.r.t. physical effects

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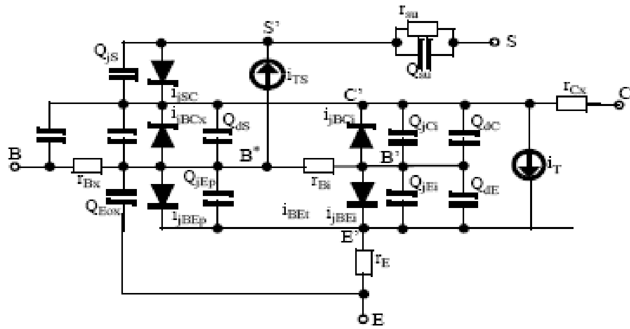
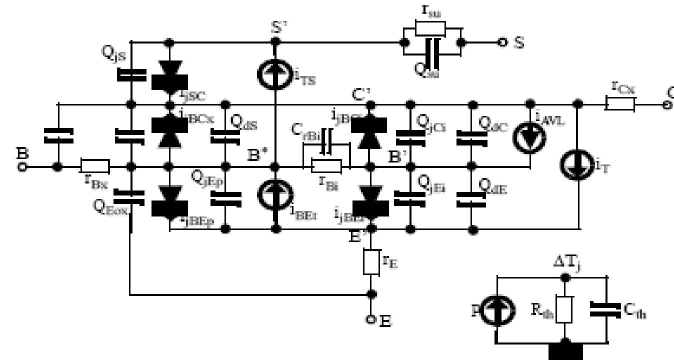
# Introduction – Basic Idea

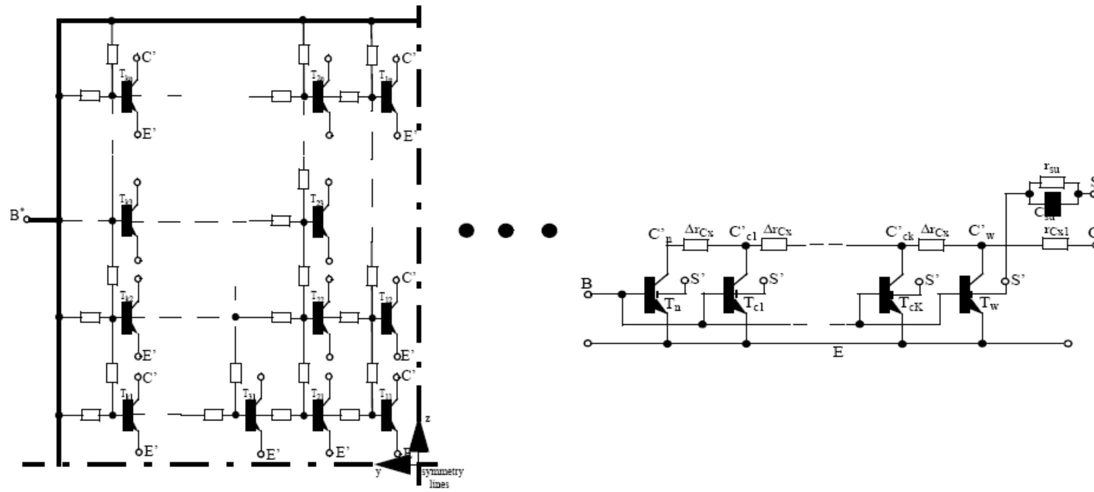
SGPM/Level2



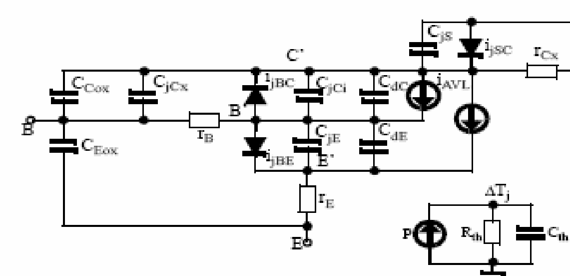

HICUM/Level2



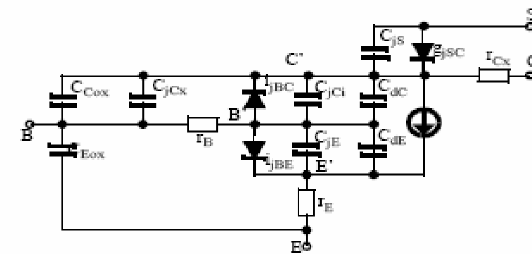

HICUM/Level4




HICUM/Level0




SGPM/Level0

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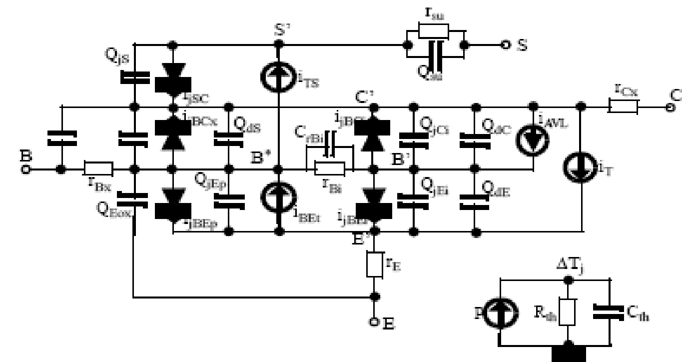
# Introduction – Basic Idea

- provide ***criteria for transistor sizing***
- provide fast means for generating ***consistent sets of (compact) model parameters*** based on design rules and process information
- provide compact models for various types of devices and applications
  - ***different model types***
  - **model hierarchy => different complexities**
- basic assumption:
  express the value Z of each element $E_k$ in a compact model as function
  $Z(E_k) = f_k$ (voltage
  current
  junction temperature
  transistor configuration
  process data
  design rules
  tolerance data)

HICUM/Level2

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# Process Input

- design rules
  - lateral dimensions
  - vertical dimensions

defining the ***transistor layout*** of a given process

- specific electrical parameters
  - fixed for a given process
  - sheet resistances, contact resistances, zero-bias capacitances
  - can be obtained by measurement or calculation directly from process information
    $\Rightarrow$ allows ***fast predictive modeling for concurrent engineering***

- process tolerances
  - process control monitors (PCMs)
  - technology parameters (TPs)

- other process information, such as
  - smallest manufacturable (or guaranteed) emitter window dimensions
  - electromigration limits and BE contact metal pitch that affects linear scaling rules

- requirements for the “process-based scalable” approach:
  - process technology produces geometrically scalable transistor characteristics
  - employed compact models are sufficiently physics-based

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# Process Input

## process tolerances

process control monitors (PCMs) - technology parameters (TPs)

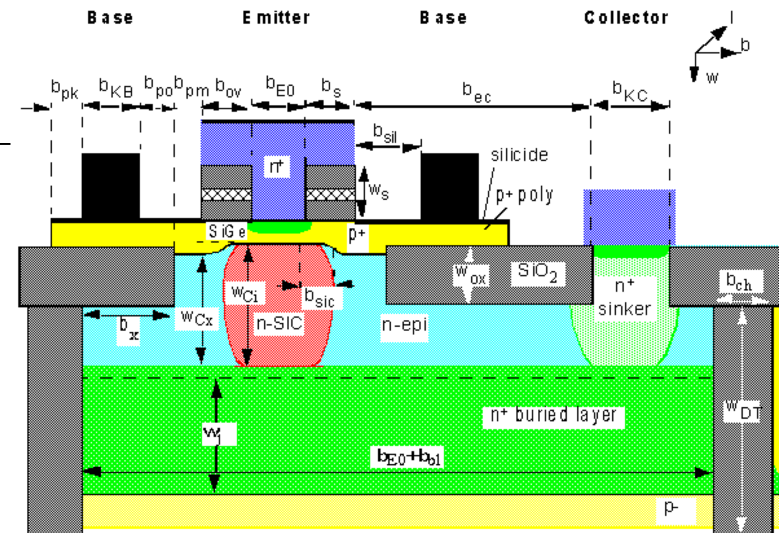
| PCM | value | TP | value | unit |
|---|---|---|---|---|
| r_rsBi0 | 0.154 | r_NBEi | 0.05 | |
| r_cjEi0 | 0.07 | r_wB | 0.08 | |
| r_cjE0 | 0.07 | r_NCi | 0.14 | |
| r_cjCi0 | 0.046 | ΔδVgm | 0.006 | V |
| r_iCil | 0.371 | ΔbE0 | 0.02 | µm |
| r_iCl | 0.371 | r_JBEi | 0.3 | |
| r_iBEil | 0.4 | r_tbdr | 0.0 | |

## process specific parameters

| base resistance | | | base emitter capacitance | | |
|---|---|---|---|---|---|
| rSBi0 | 1e+004 | Ohm | CjEi0 | 3.5 | fF/µm² |
| α(rSBi) | 0.003 | 1/K | VDE,i | 0.95 | V |
| rSsp | 800.0 | Ohm | nE,i | 2.0 | |
| α(rSsp) | 0.0007 | 1/K | ajEi | 2.5 | |

TRADICA

## design rules




predictive modeling
parameter generation

device sizing
process optimization

statistical modeling

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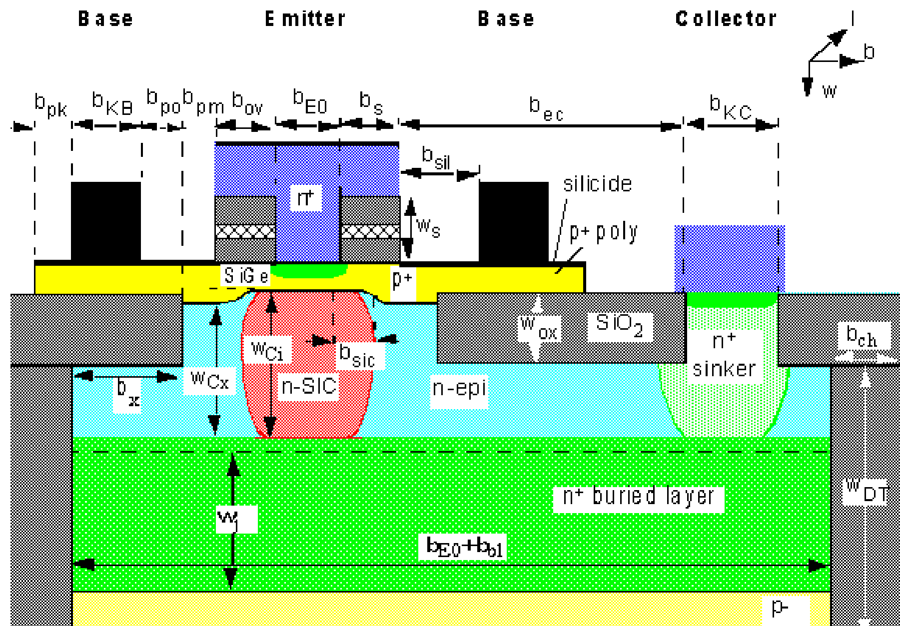
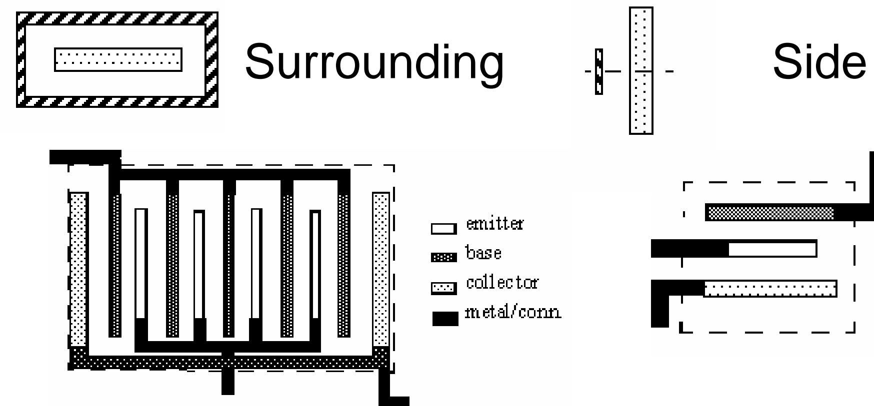
# Parameter Generation

- parameter generation is based on process information and transistor configuration

process information **+** transistor configuration




- number of base, collector, emitter contacts
- emitter window dimensions
- contact configuration (e.g. collector location)




- ***geometry scaling equations*** for each equivalent circuit element

- generate consistent sets of geometry scalable compact model parameters for any desired transistor configuration, based on ONE set of process information ⇒ ***simplifies PDK development and delivery***

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# Predictive Modeling

***purpose:*** provide (quantitative) information on how process changes impact electrical device and circuit performance

***assumption:*** "large-signal" variations from (targetted) "nominal" values can be significant

- process-based scalable approach already provides dependence of model parameters on PCMs and layout information

- TRADICA's "prediction module" contains:
  - accurate (lateral) ***geometry scaling equations*** correlating model parameters to large variations in transistor configuration
  - can be based on either ***PCM or TP input***
  - ***correlation*** between model parameters

- bias and temperature dependent compact model equations

  $\Rightarrow$ transistor sizing, output of bias and FoM information, bias and frequency sweeps

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# Statistical Modeling

***purpose:*** provide (quantitative) information on how process tolerances impact device and circuit yield

***assumption:*** tolerances can be considered as "small-signal" deviations from nominal values

- based on PCM input, such as sheet resistances and capacitances per unit area (capacitance data is mandatory for high-speed processes and applications)

- ***correlation*** of model parameters through TPs

- calculations based on ***relative changes w.r.t. "nominal" values*** (except for dimensions) and include physical effects

- procedure for generating ***statistical information on PCMs / FoMs***

  $\Rightarrow$ high-frequency S- or Y-parameters for verification purposes

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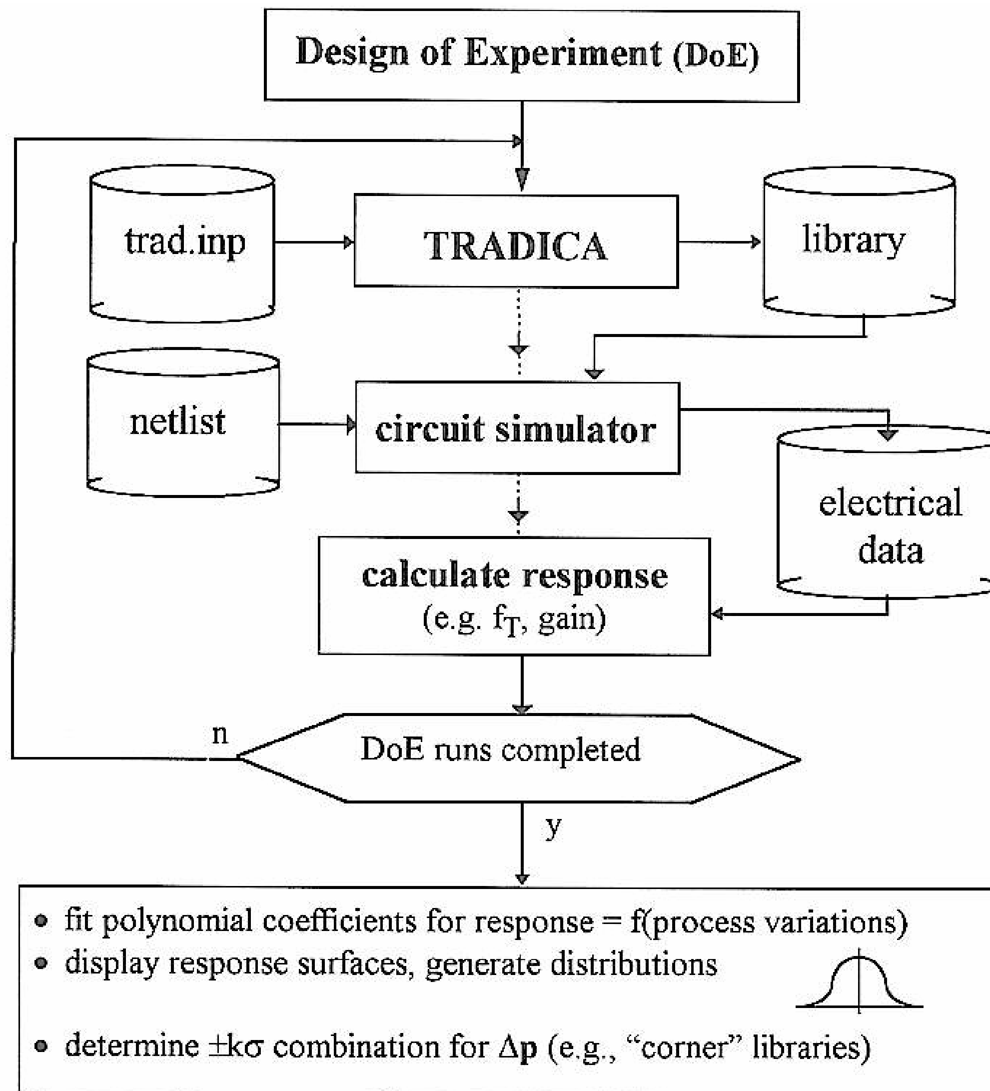
# Statistical Modeling




- usually, only a subset of all TPs is relevant for a particular design

⇒ identifiable via ***sensitivity analyses***

⇒ strong ***reduction*** of simulation runs

- full-scale statistical simulation based on
    - PCM or TP input
    - Design of Experiment
    - Response Surface Method

- generation of ***skewed parameter sets***

- determination of ***worst/best corner-case parameter sets*** for given device/circuit figures of merit

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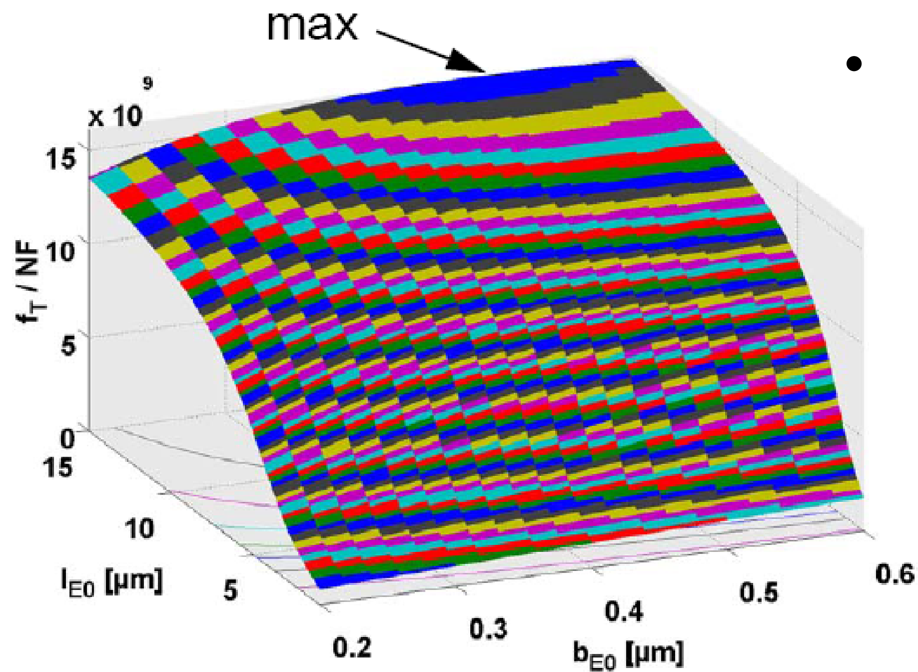
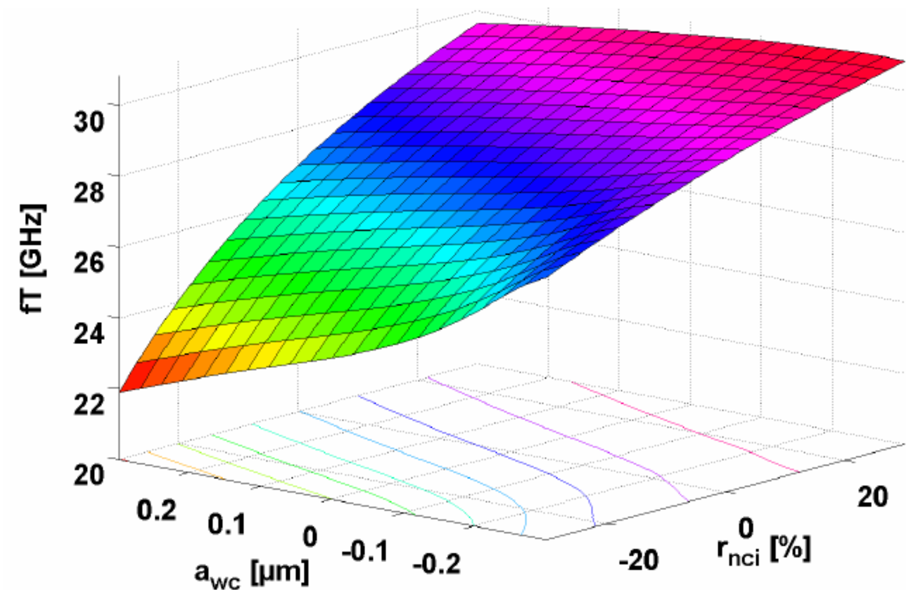
# Device Sizing and Process Optimization




- device sizing
  - calculates optimum device dimensions / configuration based on user selected FoM
  - optimization of one or several FoM at once
  - search for specific FoM value, e.g. $Z_{IN}$=50Ω
  - designed for high-dimensional optimization
  - analytical equations for circuit FoMs

- process optimization
  - calculates optimum TPs
  - provides quick overview on influence of process changes on device/circuit FoMs early in process development

  ⇒ ***fast w.r.t. TCAD simulations*** (orders of magnitude)

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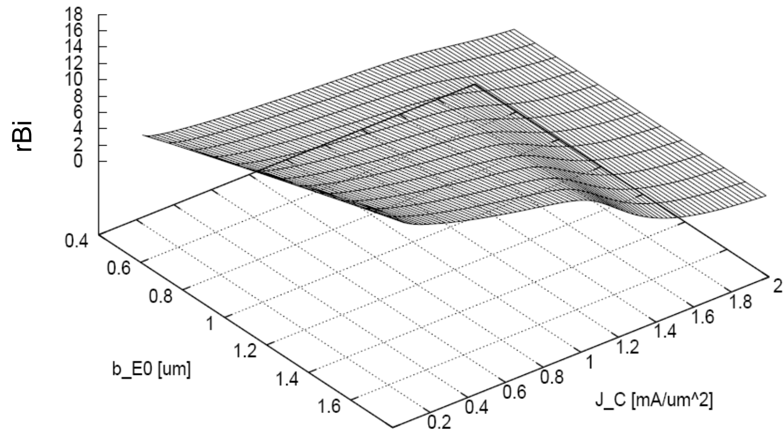
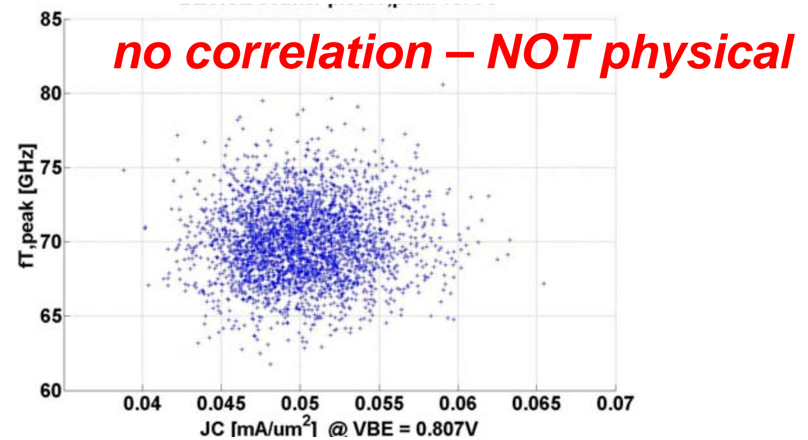
# Examples

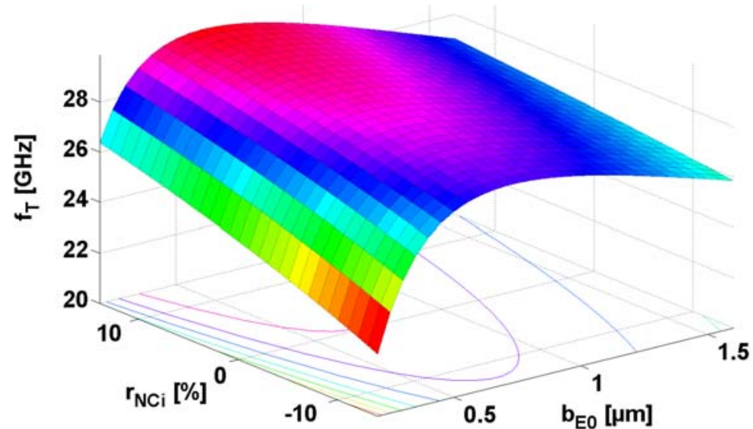
- teaching
- statistics

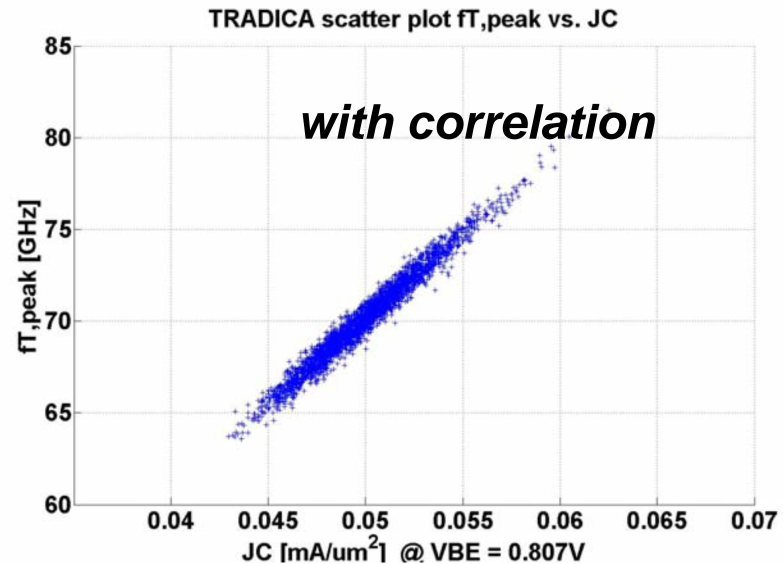



model element values and FoMs vs. geometry, bias, frequency and temperature

influence of correlation on statistical simulation results

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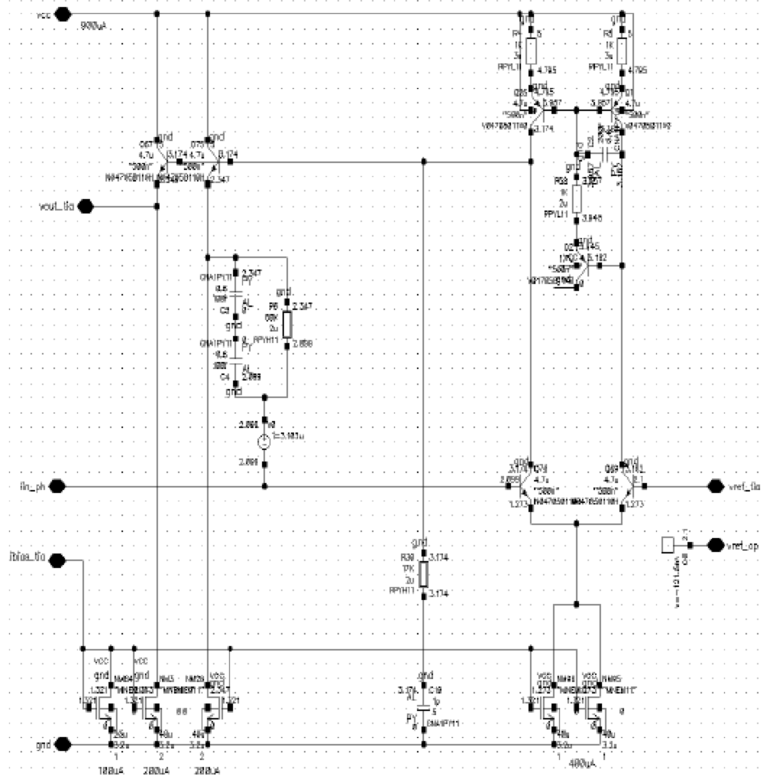
# Examples

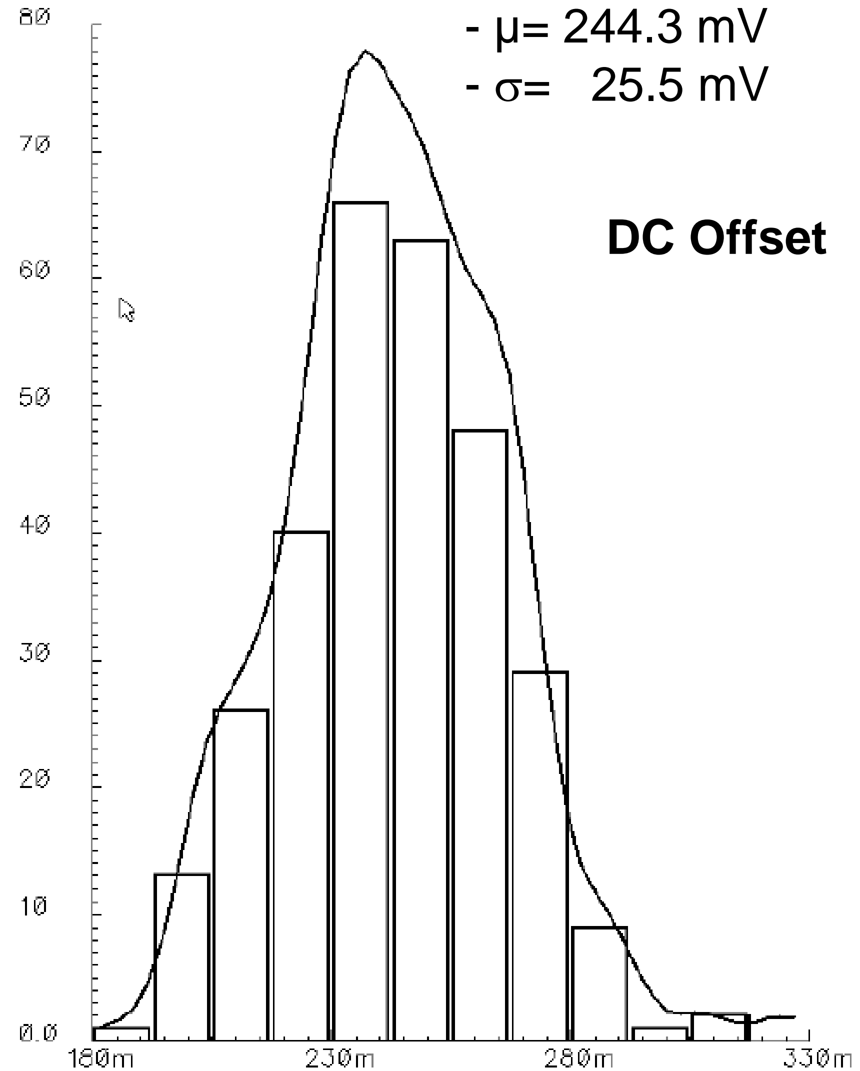
**Transimpedance Amplifier (TIA)**

first production design by Atmel



- sensitivity analysis
  ⇒ identify nbei
- TIA process variation (nbei)
  - $\mu$= 244.3 mV
  - $\sigma$= 25.5 mV

**DC Offset**

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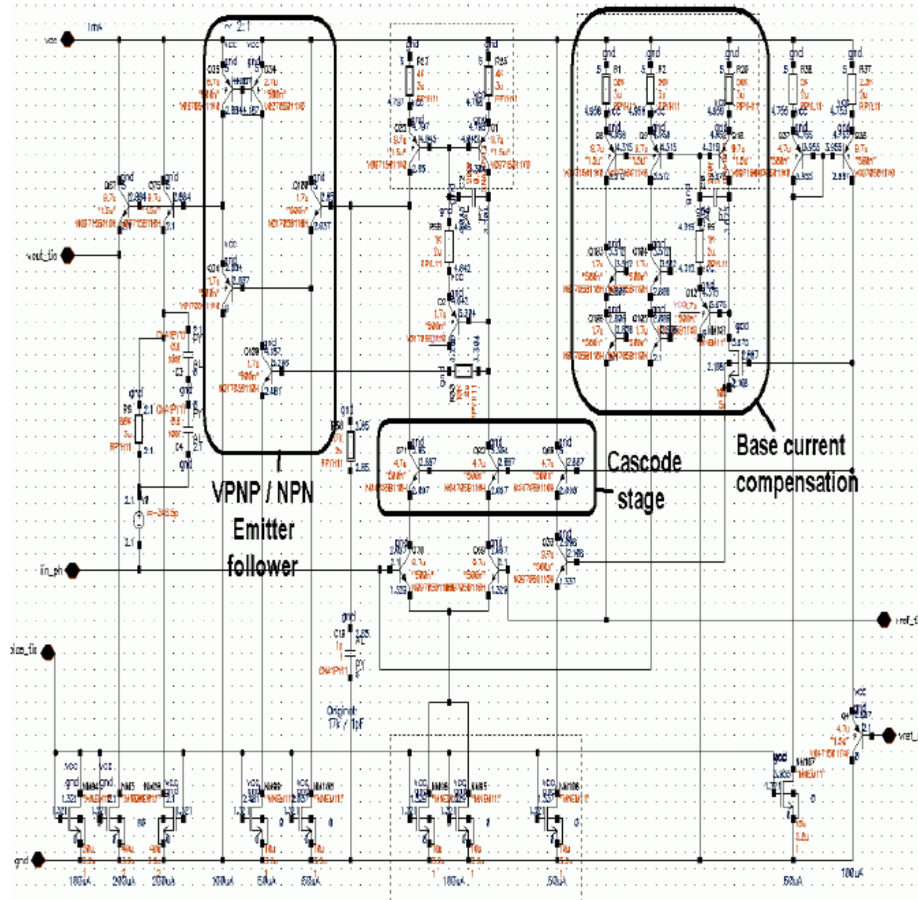
# Examples

**Transimpedance Amplifier (TIA)**

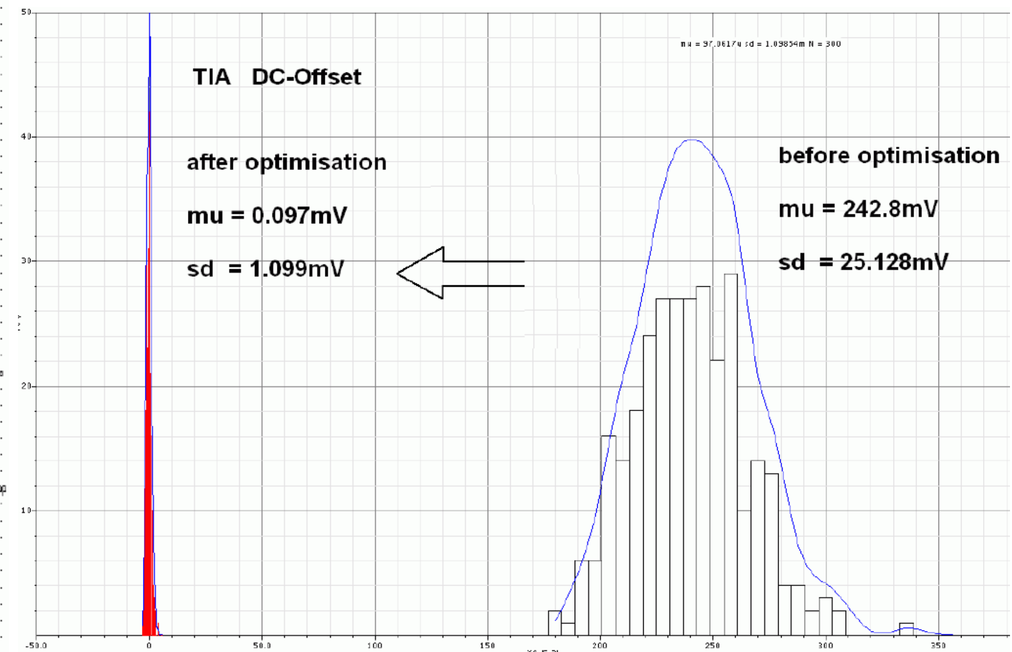
redesign




- process variation analysis
  - $\mu$=0.1 mV
  - $\sigma$=1.1 mV

⇒ significant yield improvement

⇒ experimentally confirmed, also for other circuits and process technologies

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# Conclusion

- generation of consistent sets of geometry scalable model parameters
  $\Rightarrow$ more efficient (time / cost) than the “single transistor fitting” approach
  $\Rightarrow$ faster and more accurate parameter determination
  $\Rightarrow$ PDKs are much easier to generate and deliver

- generation of predictive parameter sets
  $\Rightarrow$ concurrent engineering (e.g. reduction of design cycles, time-to-market)

- statistical simulation and modeling capability
  $\Rightarrow$ generation of skewed parameter sets
  $\Rightarrow$ full-scale statistical simulations
  $\Rightarrow$ determination of worst/best corner-case parameter sets

- generic optimization algorithms are available
  $\Rightarrow$ device sizing
  $\Rightarrow$ process optimization

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