Optimization of the Substrate Parameters for EM-Simulators

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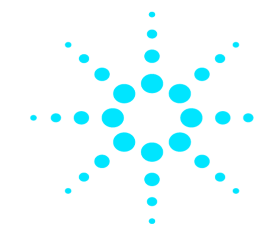

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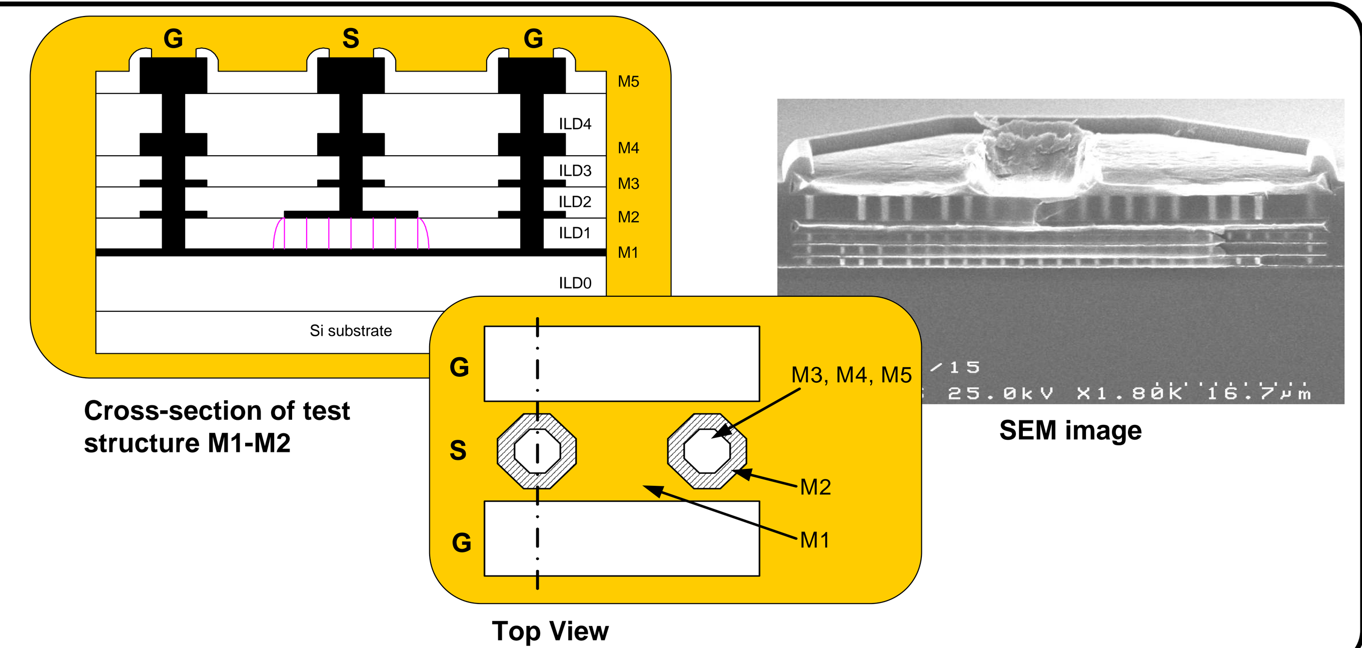
1. Introduction / Goal

High frequency circuits need precise models of the passive components. Usually these components are designed with the aid of electromagnetic (EM) field simulators. For an accurate EM-simulation result, it is important to accurately know the substrate parameter values at the frequencies of the EM-simulation.

A technique for the extraction and optimization of the EM-simulator substrate parameters (relative permittivity ε_r, dielectric loss *tan-δ*) is presented. Those parameters are extracted/optimized for each interlayer dielectric (ILD) and/or silicon substrate separately.

2. Test Structures

The focus of the substrate parameter optimization are the dielectric layers between metallization. Inter-metal capacitors are excellent candidates for that purpose. They are placed directly under the contact pads to minimize the influence of metal layers. The capacitors are measurable with Ground-Signal-Ground (GSG) probes. Deembedding errors are automatically avoided since no deembedding is necessary. The top plate metal of the capacitor is wider than the via-metals above. This prevents a disturbing of the measurements by fringing capacitances from the upper metals.

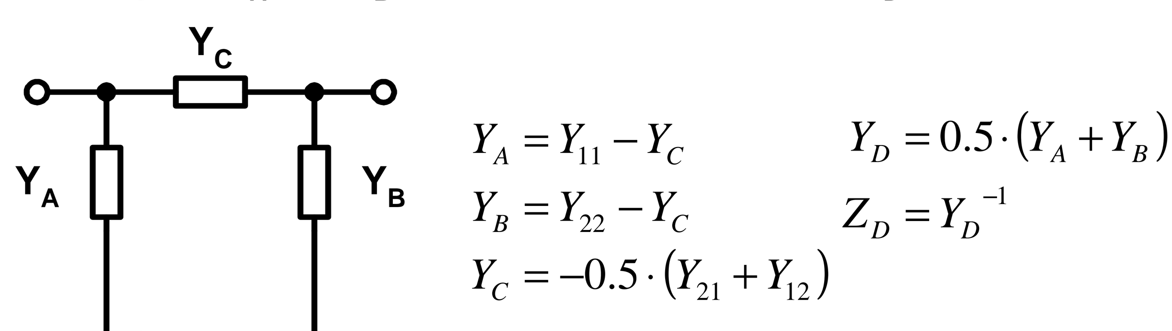


Cross-section of test structure M1-M2

Top View

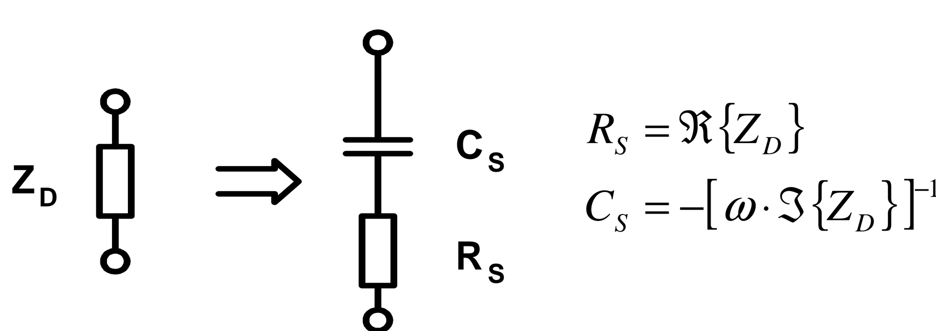
3. Measurements

The test structures are interpreted as Π structures, so S-parameters are converted to Y-parameters. The test structures are fully symmetrical, so $Y_{21}=Y_{12}$ and $Y_A=Y_B$. The average of Y_A and Y_B is converted to impedance Z_D.



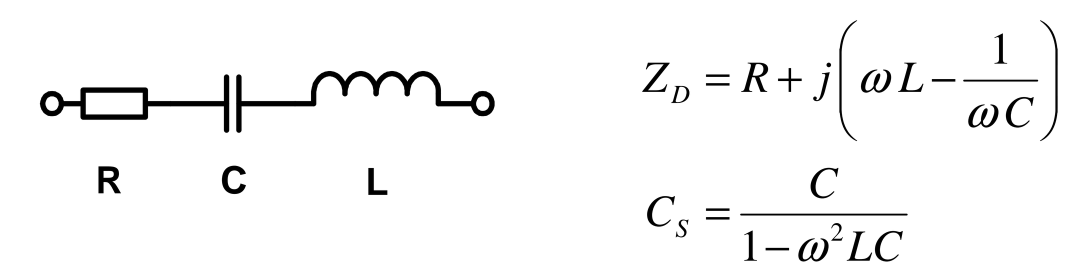
$$Y_A = Y_{11} - Y_C \qquad Y_D = 0.5\cdot(Y_A+Y_B)$$
$$Y_B = Y_{22} - Y_C \qquad Z_D = Y_D^{-1}$$
$$Y_C = -0.5\cdot(Y_{21}+Y_{12})$$

The impedance Z_D becomes the main target for the optimization of the EM-simulation substrate parameter values. For the proposed test structures, ε_r is represented by a capacitance, and *tan-δ* by a series resistance. This leads to the final interpretation of Z_D as a series of capacitance C_S and resistance R_S.



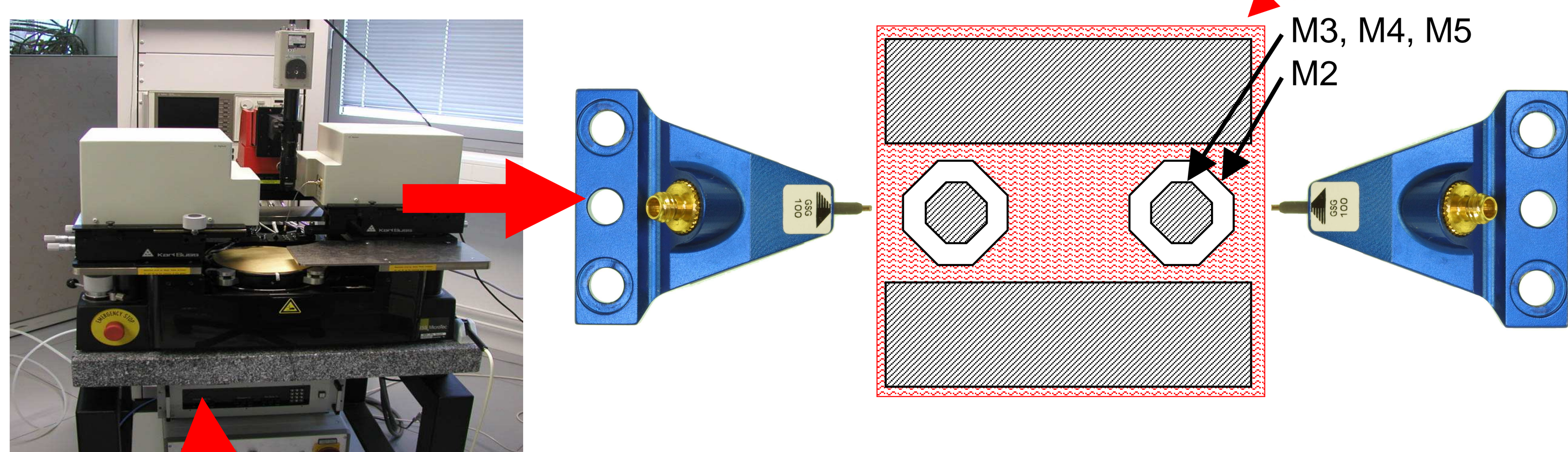
$$R_S = \Re\{Z_D\}$$
$$C_S = -[\omega\cdot\Im\{Z_D\}]^{-1}$$

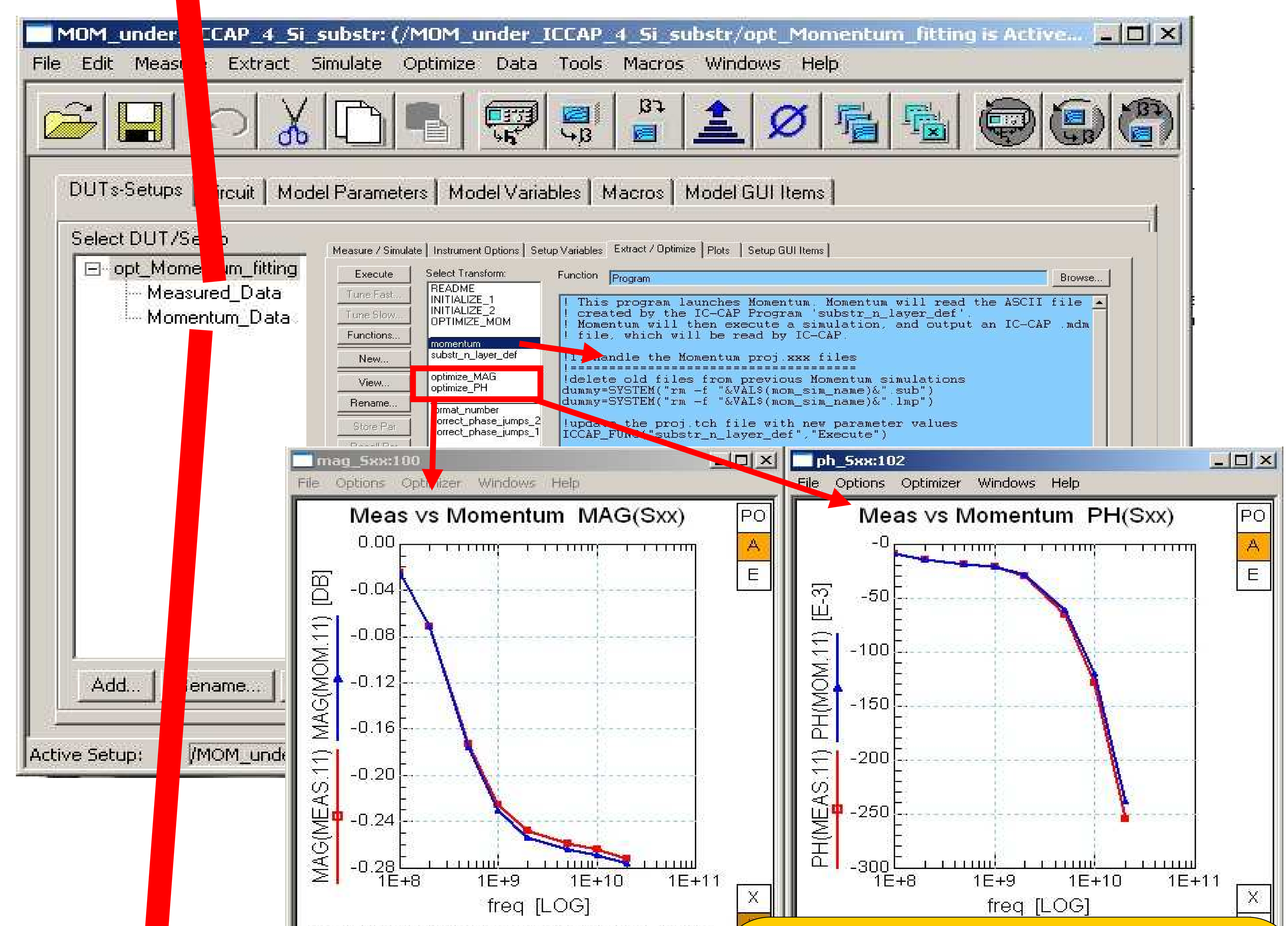
The elements C_S and R_S are frequency dependent if the equivalent circuit is too simple compared to the real measurement structure. The measurements show indeed an increasing capacitance over frequency. This indicates the presence of a small parasitic inductance, related to the signal current flowing from the signal contact to both ground contacts, in the lower metallization layer. The extracted parasitic inductance of the applied structures is about 3 pH.



$$Z_D = R + j\left(\omega L - \frac{1}{\omega C}\right)$$
$$C_S = \frac{C}{1-\omega^2 LC}$$

4. Optimization Loop Measured Data ➔ IC-CAP ⬌ ADS Momentum





The verified S-parameter measurements of the test structure are taken as the fixed target.

The result of the EM-simulations is considered as the material-parameter-dependent result.

An optimization loop, consisting of Agilent EEsof's modeling software IC-CAP and the EM-simulator ADS Momentum, will tune the material parameter values, starting from their available 1 MHz values, until a best fit between measurements and EM-simulations is obtained.

The final parameter values represent the material properties in the applied EM frequency range and thus, can be considered as calibrated substrate parameters.

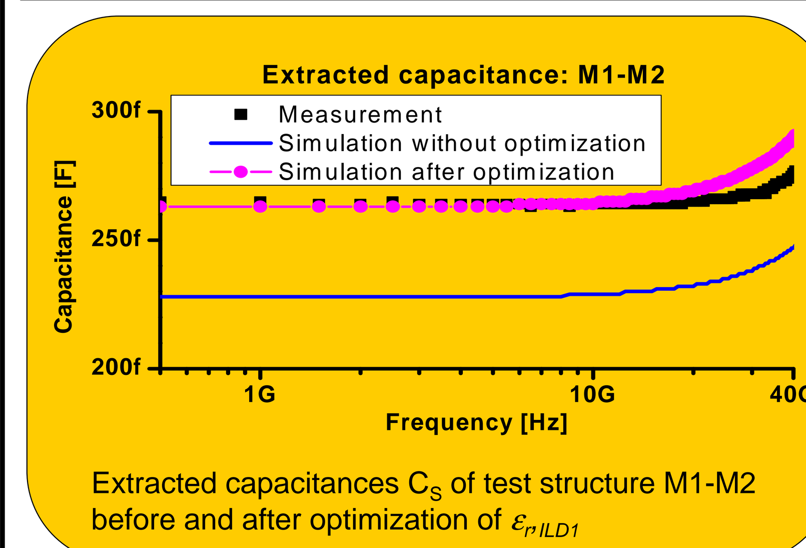
They are typically slightly different to those known from conventional, standard 1 MHz measurements.

5. Results

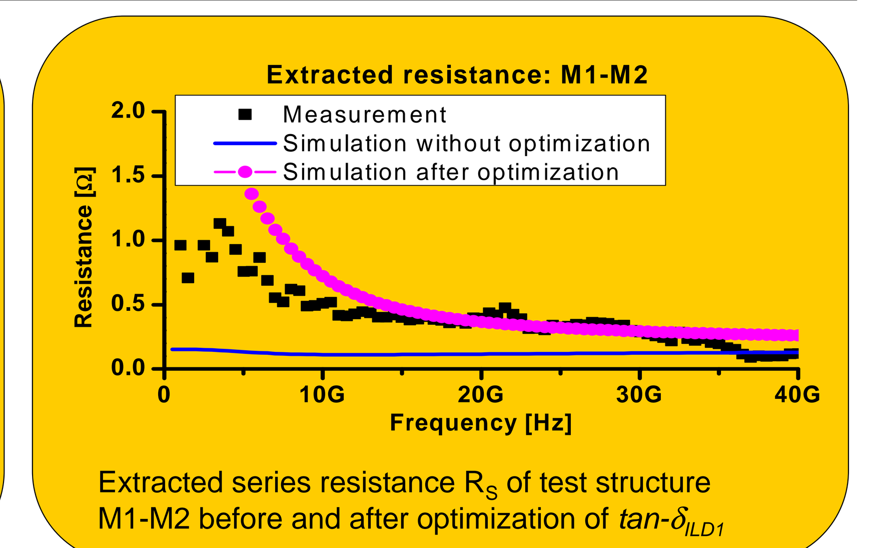
Since the frequency dependence of C_S does not be a function of the substrate parameters ε_r and *tan-δ*, which are to be optimized, we select the most flat frequency range in the C_S plots for this task.

The extracted resistance consists of 2 parts. Part 1 stems from the metallization including vias, the other part comes from the loss inside the oxide. We achieved a good fit of the extracted resistance after optimization of *tan-δ*. The trace "Simulation without optimization" (*tan-δ=0*) indicates the influence of the metal on the extracted series resistance.

Test structure	Area in µm²	Measured capacitance @1 MHz in fF	Measured capacitance @10 GHz in fF	Start values		Optimized values	
				ε_r	Loss tangent	ε_r	Loss tangent
M1-M2	5307	270	265	4.1	0	4.27	0.009
M2-M3	5307	250	245	4.1	0	4.37	0.006
M3-M4	5307	245	235	4.1	0	4.14	0.008
M4-M5	5307	85	80	4.1	0	4.28	0.014



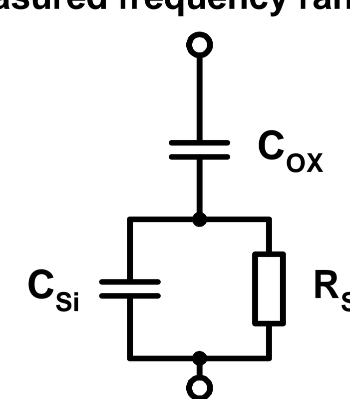
Extracted capacitances C_S of test structure M1-M2 before and after optimization of $\varepsilon_{r,ILD1}$



Extracted series resistance R_S of test structure M1-M2 before and after optimization of $tan\text{-}\delta_{ILD1}$

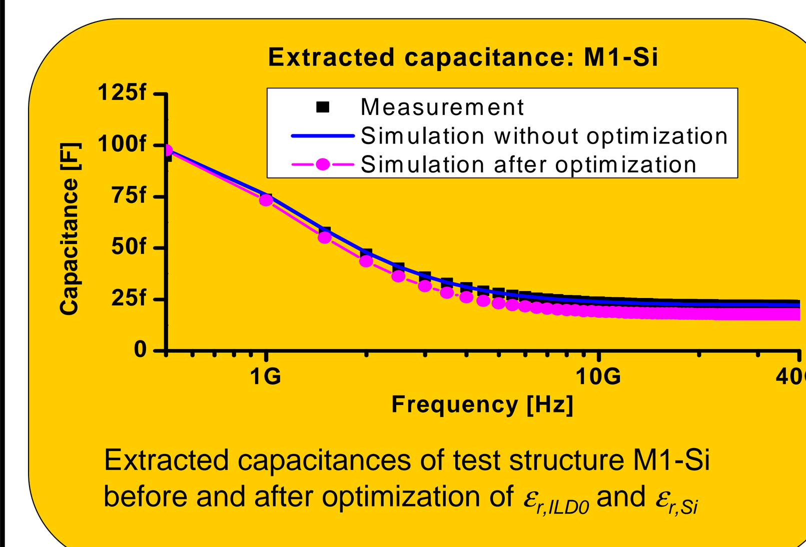
A special case is the test structure M1-Si. Silicon exhibits a conductive part and a dielectric part in parallel. They are represented by the elements R_{Si} and C_{Si} in the equivalent circuit. The extracted elements C_S and R_S are functions of the frequency.

The loss of ILD0 cannot be determined since the extracted real part is dominated by R_{Si} in the measured frequency range.

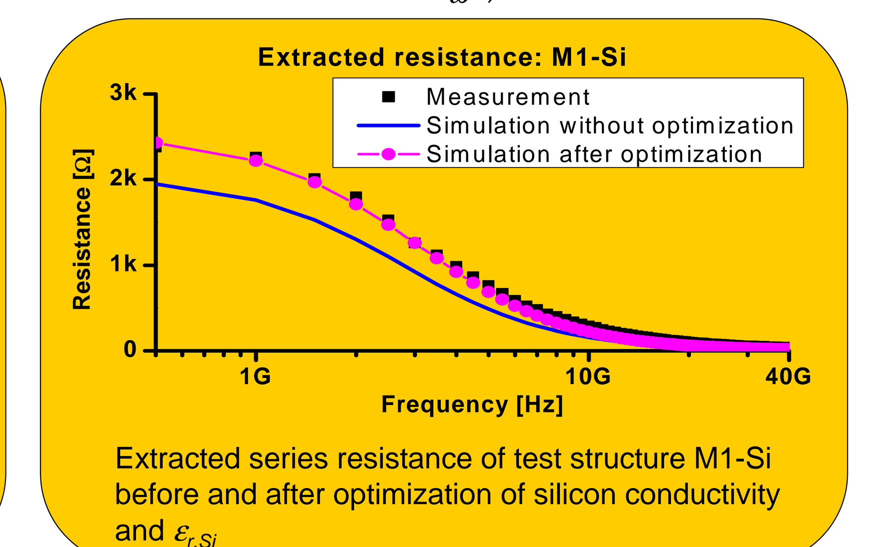


$$Z_D = -j\frac{1}{\omega C_{OX}} - j\frac{1}{\omega C_{Si}} \parallel R_{Si}$$
$$C_S = \frac{C_{OX}\left(1+\omega^2 R_{Si}^2 C_{Si}^2\right)}{1+\omega^2 R_{Si}^2 C_{Si}(C_{OX}+C_{Si})}$$
$$R_S = \frac{R_{Si}}{1+\omega^2 R_{Si}^2 C_{Si}^2}$$

$$\lim_{\omega\to 0} C_S = C_{OX} \qquad \lim_{\omega\to\infty} C_S = \frac{C_{OX}\cdot C_{Si}}{C_{OX}+C_{Si}}$$
$$\lim_{\omega\to 0} R_S = R_{Si} \qquad \lim_{\omega\to\infty} R_S = 0$$



Extracted capacitances of test structure M1-Si before and after optimization of $\varepsilon_{r,ILD0}$ and $\varepsilon_{r,Si}$



Extracted series resistance of test structure M1-Si before and after optimization of silicon conductivity and $\varepsilon_{r,Si}$

6. Conclusions

- Successful optimization of the substrate parameters (ε_r, *tan-δ*) for an EM-simulator has been presented
- Method of simulator calibration was adapted to an EM-simulator
- Suitable test structures have been shown
- The electrical behavior of the test structures is mainly dependent on the isolation parameters to find out
- Subsequent simulations of any arbitrary passive on-wafer structures can be expected as most accurate to the real, measurable components