Incomplete modeling when using MOS capacitor changing from inversion into depletion: A comparator design as an example

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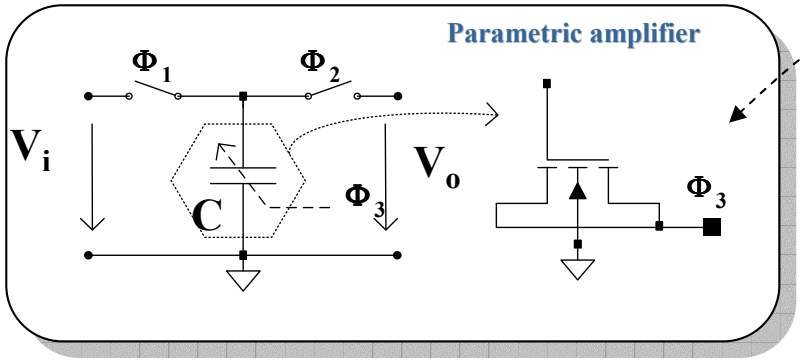
Introduction / Outline

A new comparator architecture has been developed around a input sampling switched-capacitor network with embedded pre-amplification. This amplification gain is obtained by a discrete-time operation in which a sampled input signal is held and boosted as a consequence of a MOS gate-to-ground capacitance reduction, while maintaining the total gate charge [1].

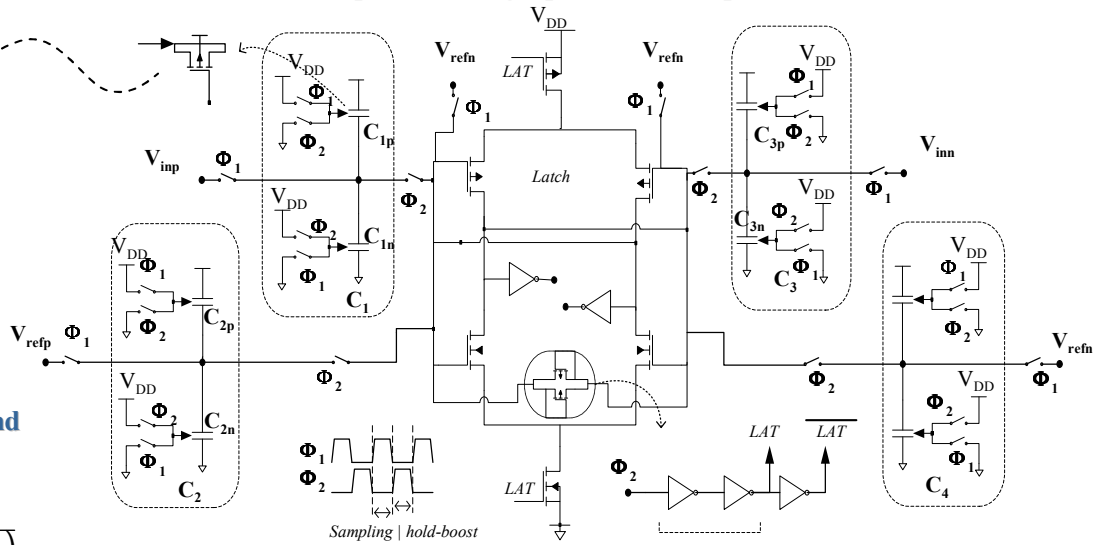


Input sampling network defines the comparison level and gain is obtained by changing the capacitance values

$$V_{12d}^{\phi 2} = \left(V_{ind} + \frac{V_{refd}}{\alpha_c} \right) \cdot \frac{\alpha_c \cdot k_{c13}}{\alpha_c + k_{c13}/k_{c24} \cdot \left(1 + C_L / C_{24,\phi 2}\right)}$$

$$C_{13,\phi 1} = k_{c13} \cdot C_{13,\phi 2}, \quad C_{24,\phi 1} = k_{c24} \cdot C_{24,\phi 2}$$

Comparator using a parametric amplifier



A gain of 2.5 can be achieved with $C_{13,ø1}=4*C_{24,ø1}$.

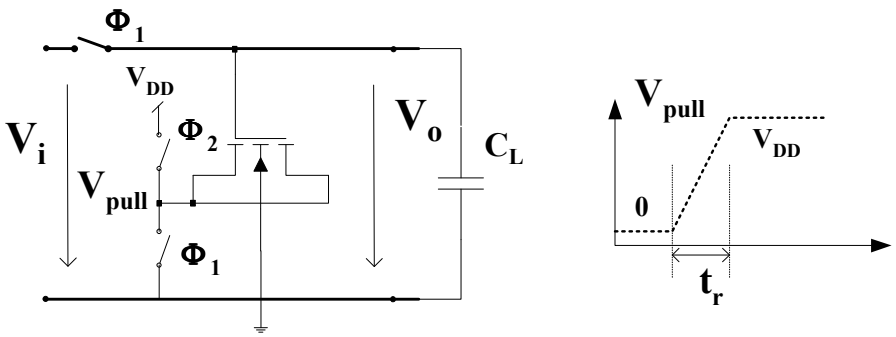
In a MOS transistor, this capacitance reduction can be accomplished by moving the transistor from **inversion into depletion** [1].

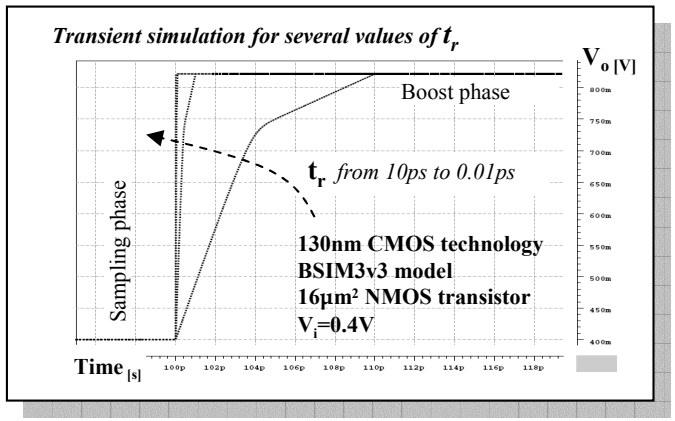
The parametric amplification speed depends also on the time needed to remove the inversions charges from the transistor channel. Therefore spice simulations have been carried out using **BSIM3v3** model, to find the maximum operation speed of the amplifier (and comparator).

1.S. Ranganathan, Y. Tsividis, "Discrete-Time parametric amplification based on a three-terminal MOS varactor: analysis and experimental results", *IEEE, J. Solid State Circuits*, no. 12, pp. 2087-2093, Dec. 2003.

Main results / Summary

Parametic amplifier

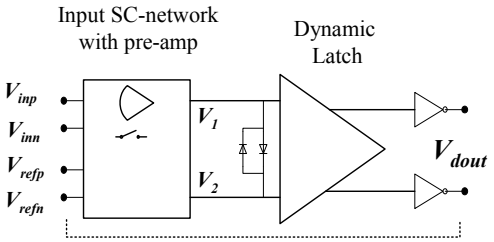


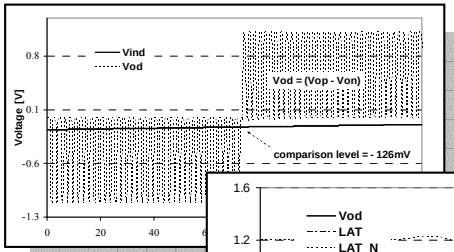


Simulations are not fully clear about the minimum time needed by the parametric amplifier to achieve the boost step, since they indicate a extremely low value for this transient time (lower than 0.01ps, in this case).

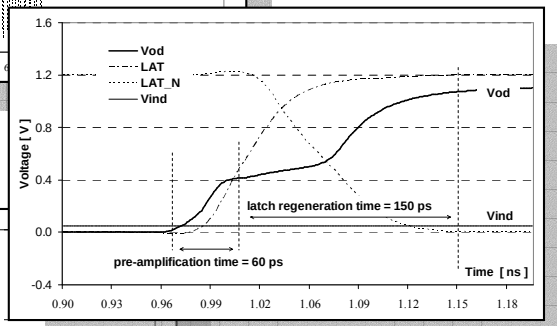
Some degree of theoretical validation/confirmation is needed on the BSIM3v3 model concerning the minimum time needed to remove charges from the channel of a NMOS device that changes from inversion into depletion region.

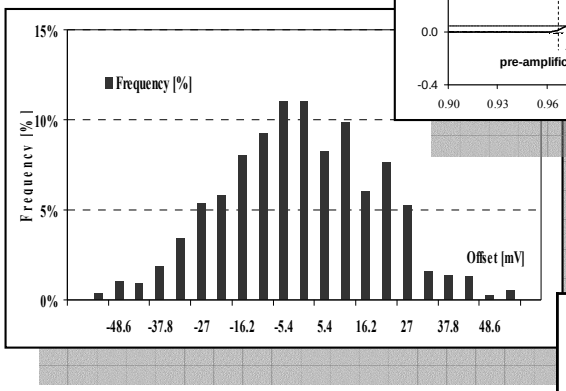
Comparator





Comparator Time response





Offset distribution from 800 Monte-Carlo SPICE simulations

Item	*value*
Technology	130 nm CMOS
Supply voltage	1.2 V
Power dissipation @ Fs=500MS/s	142µW
Regeneration time	210 ps
Offset standard deviation	20.3 mV
Input Capacitance (single-ended)	85 fF (sampling phase)
Energy Efficiency	0.14 pJ (per comparison)