Small-signal Modelling of SOI-specific MOSFET Behaviours

D. Flandre

Microelectronics Laboratory (DICE), Research Center in Micro- and Nano-Scale Materials and Electronics Devices (CeRMIIN), Université catholique de Louvain (UCL)
Louvain-la-Neuve, Belgium
denis.flandre@uclouvain.be
“SOI-specific device behaviors: Challenges for compact modelling as well as parameter extraction and process engineering?”

1. Introduction
2. Specific phenomena
3. Recent scaling effect
4. Conclusion

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1. Silicon-on-Insulator (SOI)

Partially Depleted vs. Fully Depleted

\[ V_{th} \neq f(T_{BOX}, T_{Si}) \]

\[ \Rightarrow \text{Easier to manufacture at present (IBM, AMD...)} \]

\[ \Rightarrow \text{Less industrialized (only OKI 0.15 \( \mu \)m),} \]

\[ \text{but higher promises (UTB, FinFET...)} \]
Basic I-V behavior

Partially Depleted vs. Fully Depleted

\[ V_{th,front} \neq f(V_{Gb}) \]
But \( \sqrt{V_B} \)
As in bulk CMOS

\[ V_{th,front} = f(V_{Gb}) \]
But linear and lower coupling
vs. Bulk and PD

In both cases, to 1st order, I-V curves as in bulk
⇒ Similar models but with adequate parameters:
BSIMSOI (+ EKV, PSP under development)!
Partially-depleted SOI MOSFET

Floating substrate node $V_B$

- normal operation: $V_B - V_S$
  $V_{ch} - V_B \rightarrow \gamma$ as in bulk

- far in saturation: $I_{ii}$
  $V_B > V_S \rightarrow V_{th} \downarrow, I_D \uparrow$

Impact Ionization, Gate tunneling $\rightarrow$ Hole current in n-MOS

Also parasitic bipolar effect!
NMOS (W=10µ, L=0.25µ) @ VGS=1V

Trade area vs FBE, but care with tie efficiency, i.e. resistance!

PD SOI
BT = « Body tie »
P+ - substrate contact To source or ground
NMOS (W=10µ, L=0.25µ) @ VGS=1V

PD SOI : FB = Floating body
Beneficial for current increase, i.e. speed,
But dynamic couplings can be detrimental!
Delay Time between DC point measurements

What is DC?
Floating-body effects (FBE) compact modelling

All static and dynamic Body (B) couplings to G, S, D and Gnd
⇒ • History effects
• AC/RF effects on small-signal parameters

Introduced in major models: BSIMSOI ...
But requires careful parameter extraction!
Output conductance vs. Frequency

Wideband frequency measurements = solution for parameter extraction!
Output conductance vs. Frequency

*Wideband* = from DC to … > GHz

**FB** : \( f_{\text{pole}} < f_{\text{zero}} \)

**BT** : \( f_{\text{pole}} > f_{\text{zero}} \)
Output conductance : Modelling

\[ g_d = g_{dsi} + g_{mbi} \text{Re} \left[ \frac{v_{bi}}{v_{di}} \right] \]

\[ \Rightarrow \frac{g_{bdsi} + j\omega C_{bdi}}{g_{bdi} + j\omega C_{bdi}} \]
Output conductance: Modelling

\[ g_{bbi} = g_{jbsi} + g_{jbsi} + R_{be}^{-1} \]

\[ C_{bbi} = C_{bbsi} + C_{bsdi} + C_{bgdi} \]

\[ f_p = \frac{1}{2\pi} \frac{g_{bbi}}{C_{bbi}} \]

\[ f_{0,kink} = \frac{1}{2\pi} \frac{\sqrt{g_{bbdi} g_{bbi}}}{\sqrt{C_{bbdi} C_{bbi}}} \]
Output conductance: Modelling with BSIM

Need for extraction: $C_{gb}$, $g_{bs}$, $C_{bs}$, $g_{bd}$, $C_{bd}$…!
Self-heating

Observations: large $V_g$ and $V_d$ → negative conductance
$I_{static} < I_{dynamic}$

Origin:
- buried oxide = thermal isolator
- power not dissipated in substrate
- device temperature $\uparrow$
- $\mu, I_D \downarrow$

important for device characterization, not for LVLP circuit operation

motivation to scale BOX to increase heat evacuation?
Frequency response of output conductance

**Self-heating**

**Floating body (PD)**

\[ g(f) = g_{\text{intr}} + g_{\text{SH}}(f) + g_{\text{FB}}(f) \]

- **SH**
  - kink-effect
  - no SH
  - \( f \approx 10^5 - 10^7 \) Hz

- **kink**
  - no kink
  - \( f \approx 10^2 - 10^6 \) Hz

- **body C-coupled**
  - before kink
  - \( f \approx 10^2 - 10^8 \) Hz


III. Recent scaling effect

Length and BOX scaling

⇒ **SFBE:** Substrate Floating Body Effect on $g_m$ and $g_d$

High frequency exp.

FD SOI MOSFET: $L_{\text{eff}}=0.16\mu$m, $W=16\times6.6\mu$m, $V_D=V_G=1V$

Substrate coupling?

Difference with DC is due to SH (*in part*)

Kilchytska et al, IEEE EDL, 2004
Experimental results: Low frequency

FD SOI MOSFET: $L=90\text{nm}$, $W=5\mu\text{m}$, $V_D=1.5\text{V}$, $V_G=0.5\text{V}$

Not compatible with SH!

Kilchytska et al, IEEE EDL, 2007
2D Atlas device simulations

\[ G_{SD}, \mu \text{S}/\mu \text{m} \]

Conductance vs. Frequency, Hz

1\textsuperscript{st} transition

2\textsuperscript{nd} transition

3\textsuperscript{rd} transition

Self-heating

L=1 µm, \( V_D=V_G=1 \text{V} \)

With substrate

1\textsuperscript{st} and 3\textsuperscript{rd} tr. still present for simulation without SH

Without substrate

1\textsuperscript{st} and 3\textsuperscript{rd} tr. disappear for simulation without substrate

Kilchytska et al, ESSDERC, 2002
2D Atlas simulations: Influence of substrate bias

Reduced Output Conductance

\[ G_{SD} = G_{SD}(f) - G_{SD}(10 \text{ Hz}) \], \, \mu S/\mu m

Analogy with MOS capacitor

L=0.25\mu m; \, V_D=V_G=1V

accumulated BOX-substrate interface

inverted BOX-substrate interface

D. Flandre, Microelectronics Laboratory, CeRMiN

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Analytical substrate model

1\textsuperscript{st} tr. is due to inertia of minority carriers

3\textsuperscript{rd} tr. is due to inertia of majority carriers

1\textsuperscript{st} tr. in $G_{SD}(f)$

3\textsuperscript{rd} tr. in $G_{SD}(f)$
Equivalent macro compact model

Fully-depleted

\[ G_{SD} = g_{ds} + g_{SDsub} \]

\[ g_{SDsub} = g_{mb} \cdot \frac{v_{BGS}}{v_{DS}} = (n_{FD} - 1) \cdot g_m \cdot \frac{v_{BGS}}{v_{DS}} \]

\[ v_{BGS} \approx \frac{C_{BDG}}{C_{BDG} + C_{SBG} + C_{GBG} + C_{sub}} \cdot v_{DS} \]
Substrate Coupling: Scaling trend

Reduced $G_{SD}$ (µS/µm)

Amplitudes of substrate-related transitions in $G_{SD}$ increase very strongly with BOX thinning!!!

Kilchytska et al, ULIS 2007
Conclusions

SOI specific « floating body » phenomena =

* special concern for new devices / circuits
  - characterization methods (wideband)
    - modelling and simulation
  - process engineering / optimization

* deserves attention for correct
  - performance assessment
    - parameter extraction
  - application (avoid detrimental effects, exploit benefits, opportunities)