UCL
Université catholique de Louvain

Small-signal Modelling of SOI-specific MOSFET Behaviours

D. Flandre

Microelectronics Laboratory (DICE),
Research Center in Micro- and Nano-Scale
Materials and Electronics Devices (CeRMiN),
Université catholique de Louvain (UCL)
Louvain-la-Neuve, Belgium
denis.flandre@uclouvain.be

UCL
Université catholique de Louvain

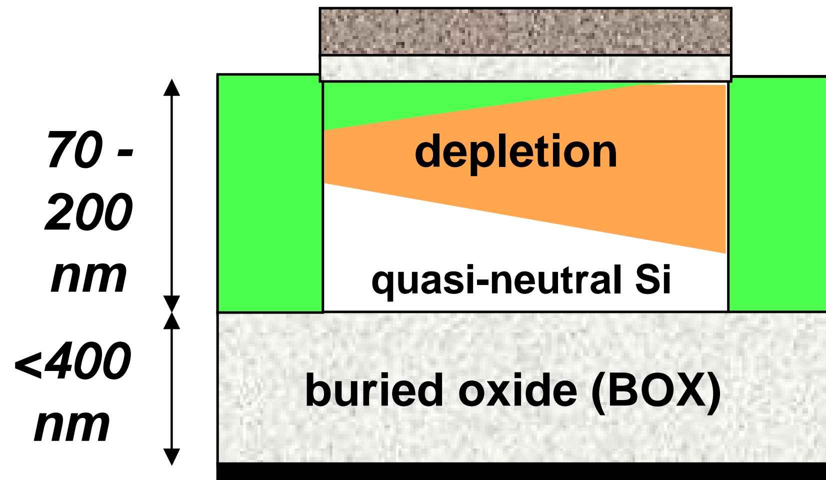
“SOI-specific device behaviors: Challenges for compact modelling as well as parameter extraction and process engineering ?”

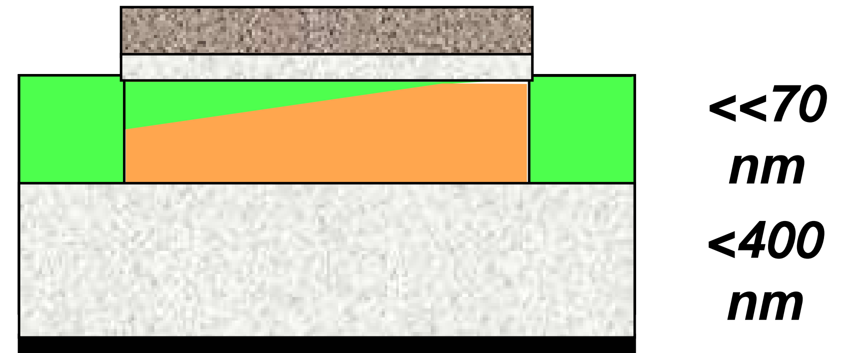
1. Introduction
2. Specific phenomena
3. Recent scaling effect
4. Conclusion

Acknowledgements : UCL colleagues (M. Bawedin, D. Lederer, D. Levacq, V. Kilchytska, P. Simon, J.-P. Raskin…), IMEC, LETI (for advanced devices), SINANO (EU Network)…

I. Silicon-on-Insulator (SOI)

Partially Depleted vs. Fully Depleted





$V_{th} \neq f(T_{BOX}, T_{Si})$

$\Rightarrow$ **Easier to manufacture at present (IBM, AMD…)**

$V_{th} = f(T_{BOX}, T_{Si})$

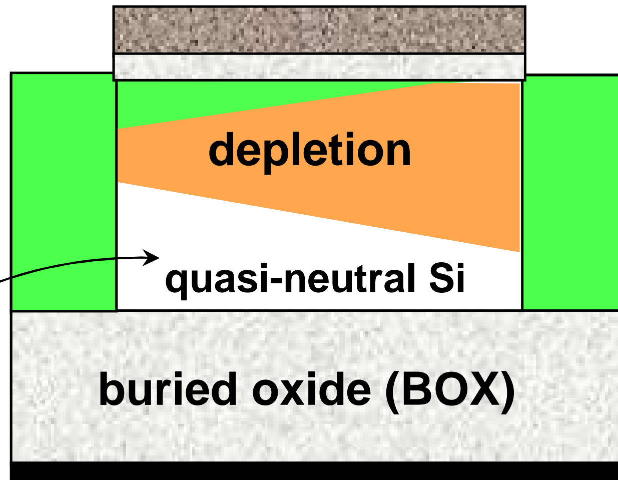
$\Rightarrow$ **Less industrialized (only OKI 0.15 µm),**

but higher promises (UTB, FinFET…)

UCL Université catholique de Louvain

Basic I-V behavior

Partially Depleted *vs.* *Fully Depleted*



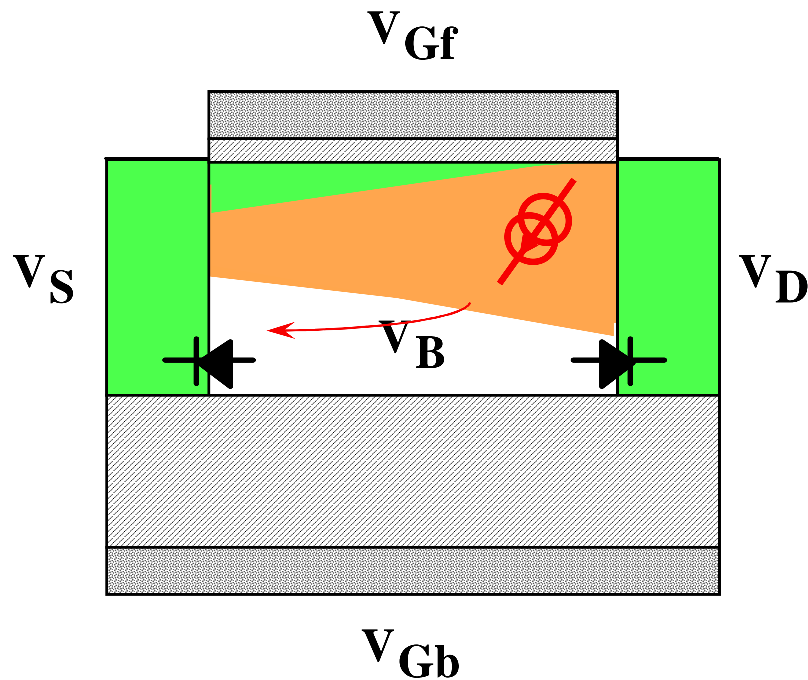
$V_{th,front} \neq f(V_{Gb})$
But sqrt (V_B)
As in bulk CMOS

$V_{th,front} = f(V_{Gb})$
But linear and lower coupling vs. Bulk and PD

In both cases, to 1st order, I-V curves as in bulk
⇒ Similar models but with adequate parameters : BSIMSOI (+ EKV, PSP under development) !

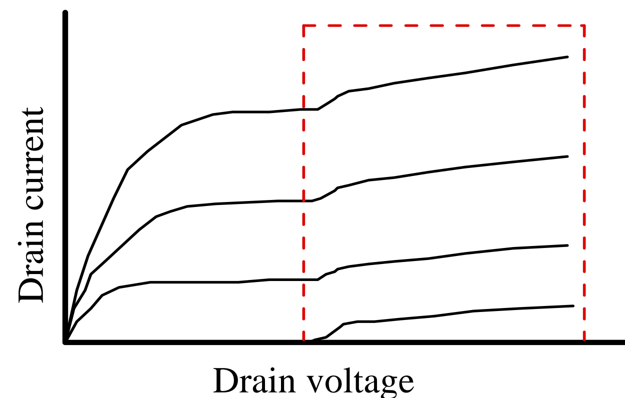
II. Specific SOI Phenomena

Partially-depleted SOI MOSFET



Floating substrate node V_B

- normal operation : V_B - V_S
  V_{ch} - V_B → γ as in bulk
- far in saturation : I_{ii}
  $V_B > V_S \rightarrow V_{th} \downarrow, I_D \uparrow$



« KINK Effect »

Impact Ionization, Gate tunneling
→ Hole current in n-MOS

Also parasitic bipolar effect !

NMOS (W=10µ, L=0.25µ) @ VGS=1V

ID (A): 0.00E+00, 2.00E-04, 4.00E-04, 6.00E-04, 8.00E-04, 1.00E-03, 1.20E-03, 1.40E-03

VD (V): 0, 0.2, 0.4, 0.6, 0.8, 1, 1.2, 1.4, 1.6

FD SOI

PD SOI FB

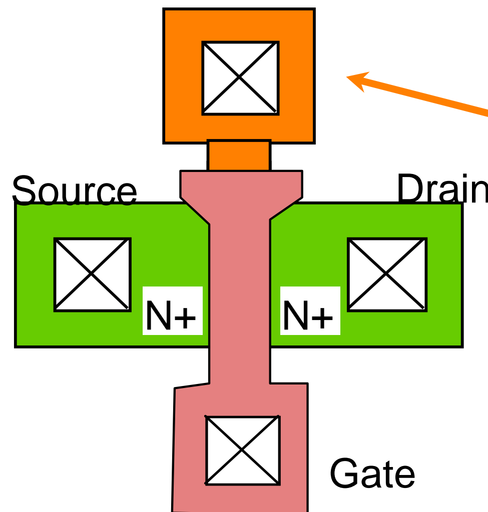
PD SOI BT

BULK

PD SOI

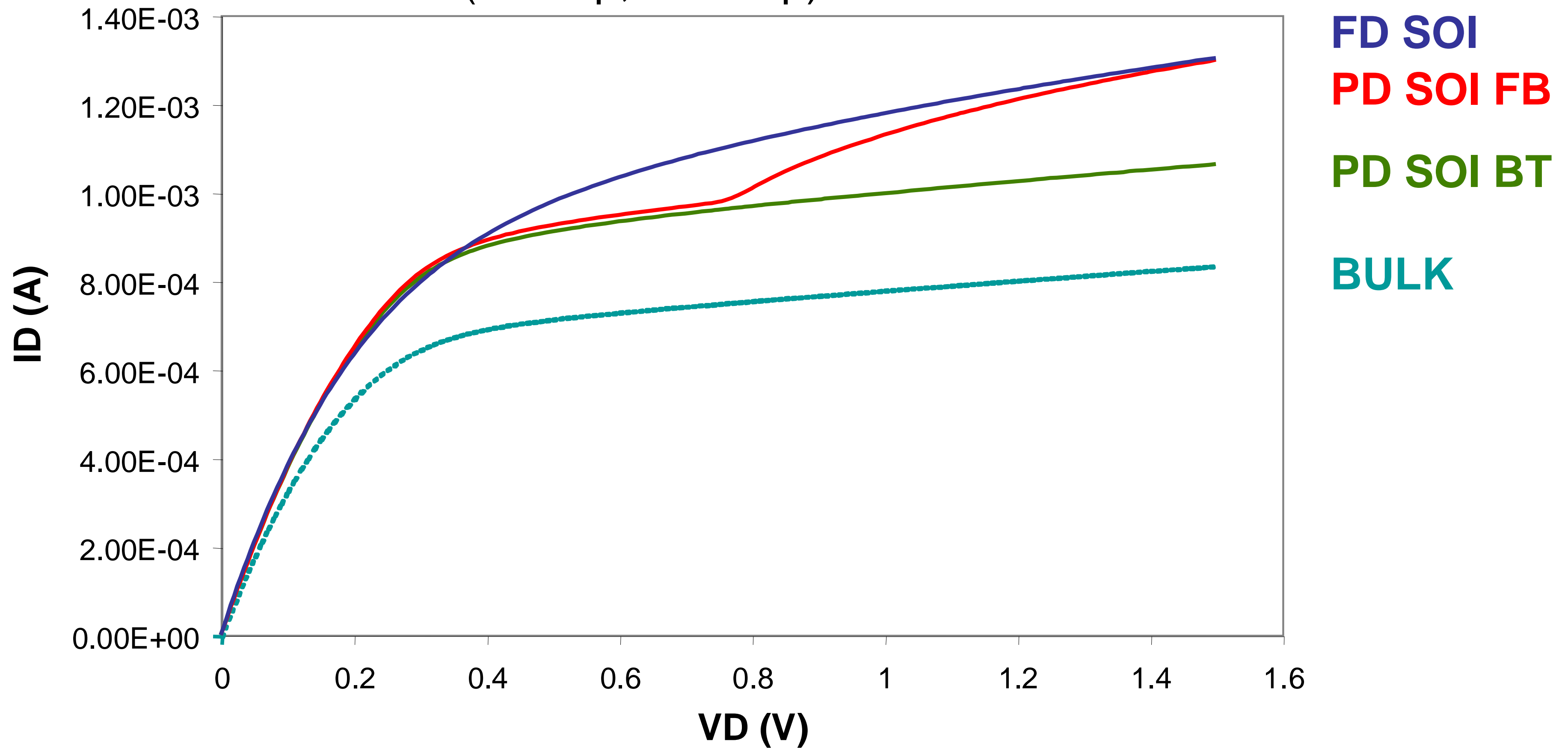
BT =

« Body tie »



P+ - substrate contact
To source or ground

Trade area vs FBE, but care with tie efficiency, i.e. resistance !

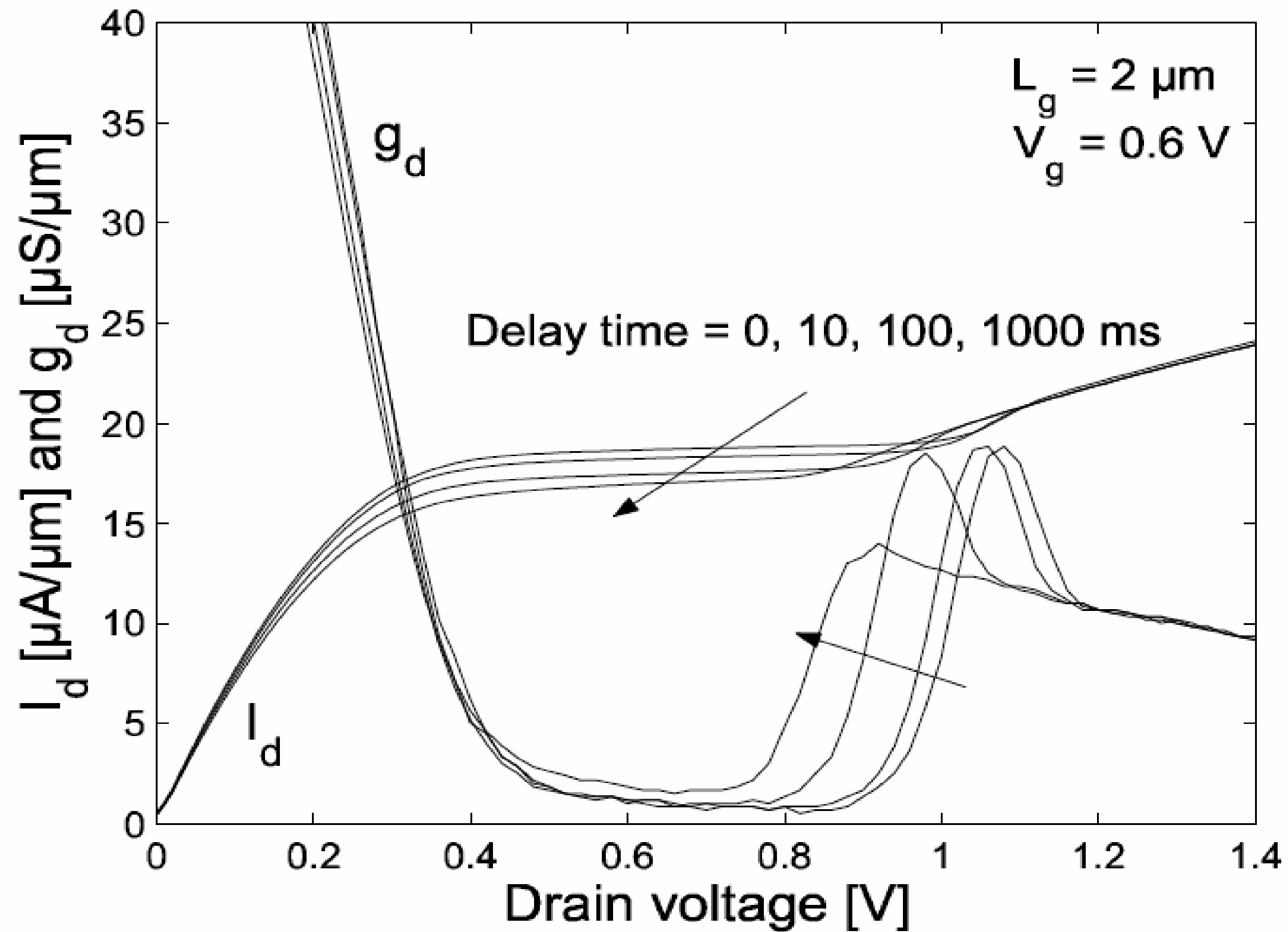


PD SOI : FB = Floating body

Beneficial for current increase, i.e. speed,

But dynamic couplings can be detrimental !

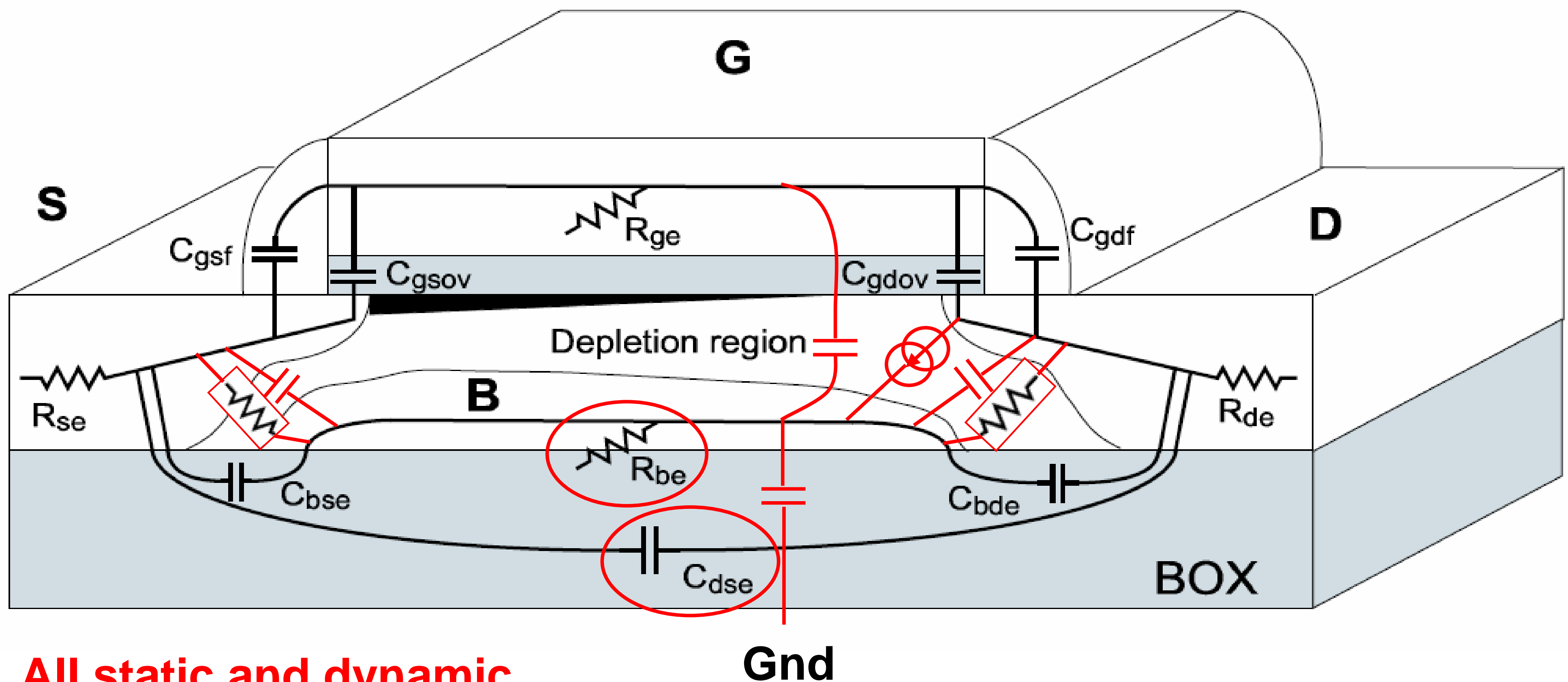
Delay Time between DC point measurements



What is DC ?

UCL Université catholique de Louvain

Floating-body effects (FBE) compact modelling



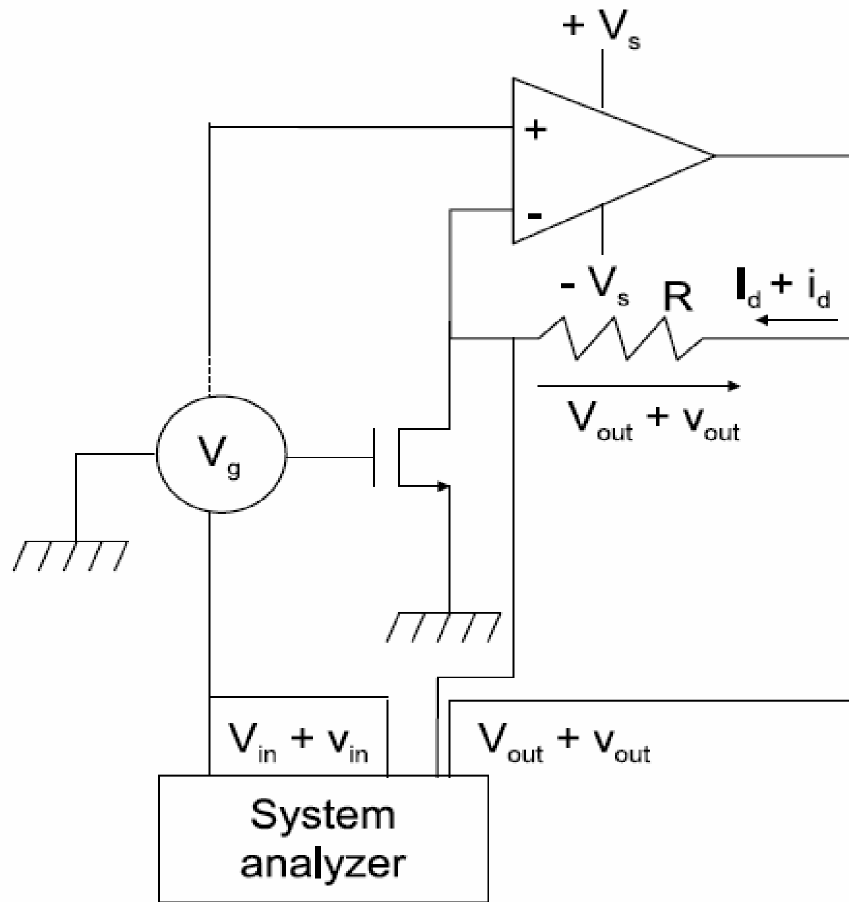
All static and dynamic Body (B) couplings to G, S, D and Gnd

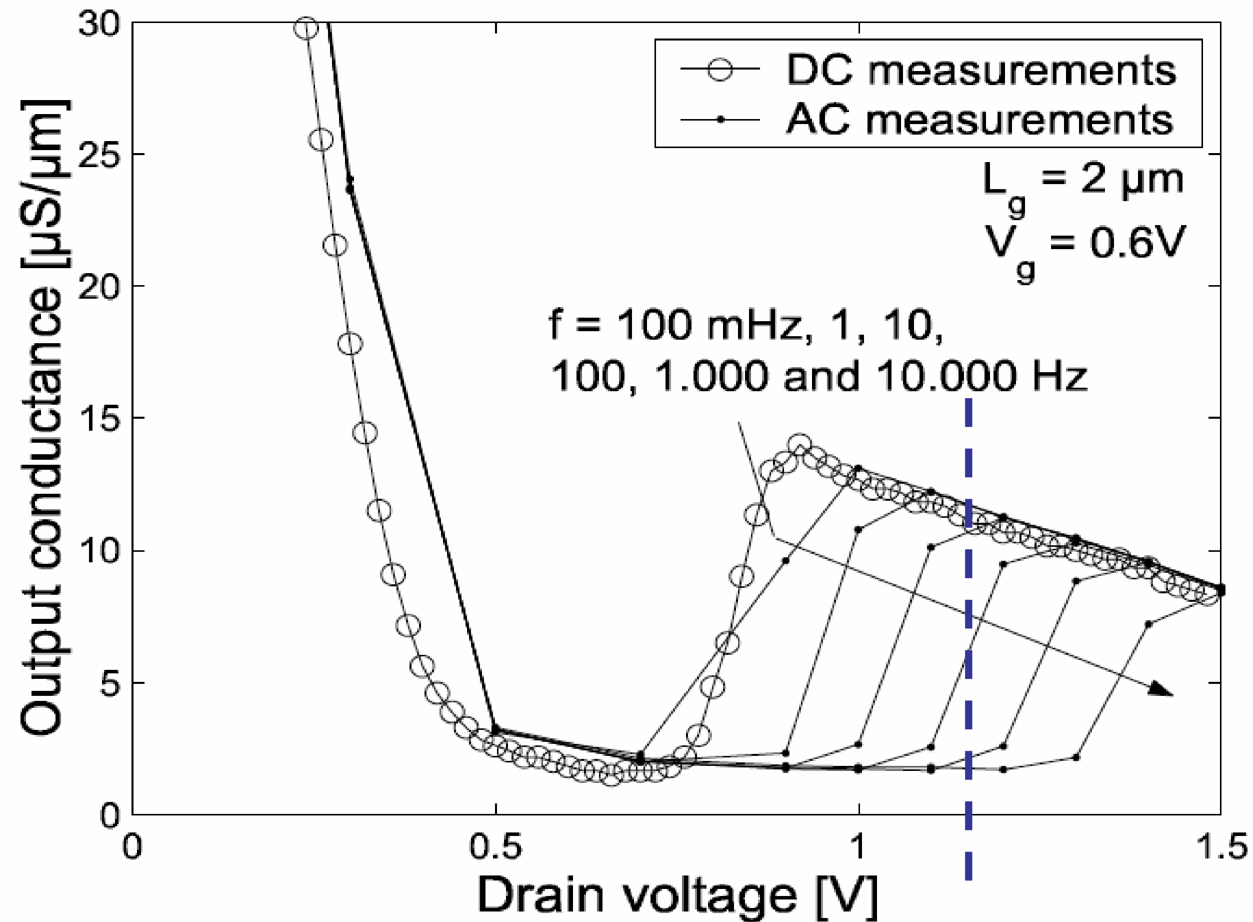
⇒ • History effects

• AC/RF effects on small-signal parameters

Introduced in major models : BSIMSOI … But requires careful parameter extraction !

Output conductance vs. Frequency

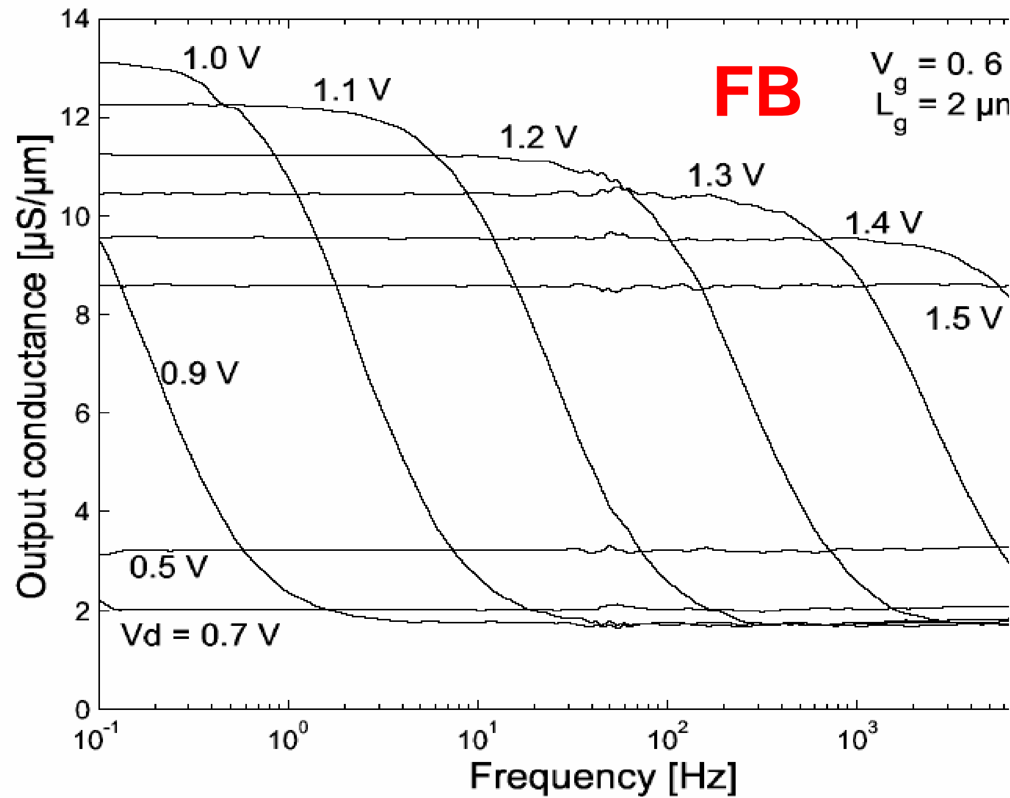


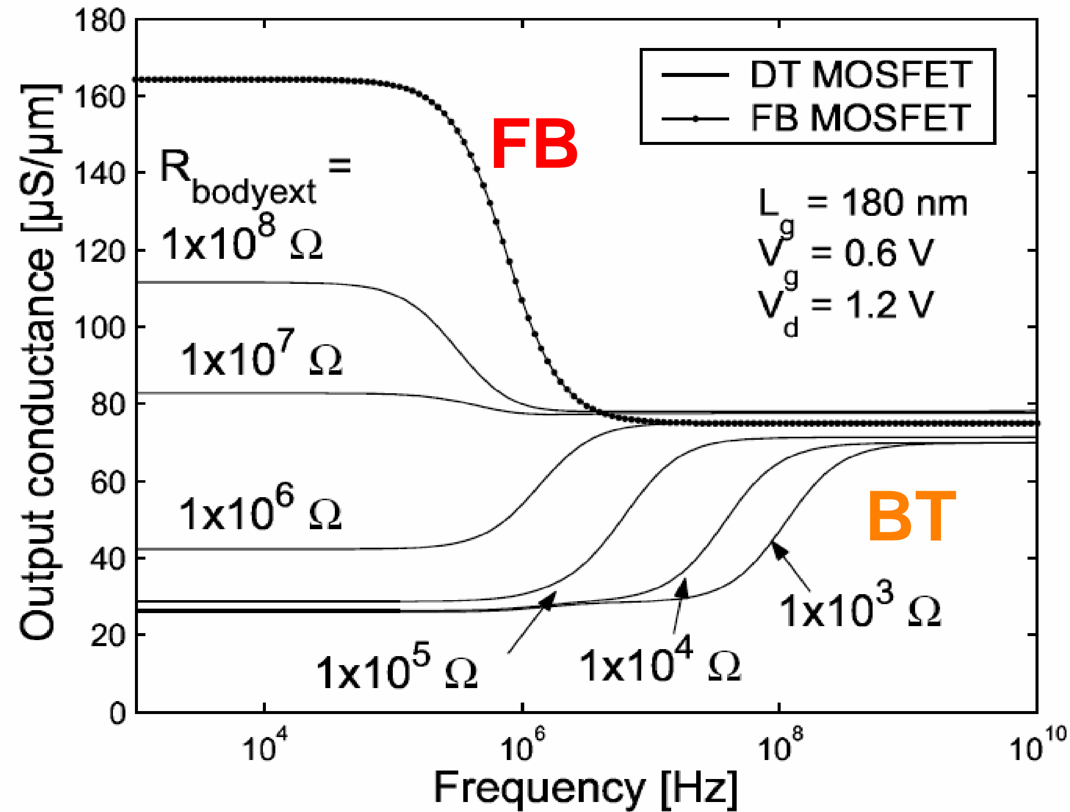


Wideband frequency measurements
= solution for parameter extraction !

Output conductance vs. Frequency

Wideband = from DC to … > GHz

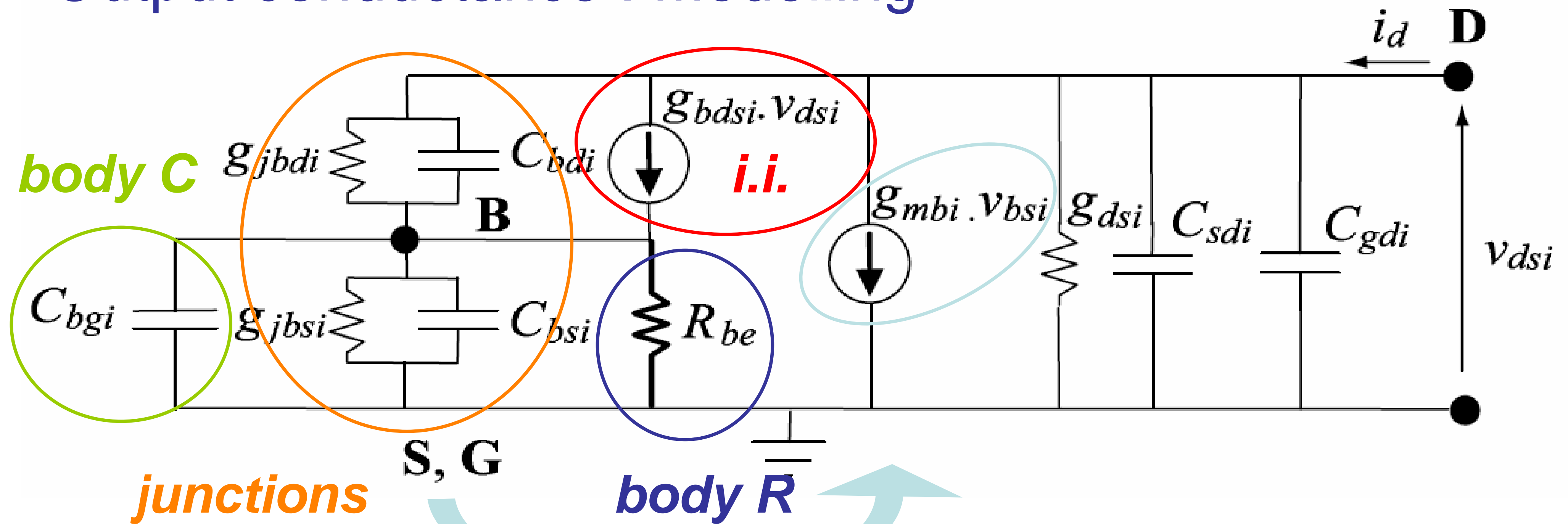




FB : $f_{pole} < f_{zero}$

BT : $f_{pole} > f_{zero}$

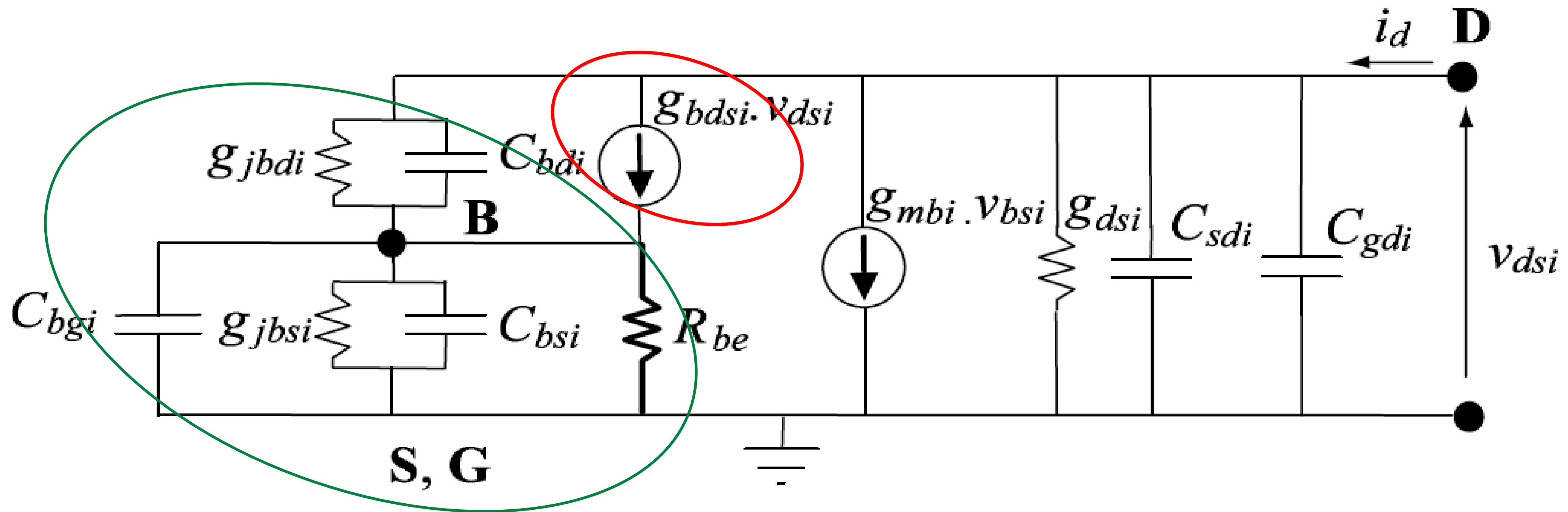
Output conductance : Modelling



$$g_d = g_{dsi} + g_{mbi} Re\left[\frac{v_{bi}}{v_{di}}\right]$$

$$\cong \frac{g_{bdsi} + j\omega C_{bdi}}{g_{bbi} + j\omega C_{bbi}}$$

Output conductance : Modelling



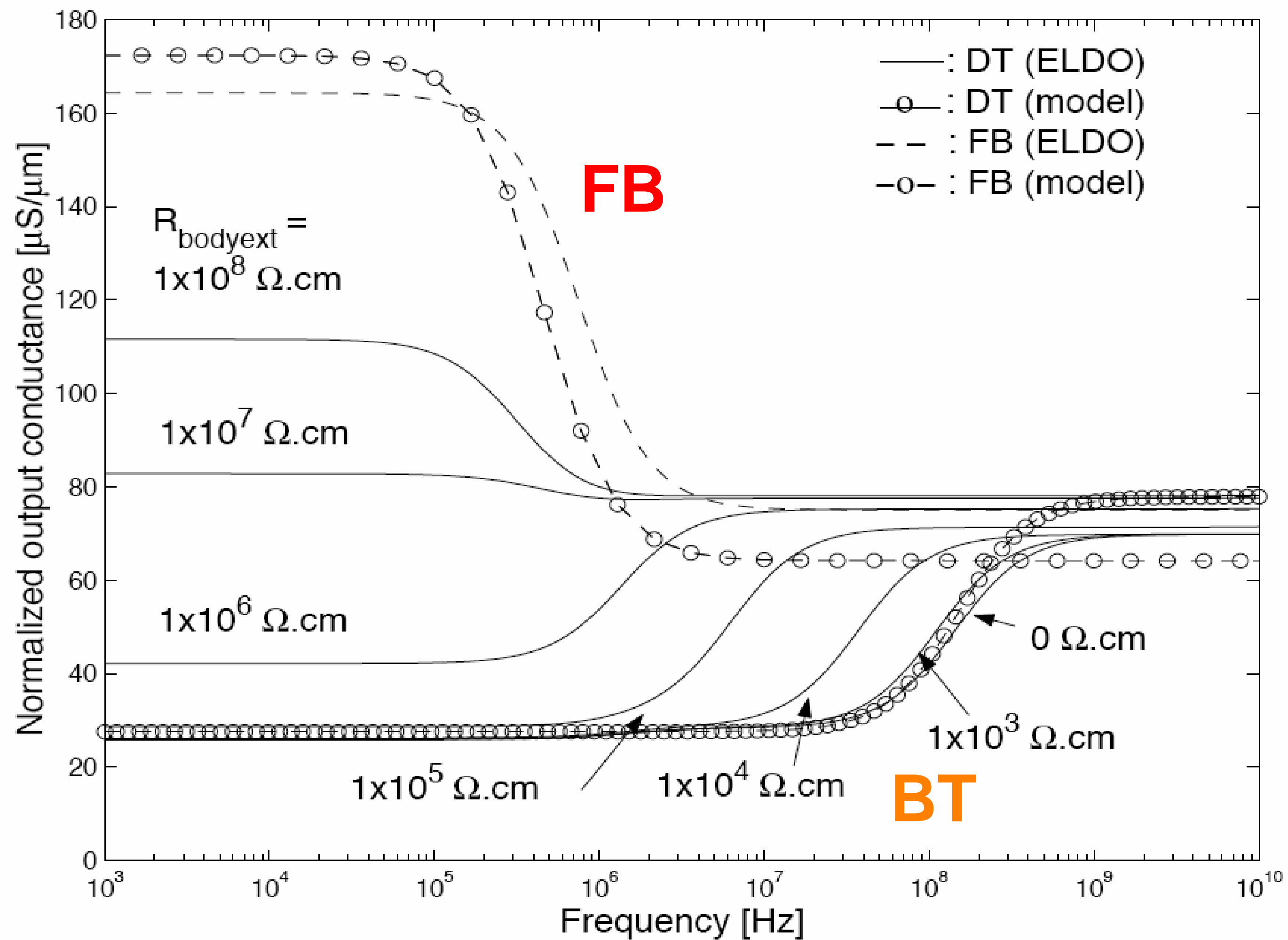
$$f_p = \frac{1}{2\pi} \frac{g_{bbi}}{C_{bbi}}$$

$$f_{0,kink} = \frac{1}{2\pi} \frac{\sqrt{g_{bdsi} g_{bbi}}}{\sqrt{C_{bdi} C_{bbi}}}$$

$$g_{bbi} = g_{jbsi} + g_{jbdi} + R_{be}^{-1}$$

$$C_{bbi} = C_{bsi} + C_{bdi} + C_{bgi}$$

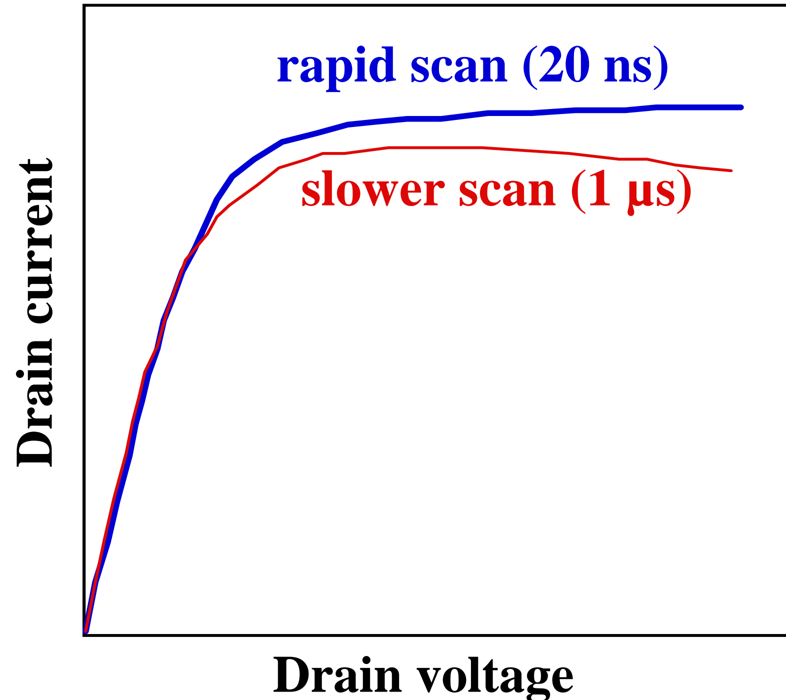
Output conductance : Modelling with BSIM



Need for extraction : C_{gb}, g_{bs}, C_{bs}, g_{bd}, C_{bd}… !

Self-heating

Observations : large Vg and Vd → negative conductance
Istatic < Idynamic



Origin : buried oxide = thermal isolator
⇓
power not dissipated in substrate
⇓
device temperature ↑
⇓
μ, I_D ↓

important for device characterization , not for LVLP circuit operation

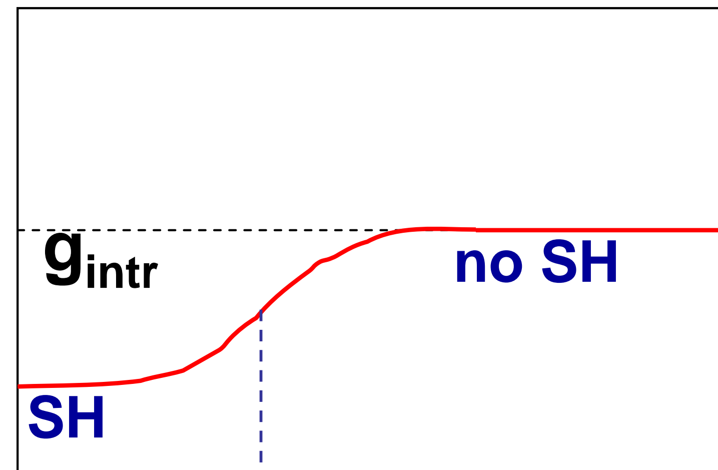
motivation to scale BOX to increase heat evacuation ?

UCL Université catholique de Louvain

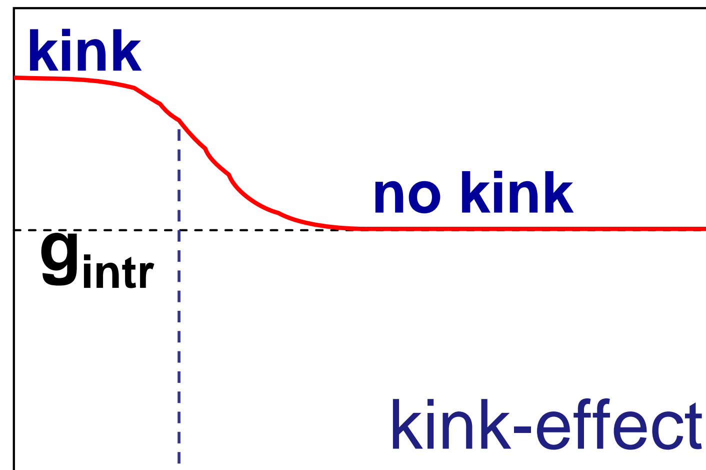
Frequency response of output conductance

Self-heating

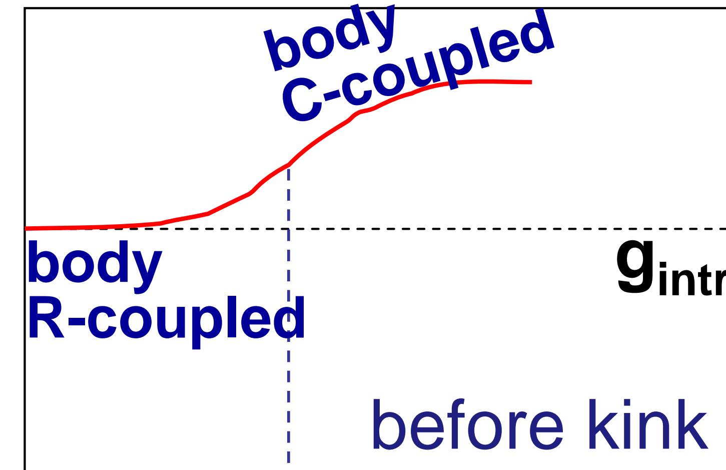
Floating body (PD)



f~10⁵-10⁷ Hz



f~10²-10⁶ Hz



f~10²-10⁸ Hz

$$g(f)=g_{intr}+g_{SH}(f)+g_{FB}(f)$$

W. Jin, W. Liu, S.K.H. Fung, P.C.H. Chan, and C. Hu, "SOI thermal impedance extraction methodology and its significance for circuits simulation", *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 730-735, 2001.

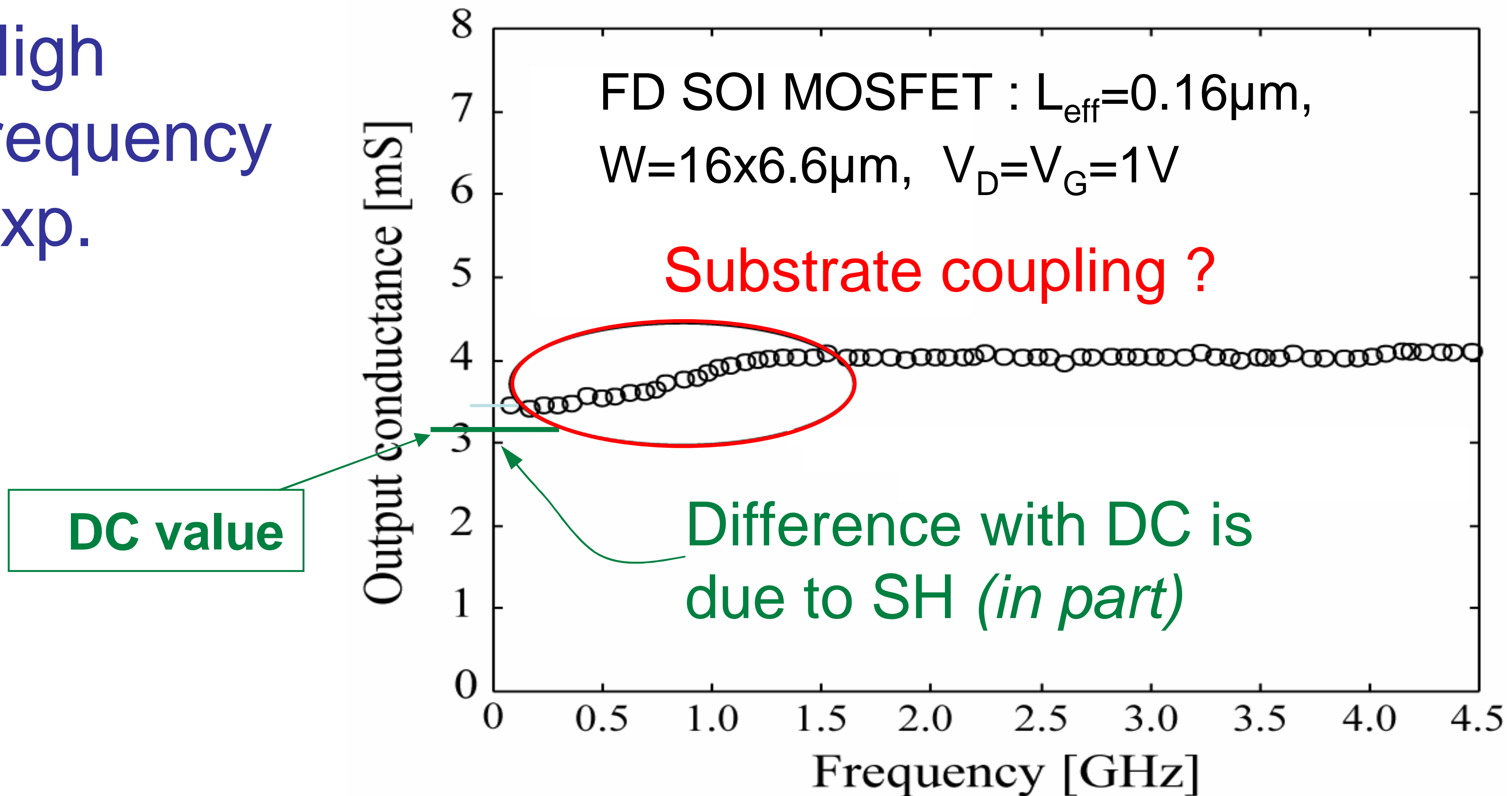
B.M. Tenbroek, W. Redman-White, M.J. Uren, et al., "Identification of thermal and electrical time constants in SOI MOSFETs from small signal measurements", *Proc. of 23rd ESSDERC*, Grenoble, France, Sept. 1993, pp.189-192.

III. Recent scaling effect

Length and BOX scaling

⇒ *SFBE: Substrate Floating Body Effect on g_m and g_d*

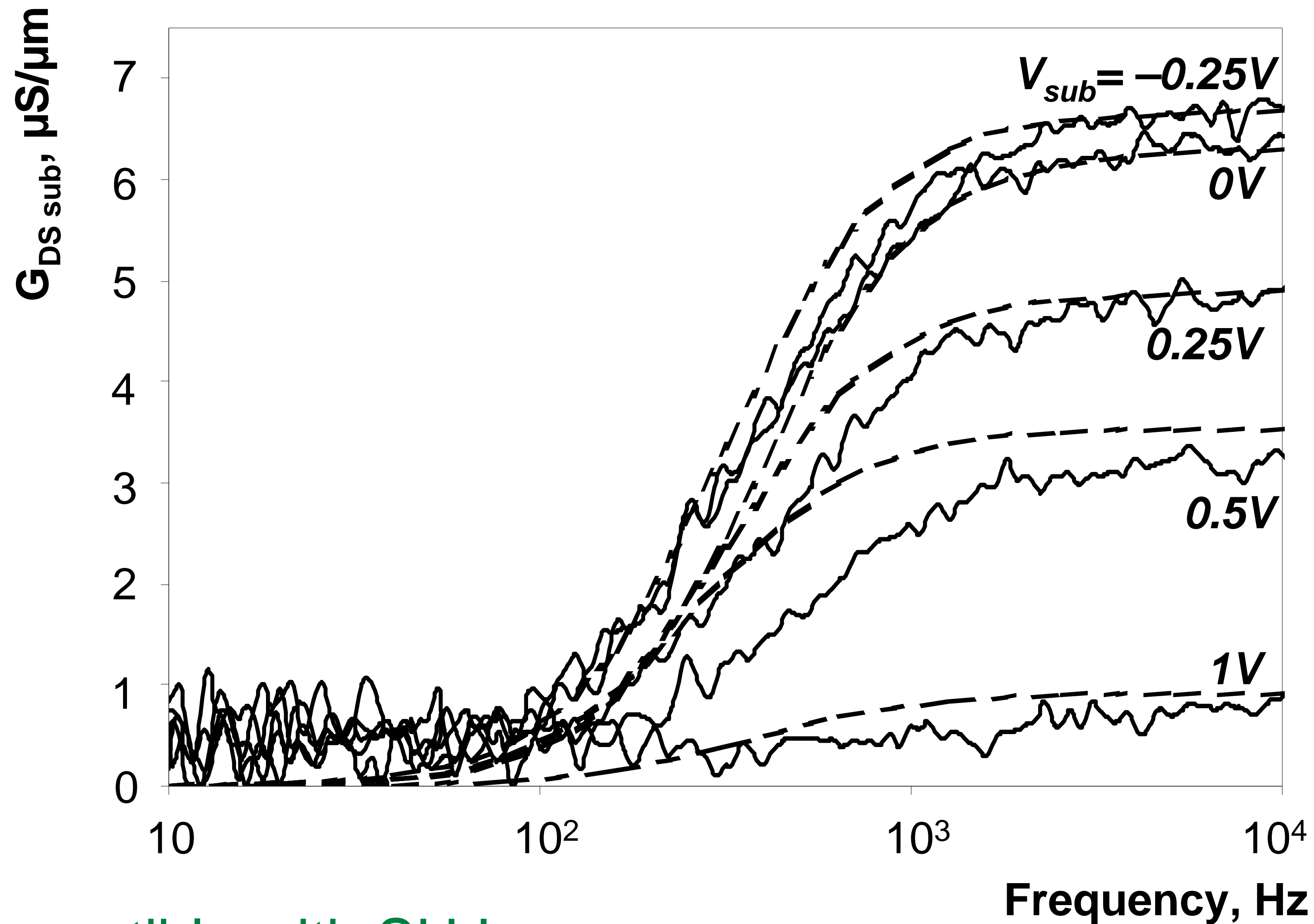
High frequency exp.



Kilchytska et al, IEEE EDL, 2004

Experimental results : Low frequency

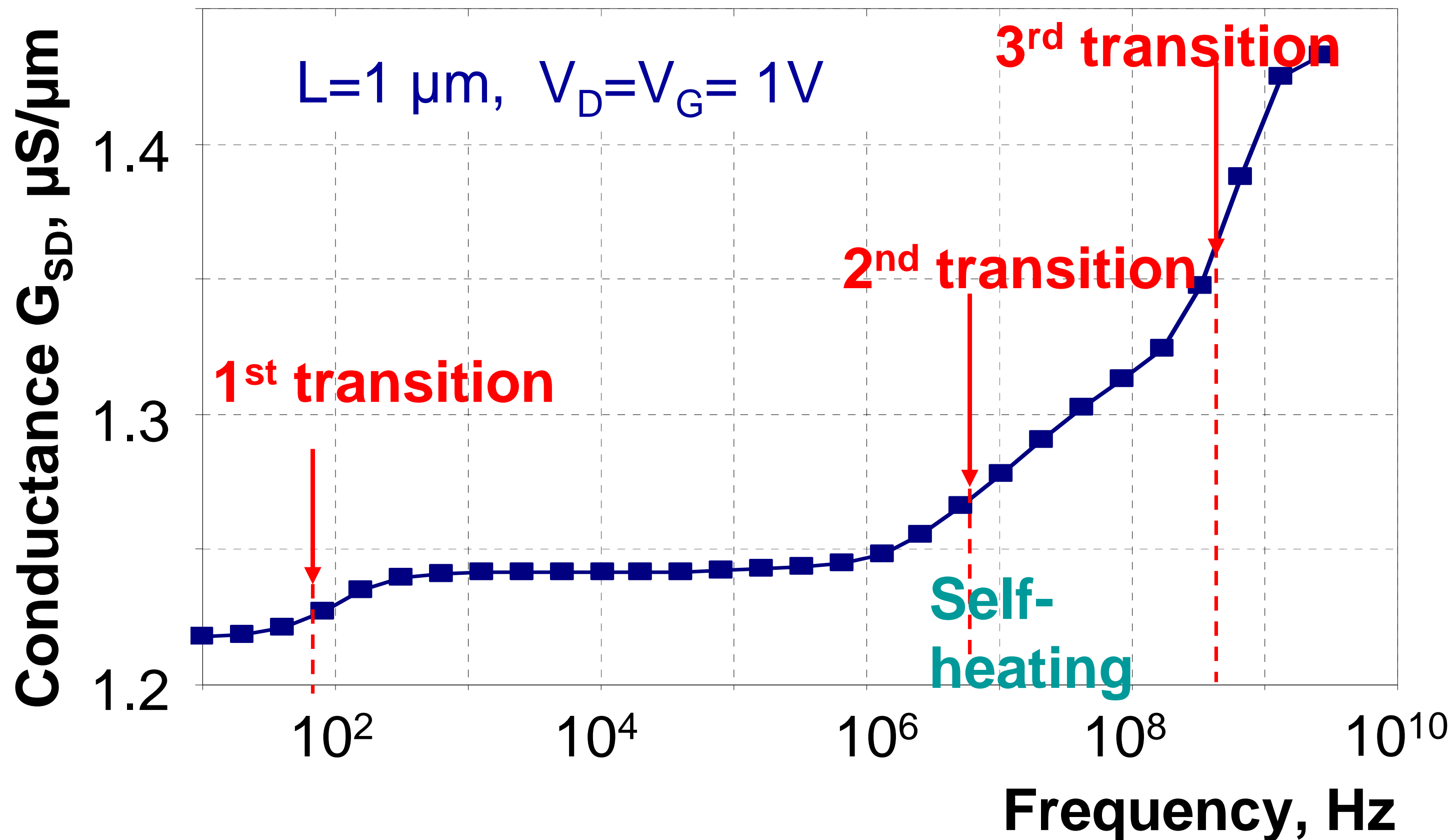
FD SOI MOSFET : L=90nm, W=5µm, V_D=1.5V, V_G=0.5V



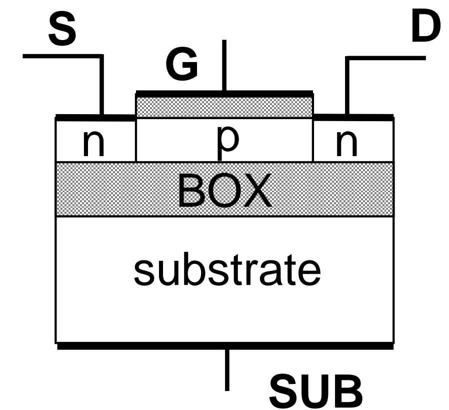
Not compatible with SH !

Kilchytska et al, IEEE EDL, 2007

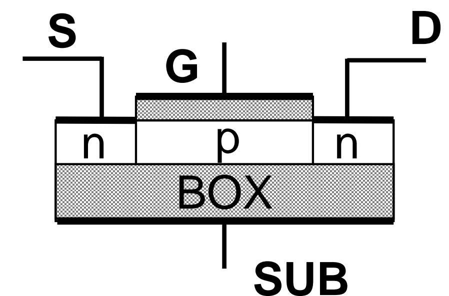
2D Atlas device simulations



With substrate



Without substrate

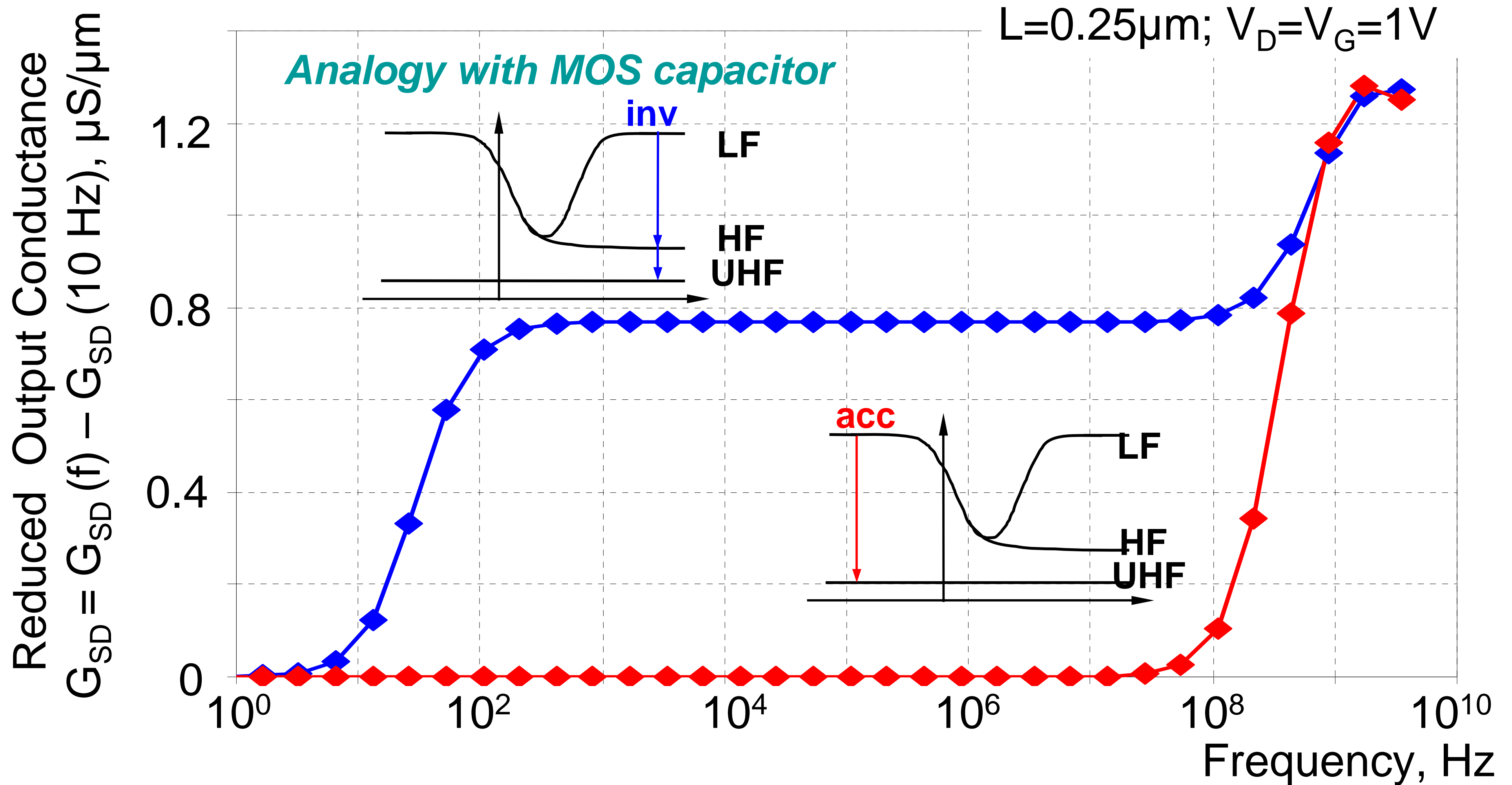


1st and 3rd tr. still present for simulation without SH

1st and 3rd tr. disappear for simulation without substrate

Kilchytska et al, ESSDERC, 2002

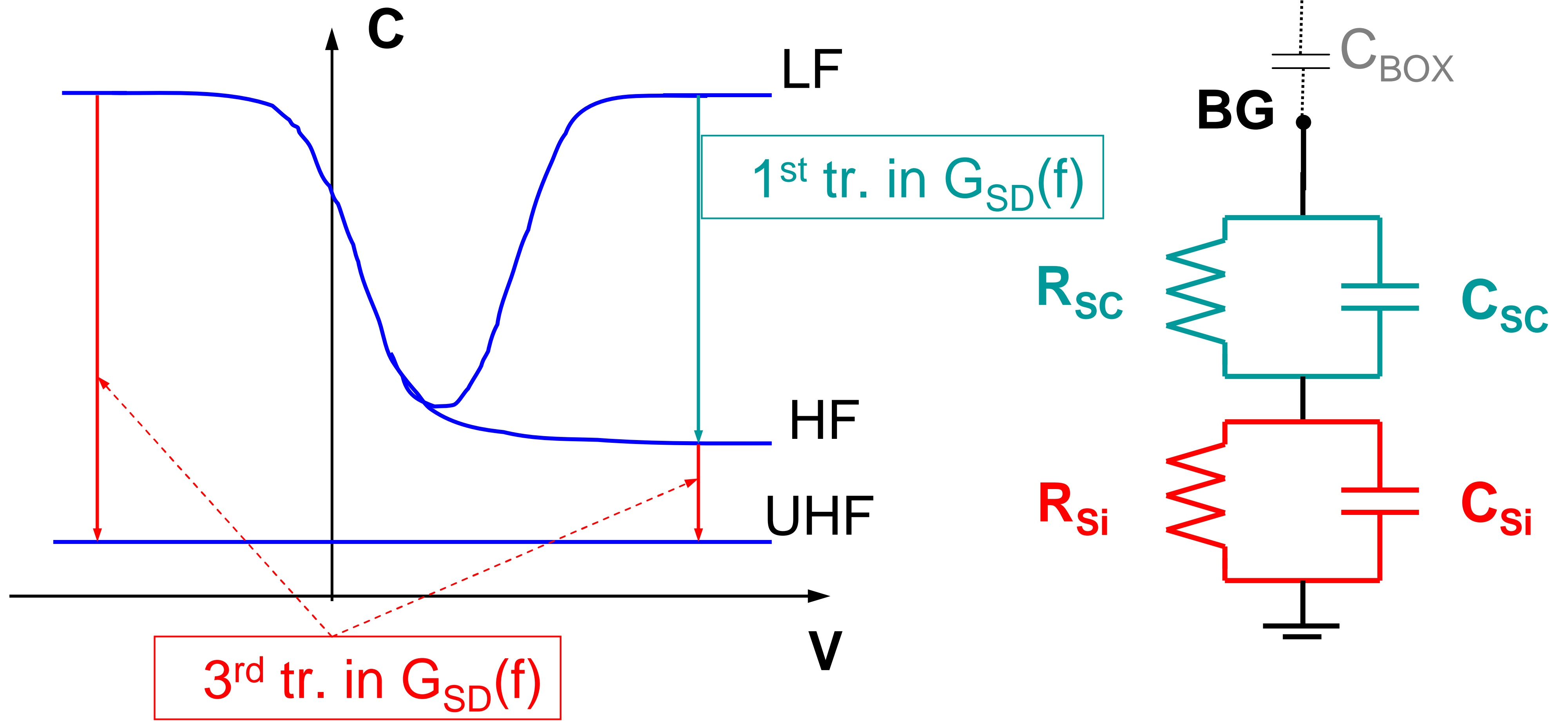
2D Atlas simulations: Influence of substrate bias



accumulated BOX-substrate interface → only 3rd tr. in $G_{SD}(f)$

inverted BOX-substrate interface → 1st and 3rd tr. in $G_{SD}(f)$

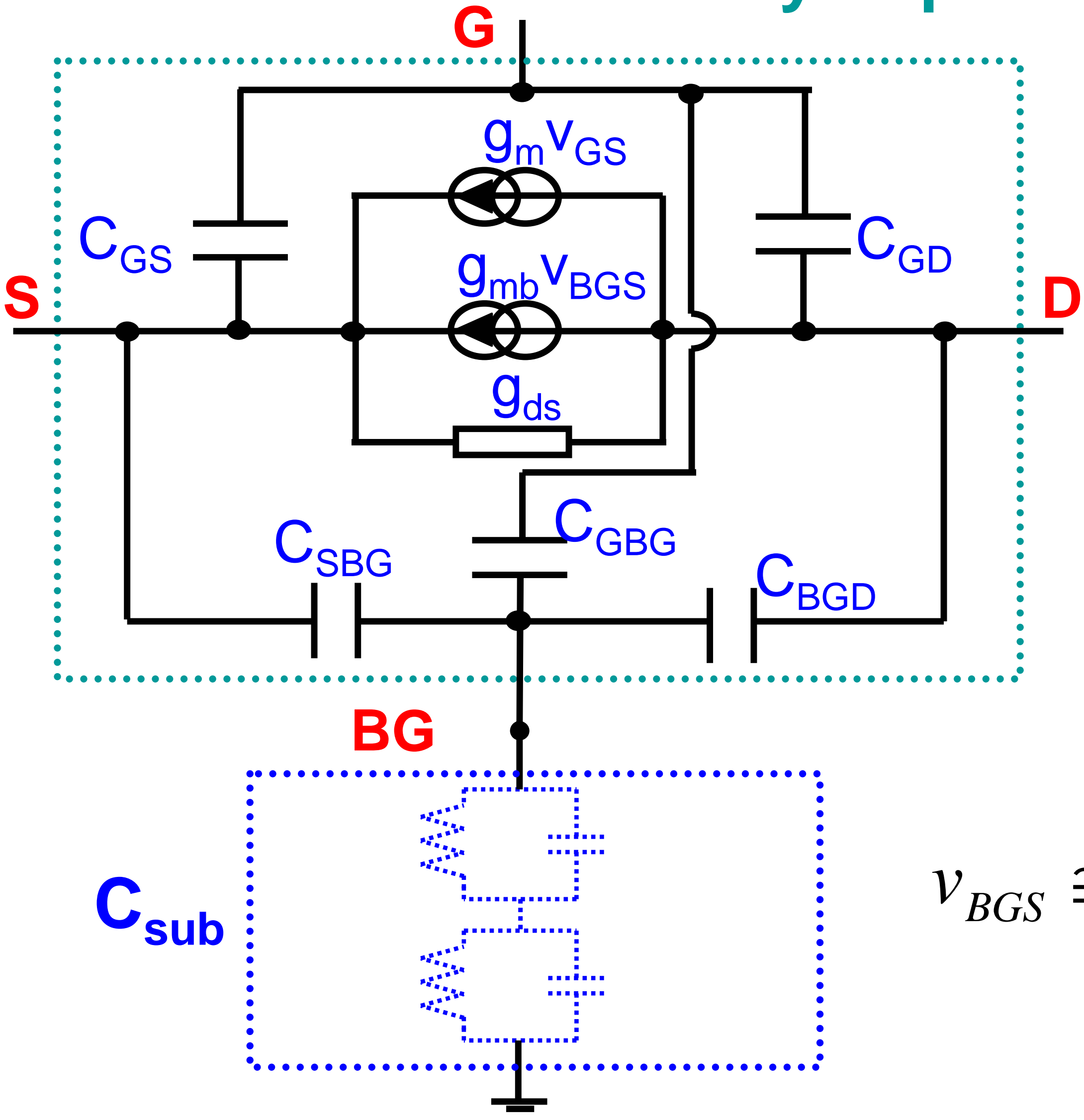
Analytical substrate model



1st tr. is due to inertia of minority carriers

3rd tr. is due to inertia of majority carriers

Equivalent macro compact model



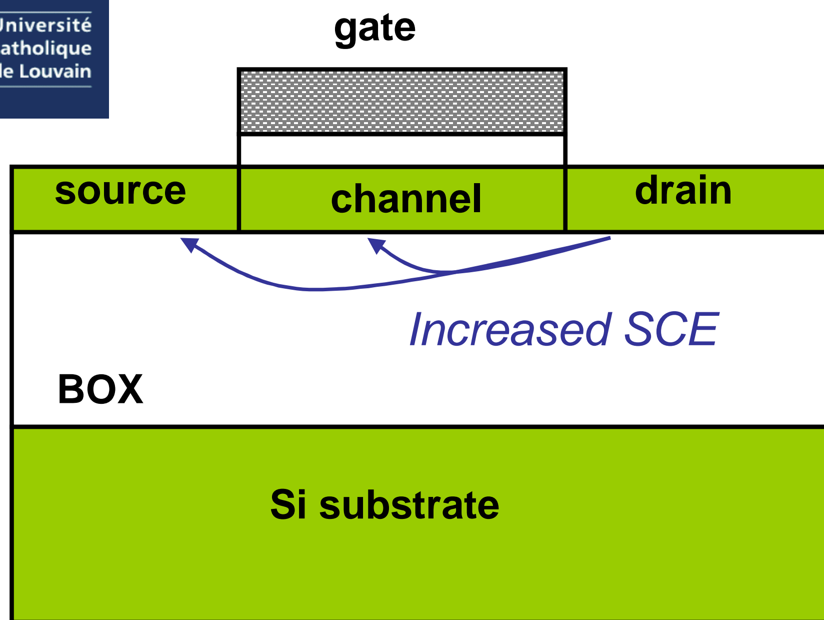
$$G_{SD} = g_{ds} + g_{SDsub}$$

$$g_{SDsub} = g_{mb} \cdot \frac{v_{BGS}}{v_{DS}} =$$

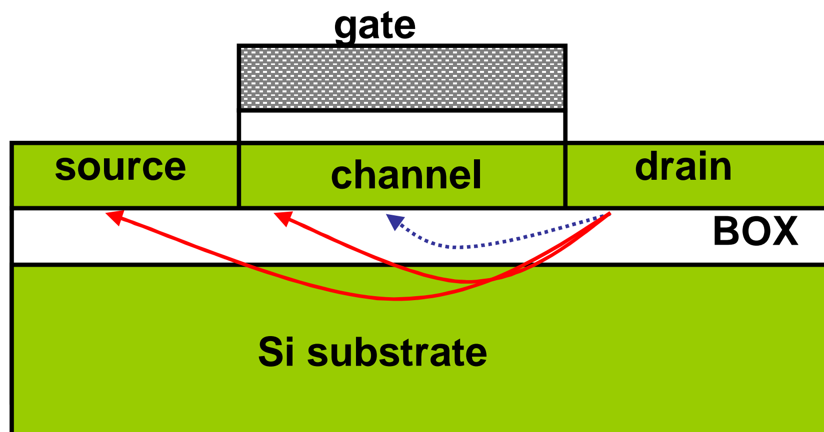
$$= (n_{FD} - 1) \cdot g_m \cdot \frac{v_{BGS}}{v_{DS}}$$

$$v_{BGS} \cong \frac{C_{BGD}}{C_{BGD} + C_{SBG} + C_{GBG} + C_{sub}} \cdot v_{DS}$$

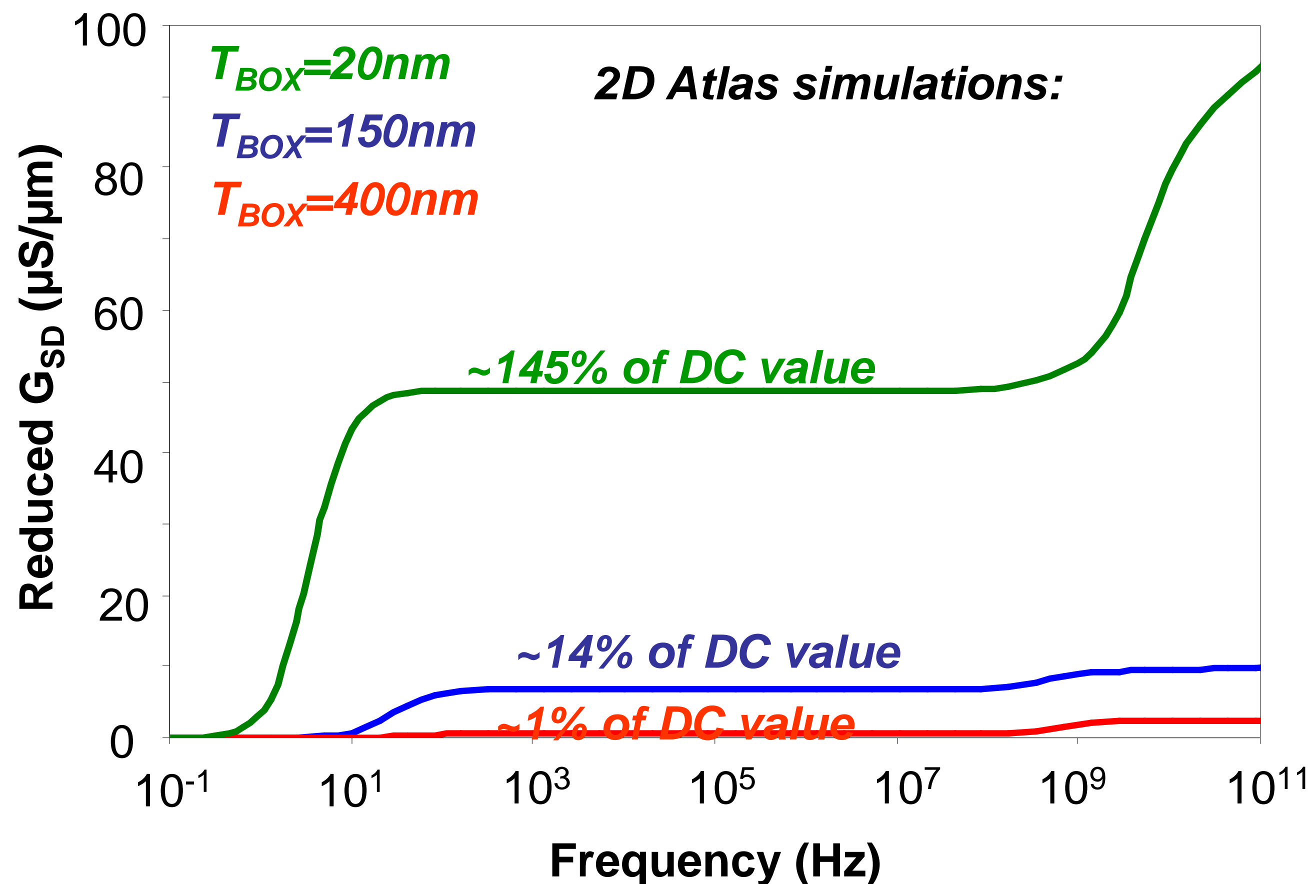
Substrate Coupling : Scaling trend



T_{BOX} ***shrinking***



SG FD SOI; L = 0.17 µm; Vg = 0.7 V; Vd = 1.5 V



Amplitudes of substrate related transitions in G_{SD} increase very strongly with BOX thinning!!!

Kilchytska et al, ULIS 2007

UCL
Université catholique de Louvain

Conclusions

SOI specific « floating body » phenomena =

* *special concern for new devices / circuits*

• characterization methods (wideband)
• modelling and simulation
• process engineering / optimization

* *deserves attention for correct*

• performance assessment
• parameter extraction
• application (avoid detrimental effects, exploit benefits, opportunities)