Modeling and Simulation of Nanomagnetic Logic with Cadence Virtuoso using Verilog-A

Gražvydas Žiemys, Simon Mendisch and Markus Becherer
Technische Universität München, Fakultät für Elektrotechnik und Informationstechnik, (D)

Nanomagnetic logic (NML) is one of the promising beyond CMOS technologies and is listed in the International Technology Roadmap for Semiconductors [1]. In recent years basic devices and small circuits, such as a full-adder, were demonstrated experimentally [2]. Moreover, the feasibility of monolithic 3D integration of NML was proven by a programmable majority gate, fabricated in two vertically stacked layers [3].

To explore the potential of Nanomagnetic logic, efficient and accurate compact models were developed, calibrated, and validated by statistical measurements on fabricated devices. Extensive micromagnetic simulations supported calibration of the presented compact models. Fig. 1. shows a statistical evaluation of the switching behavior of a nanomagnet by application of an external magnetic field [4]. In addition, Fig. 2. depicts the modular implementation of NML compact models integrated in industry standard Cadence Virtuoso tool where each of the shown parts of a magnet is described in Verilog-A file.

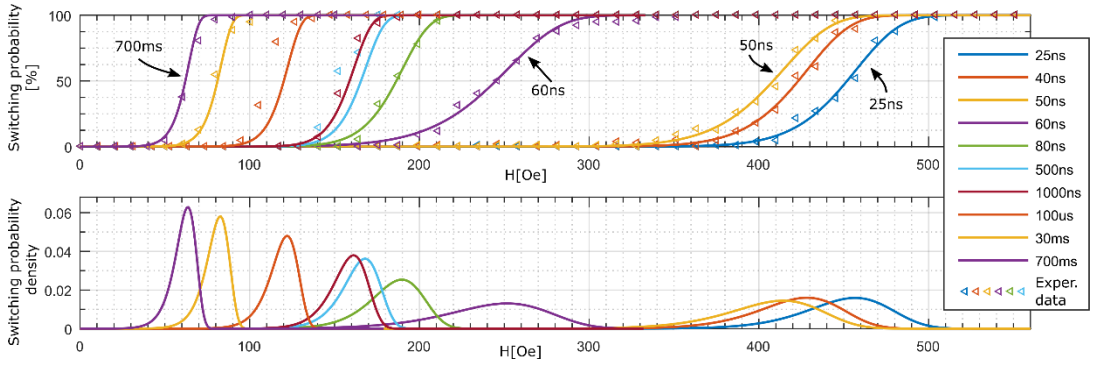

Fig. 1. (a) Switching probability of a single magnet. The solid line shows the Arrhenius equation fitted to the experimental data visualized by triangle markers. (b) Corresponding switching probability density. Single parameter set was used to model the data down to 100 ns pulses, after that each curve was fitted with designated $E_{0,ANC}$ and $H_{0,ANC}$ parameters.

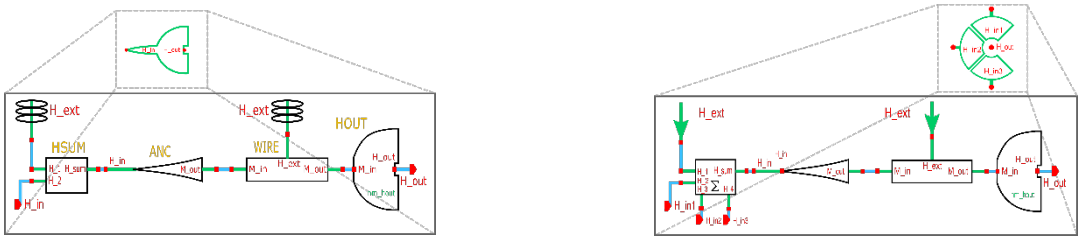

Fig. 2. Schematic view from Cadence Virtuoso depicting a nanomagnetic inverter model, comprising three parts: an ANC, a nanowire, and an output field generator. b) pNML majority gate, comprising the same main three parts as the inverter in a). Instead of one input, the majority gate has three or more inputs, depending on the type of device. All incoming fields are summed at the same instance and applied on the ANC. Each of the shown parts of a magnet is described in Verilog-A file.

[1] International Technology Roadmap for Semiconductors 2.0, 2015 edition, Beyond CMOS chapter.
[2] Experimental Demonstration of a 1-Bit Full Adder in Perpendicular Nanomagnetic Logic, Breitkreutz et al. IEEE Transactions on Magnetics, Vol. 49 Issue 7, 2013.
[3] Majority logic gate for 3D magnetic computing, I. Eichwald et al., Nanotechnology, Vol 25, Nr. 33
[4] Modeling and simulation of nanomagnetic logic with cadence virtuoso using Verilog-A, G. Žiemys et al. Solid-State Electronics Volume 125, November 2016, Pages 247-253.